M2 Quantum Devices

–

Gating of TASE Grown InAs Nanowires for Applications in Fault-Tolerant Topological Quantum Computing

Supervisor:
Fabrizio Nichele

Co-Supervisor:
Carlo Ricciardi

Carlo Ciaccia

IBM *Research-Zurich*

July 12, 2019

To my parents. Without them, I wouldn't be who I am.

ACKNOWLEDGEMENTS

First, I would like to thank Dr. Fabrizio Nichele, research member at IBM Research - Zurich, who accepted me for this internship and always managed to be available in spite of his enormous volume of work. He helped me not only in carrying out the experiments, but also in writing my report and preparing my presentation.

My thanks goes to Heike Riel and Walter Riess, department head and manager respectively of the Science & Technology research activity. Together with Dr. Nichele gave me this amazing opportunity and helped me during my stay.

Markus Ritter is also thanked for his great supervision, patience and availability. He taught me the cleanroom arts with the meticulousness and precision that only a German PhD can have. The beers and German lessons after work were unparalleled as well.

A lot of thanks to Teri Andos, the best householder in this world. She has showed me how to look at the best part of things, how to be fascinated about life, and how to enjoy it in every single part. She has the gift of making people around feel special and unreplaceable. If you ever have the chance pass by that house and stop for a coffee. You will probably end up talking until late in the night jumping from one topic to another. At the end you will go away loving the house, the crazy Greek/American woman that lives there, and even that awful tree that impedes the view.

Last but not least I want to thank Yashashwa Pandey. Together with Teri he made me feel at home away from home. He has been a talking, drinking and hiking buddy as there are no more nowadays. I wish him all the best for his future. Whatever happens, just go for the best view.

I worked in the Quantum Technology & Computing group in the Science & Technology department of IBM Research - Zurich. Scientists here are pioneering scientific breakthroughs across today's most promising and disruptive technologies including the future of artificial intelligence, blockchain and quantum computing. My team deals with hybrid semiconductor/superconductor interfaces for fault-tolerant topological quantum computing. It is a relatively new one, but it is growing together with our lab and our measuring capabilities. We are all highly motivated in doing our best to lead research in this field.

In recent years, III-V semiconductor nanowires (NWs) are attracting increasing interest in the scientific world because of the promise to provide value-added functionalities on integrated circuits by means of spintronic components[1], photonic circuit elements[2, 3] and topological quantum devices[4, 5, 6]. This is mainly thanks to their high carrier mobility and saturation velocity combined with large effective g-factor[7].
The interest of the quantum computing community in III-V nanowires stems from the possibility to engineer, when coupled to a conventional superconductor, a particular state of matter known as topological superconductivity. The reason of the interest is that one-dimensional topological superconductors are predicted to host non-abelian quasiparticles, known as Majorana Zero Modes[8] (MZMs), that may constitute the building block of fault-tolerant quantum computing.

The aim of the project was to achieve local electrostatic control of InAs NWs grown via Template Assisted Selective Epitaxy[9] (TASE), a technique developed at IBM - Research in recent years. Apart from being essential to implement quantum operation on MZMs, local electrostatic control allows to realize multiple devices on the same nanowire, hence representing an important step towards the scalability of this technology. We report on different fabrication procedures along with the challenges each of them presented and characterize the strength of the resulting gates in changing nanowires chemical potential.

A key requirement to reproduce the topological regime is that nanowires growth must be highly crystalline. On of the main evidence of low disorder in semiconducting nanowires is the observation of ballistic transport, whose hallmark is conductance quantization. In the second part of this work we then study electronic transport in several device at cryogenic temperatures and discuss the result.

TASE grown nanowires may constitute a basis for device architectures able to perform *braiding* operation. The interested reader can refer to the rich literature [5, 10, 11] for further information about topological systems and circuits. The final goal of our research is to perform fault-tolerant topologically protected quantum operations through *braiding* of MZMs in NWs networks.

CONTENTS

1

STATE OF THE ART

Many different processes have been developed in order to realize III-V nanowires as building elements of topological quantum devices. The overall trend is to look for material systems that both support MZMs and can be fabricated to provide branched, complex and scalable geometries. Majorana zero modes are predicted to emerge once a superconductor is coupled in an external magnetic field to a semiconductor nanowire having a strong spin–orbit interaction [8]. InSb nanowires are a prime choice for this application owing to the large g-factor and strong Rashba spin–orbit interaction [12]. However, the large lattice mismatch of InSb with insulating substrates limits the quality of the crystal, while its fast growing and flaky oxide makes processing quite tedious [13]. InAs NWs have been explored as well: they are characterized by worse properties in terms of reaching the topological regime (lower g-factor and larger effective mass), but offer better growth and processing. Strong indications of MZMs have been found[1] in both InSb and InAs nanowires [14, 15]. Some of the possible approaches are shown in Fig.1.1. From left to right one moves

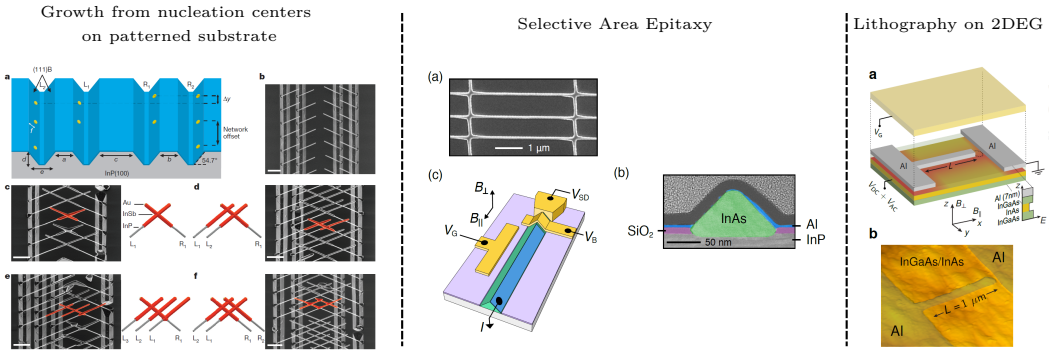

Figure 1.1: LEFT: Metal-Organic Chemical Vapor Deposition (MOCVD) of InSb NWs on a pattered InP substrate via vapuor-liquid-solid method mediated by gold nucleation centers. The superconductor is grown *ex-situ* in a MBE chamber [16]. CENTER: Selective Area Epitaxy (SAE) of InAs NWs on a patterned InP substrate with SiO_2 as a mask. The superconductor is grown *in-situ* [17]. RIGHT: Wirelike device lithographically patterned on a two-dimensional epitaxial InAs/Al heterostructure. A 2DEG is confined in the InAs layer and contacted by the Al film on top [18].

from bottom-up to top-bottom techniques. Bottom-up approaches typically require the optimization of a larger parameter space for each step of the growth process (i.e. substrate orientation, III-V ratio, temperature, etc.). They provide complex con-

1 Tunnelling spectroscopy in electrical transport is the primary tool for identifying the presence of MZMs. Being zero energy states they should produce a zero-bias peak in differential conductance. The height of the Majorana zero-bias peak is predicted to be quantized at the conductance value of $2e^2/h$ at zero temperature, as a direct consequence of the famous Majorana symmetry in which a particle is its own antiparticle. One can distinguish this quantized Majorana peak from possible non-Majorana origins by investigating its robustness to electric and magnetic fields as well as its temperature dependence.

tact schemes, with gates underneath and contacts on top, but also need non-scalable nanomanipulation steps to remove NWs from the substrate once the growth is complete. However, with such techniques, nanowires growth grants a great degree of freedom in combining materials with different lattice parameters and doping profiles, allowing for configurations impossible to realize in thin film geometry.

On the other hand, top-down fabrication is an a attractive route towards scalability. The main issue in this case is basically the fabrication of the substrate and of a high quality interface between the semiconductor and the superconductor. Moreover, patterning through Reactive Ion Etching (RIE) or Inductively Coupled Plasma (ICP) is typically avoided to reduce interface degradation, and defining fine structures with wet etching is quite challenging. Nevertheless, the mobility of a 2DEG is typically higher than the mobility of electrons in a nanowire, allowing for longer mean free path and coherence length. In addition, the interesting feature of the structure shown on the right of Fig.1.1 is that the coupling of electron wavefunction to the superconductor and the distance from the interface can be easily tuned by varying the thickness of the InGaAs barrier layer. Creating a hybrid system that supports topological superconductivity requires a balance between proximity and segregation of constituent materials (electrons should inherit superconducting correlations while retaining large SOC and large g-factor). This balance depends on how much the electron wave function resides in both materials.

The growth of InAs nanowires through SAE somehow shares characteristics of both techniques. in the center of Fig.1.1 a silicon oxide mask is used to selectively grow arbitrarily complex and continuous patterns on a InP substrate. Problems in this case may arise when depositing the superconductor, since the nanowire should remain partially uncovered to allow proper gating. Also, a high selectivity of the mask is required to avoid parasitic growth.

A very attractive prospect is to integrate III-V nanowires on a silicon carrier wafer and make them compatible with CMOS fabrication process. This typically requires dedicated surface preparation steps and buffered layers to suppress the formation of anti-phase boundaries and dislocations. In the following we will describe the growth of InAs nanowires integrated on a silicon wafer via Template-Assisted Selective Epitaxy (TASE)[9]. The wires grow in a MOCVD chamber inside SiO_2 templates defined on a SOI substrate (see Fig.1.2). TASE provides high-quality III–V nanos-

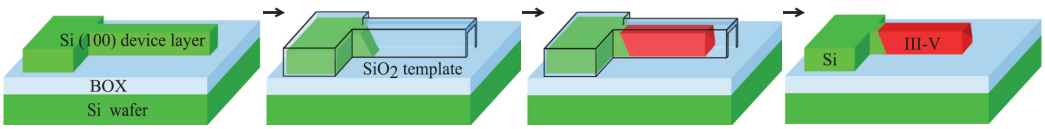

Figure 1.2: Schematic of TASE process. From left to right: shape definition, template formation and silicon back-etching, MOCVD, and template removal if desired. The crystal orientation of the silicon substrate, the direction of the nanowire with respect to it and the facet used as nucleation surface must be properly chosen to optimize the growth. This has been investigated in [19, 9].

tructures with low defect densities and surface roughness, and allows control of the position, orientation and dimensions of NWs. The advantage of the approach lies

in the fact that the first nucleation will occupy all the available material inside the template. This prevents merging of nucleation centers and the associated creation of defects. Moreover, compared to other techniques, the nanowires are encapsulated into the template, which limits surface defect density. Surface passivation is needed only to define ohmic contacts to the wire.

In the thesis presented herein, I report on the device fabrication ranging from template patterning to NWs growth, as well as contacts and gates deposition. The fabrication process has been conducted jointly with other group members. Further details will be given in the next chapter. The goal is to produce a gating scheme which allows to tune conductance of the nanowire and to perform DOS spectroscopy.

2

FABRICATION PROCESS & CHALLANGES

In this chapter we will divide the fabrication process into four sections. In each section we will discuss a particular step along with the challenges it presented and the solutions we found. At this point I would like to state that I have not taken part in any optimization procedure but put my focus on learning the fabrication steps and on the conductance of the transport experiments.

2.1 NANOWIRES TEMPLATE

Our substrates consist of 8 inches [100]-oriented SOI wafers provided by *Soitec*. The overall thickness of each wafer is 740 μm, the one of the buried oxide is 150 nm and the silicon on top is 30 nm thick. Each substrate was diced into 6 cm x 6 cm wafers using a diamond saw and the ones on the corners (no. 1, 3, 7, 9) were discarded. Out of each sub-wafer we patterned nine chips to be diced each into four quadrants before bonding. This produces a good compromise between production speed and

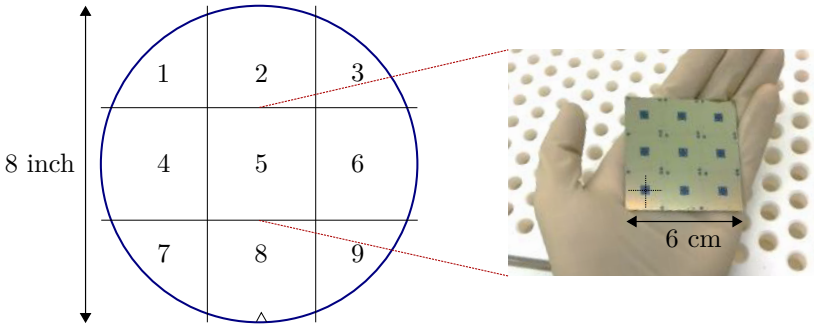

Figure 2.1: Schematic of wafer labeling and 6 cm x 6 cm chip after markers patterning.

flexibility, allowing to perform simple steps at a wafer level, but also to try different recipes on more delicate processes at a chip level.

Tungsten markers (100nm) for alignment of optical and e-beam masks during subsequent steps were patterned using optical lithography and RIE on a 100 nm-thick tungsten layer. Everything was capped into a 300 nm SiO_2 protection layer and device areas were opened with an HF dip.

Based on previous work [9, 19] all nanowires have been oriented along the [110] direction, which is to say the one perpendicular to the notch in Fig.2.1. The degree of crystallinity turns out to benefit from this adjustment. NWs pattern is defined into Hydrogen silsesquioxane[1] (HSQ) by electron beam lithography and then transferred into the SOI. ICP is used instead of RIE since we aim to obtain a nanowire sidewall as sharp as possible to have its width properly defined. With ICP the ion density in the plasma and their energy can be controlled independently thanks to two different

1 HSQ is a negative resist with high resolution.

RF generators. This allowes to increase etching anisotropy. The silicon is etched in a HBr plasma at 80 W with the ICP generator at 800 W. This recipe has an etching rate of approximately 1.8 nm/s, and its selectivity with respect to the underlying SiO_2 is 1:3.
The HSQ is then stripped in HF. It is a very delicate step since the SiO_2 below the silicon is attacked and this may cause the NW to detach. An HF dip of 12 s on 50 nm of HSQ was found to yield good results. 2 μm long Silicon NWs with widths ranging from 40 nm to 70 nm have been obtained (see Fig.2.2).

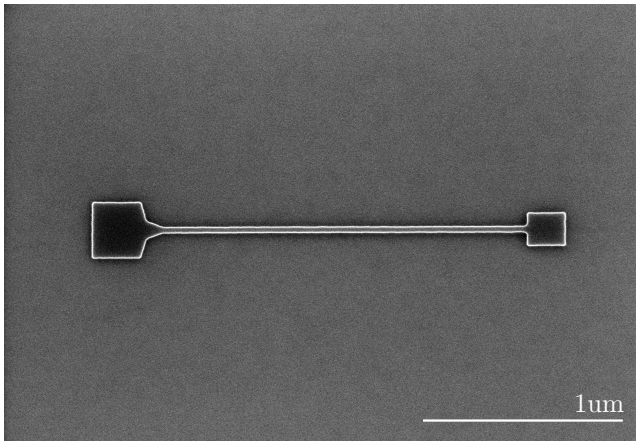

Figure 2.2: SEM image of a silicon nanowire after ICP etching and HSQ stripping. The length is approximately 2 μm. The effective length of the InAs will be defined by the contacts [sec. 2.2]

We currently are at the first step in Fig.1.2, next step being the deposition of the silicon oxide template. Since it is crucial to cover the Si nanostructure conformally, Atomic Layer Deposition (ALD) is used. This is a slow deposition process that involves self limiting reactions between precursors and the substrate. The deposition of the 60 nm we aim to obtain take approximately 8 hours. It occurs at 300°C in 250 W oxygen plasma using Tris[dimethylammino]silane (3DMAS) as silicon precursor.
The wafer is then annealed at 850°C for 30 s to improve oxide properties. The etch rate of the ALD-SiO_2 after annealing is approximately 1.6 nm/s in buffered HF. It is worth mentioning that thermal oxidation would yield the best SiO_2 properties (dielectric strength, thermal isolation, uniformity,..), but is not well suited for patterned structures due to stress developing at the edges [20].

By splitting the template deposition step in two parts sidegates and contacts may be patterned in between and hence encapsulated. This would avoid any further step after nanowire growth, reducing the risk of damages and the need of sulfuric passivation [sec 2.4]. The realization of such encapsulated gates and contacts will be the subject of the next section.

2.2 ENCAPSULATED GATES

The first material we explored to realize gates and contacts to the nanowires was TiN. The two main advantages of TiN are that it can be deposited in-situ with ALD

right after the first 30 nm of SiO_2, and it has well established adhesion properties to silicon oxide [21]. The deposition occurs at 300°C in nitrogen/hydrogen plasma at 200 W using Tetrakis[dimethylamino]titanium (TDMAT) as Ti precursor.

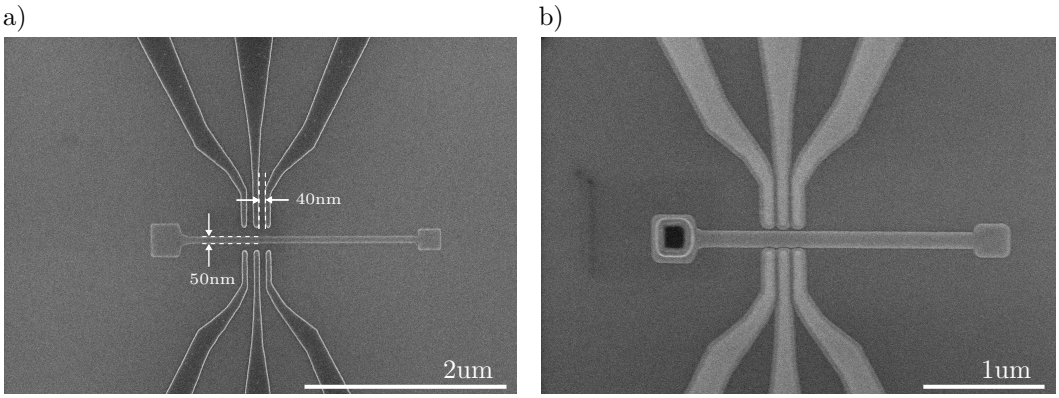

Figure 2.3: a) TiN gates patterned using ICP. b) The same gates encapsulated. At this step in the fabrication process a window in the template was opened using RIE to etch the first 50 nm and an HF dip to finally reach the silicon nanowire (see sec. 2.3).

Gates were patterned into a 20 nm-thick TiN film by ICP etching using an HSQ mask. The same recipe used for silicon has been exploited. In this case the etching rate is approximately 1.6 nm/s. Everything was then covered by the second oxide layer. Fig.2.3b shows an example of a gating structure able to tune the coupling of a quantum dot along the nanowire to the surroundings (outer sidegates) and to adjust its chemical potential (inner sidegates).

TiN gates have one main drawback that we only discovered when the device fabrication was completed. During the annealing following the gates encapsulation, titanium silicide may form at the Ti-SiO_2 interface due to the dissociation of SiO_2. As described in [22] this occurs for pure Ti already at low temperature (<500°C) and can involve up to 100 nm of oxide. In our case, due to the presence of nitrogen, the reaction could be weaker or even absent. Still, if it occurs, the effective distance among gates would be much less then the designed one, leading to leakage issues. One could reduce the SiO_2 dissolution by decreasing the annealing temperature, but the gates would still need to withstand the growth of the nanowires, which occurs at approximately 550°C. A possible solution would be to exchange the oxide (i.e. Si_3N_4), but this would decrease the selectivity of nanowires growth (see sec. 2.3).

After nanowires growth and contacts deposition, the chip was glued on a chip carrier and then bonded using an aluminum-based ultrasonic wire bonder. All measurements have been obtained applying a DC voltage (Yokogawa GS200) to one contact and feeding the output from the other contact to an IV converter with variable gain. The output from the IV converter was then measured using a digital multimeter (Keysight 34465a). What we have measured is a finite gate-to-gate and gate-to contact resistance on several devices, suggesting that the integrity of structure is not preserved. Plots in Fig.2.4 show a resistance of approximately 150 kΩ between gate and contact (6-8) and of 210 kΩ between two gates (8-11). Also, conduction

through the nanowire (14-6) is compromised.

Another route to realize encapsulated gates is to use a more stable metal such as tungsten. Tungsten silicide forms at much higher temperatures (1000°C) [23]. In this case however, patterning issues came into play. Possible strategies, along with the results they led to, are summarized in Fig.2.9.

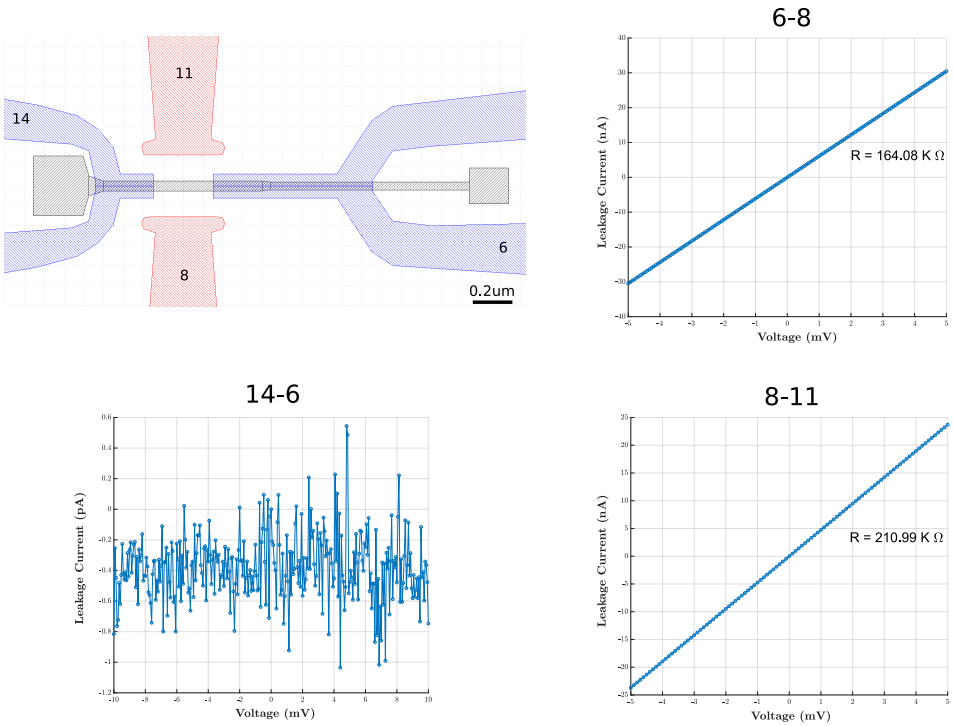

Figure 2.4: Leakage measurements of a device with TiN gates. TOP-LEFT: Device contact scheme. Contacts to the nanowire are realized as described in sec 2.4. IV-CURVES: A finite resistance is measured between the two gates and from one gate to the left contact (8-11, 6-8). The nanowire (14-6) does not conduct.

Initially, we transferred an HSQ pattern into a 20 nm-thick evaporated tungsten layer via 2 min RIE using SF_6 in nitrogen plasma at 25 W (18 nm/min). The gates turn out to be quite well defined. However, because of the presence of the silicon nanowire, the amount of tungsten to be removed in correspondence of the height step is approximately 3 times the one to be removed elsewhere (40 nm of Si + 20 nm of tungsten). Therefore, tungsten residues remain near the sidewalls (see Fig.2.9a). Such residues are difficult to remove since the etching recipe attacks both the underling silicon oxide, with a selectivity of approximately 1:2, and the HSQ on top, with a much worse selectivity. The risk is that either we reduce too much the oxide thickness or we consume the HSQ on top and start etching the gates themselves. The same probably happened with the TiN etching and contributed to leakage, even if we did not notice it from the SEM images. Metallic residues on the sidewalls of the nanowire are not acceptable since they will screen the effects of the gates.

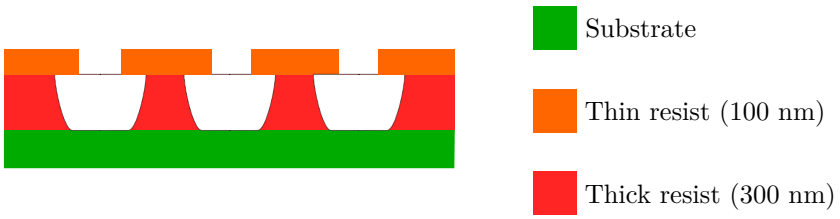

Figure 2.5: Double-layer structure. The two resists are such that at a given dose the lower layer is overexposed, so that the subsequent development produces the desired undercut.

Another possibility could be to perform a lift-off step. This means to expose and develop a positive resist, deposit the desired metal, and then strip off the mask along with the unwanted metal deposited on top. Typically one tries to obtain a exposure profile that gets larger when approaching the substrate. In this way the deposited metal does not get stuck on the sidewalls and the resist can be easily washed off. This is mostly obtained by means of double-layer structures (see Fig.2.5). Sometimes, however, the lift-off can still work with a single layer resist provided that the thickness of the metallic layer is few times smaller than the resist. Spinning of AR-P-672.03 (PMMA) at 500rpm for 5 s, and at 6000rpm for 40s, using a hexamethyldisilizane (HMDS) adhesion promoting layer, gives approximately 100 nm. The process will work if we aim to deposit 20 nm thick metallic layer. Single-layer lift-off becomes mandatory when moving to critical dimensions of approximately 50 nm. This is because the undercut in the lower resist may compromise the stability of the mask.

However, tungsten evaporation is quite demanding since the material needs to be locally heated up to 3400°C. Moreover, because of the high temperature, tungsten particles may burn resist edges and fall down in the deposition areas. This turns into flipping over of the gates on top of each other when removing the resist (see Fig.2.9b). Anyway, evaporation remains a better option compared to sputtering since it leads to less metal deposition on the resit sidewalls (less conformal covering).

Finally, obtaining fine structures with wet etching (i.e H_2O_2) is quite challenging. The mask design must take into account the isotropy of the process, for example by exposing resist areas smaller than the desired gates distance.

In parallel to the search of a good recipe for encapsulated gates, we carried on the growth of InAs nanowires whose gates will be defined by a lift-off step at the end. The growth process will be the subject of the next section.

2.3 NANOWIRES GROWTH

Before starting the growth, one needs to access and then back-etch the silicon nanowire inside the template. The SiO_2 cap is opened by patterning a Chemical Semi-Amplified Resist[2] (CSAR 62) with e-beam lithography, and then etching the oxide. The etching is done with a first RIE step followed by a buffered HF (BHF)

2 CSAR is a positive resist where an acid generator is introduced to increase sensitivity and contrast (>15).

dip to remove the last 30 nm. The RIE step ensure a high aspect ratio, while the HF ensures the underlying SOI is not attacked and enlarge the window for the diffusion of III-V precursors. Etching is performed by CHF_3 in argon atmosphere with an RF power of 100 W for 2 min at 10 mTorr (etch rate of 16 nm/min). Results of this step has already been shown in Fig.2.3b.

To have the possibility to adjust the subsequent processes from chip to chip, the wafer is diced into 2 cm x 2 cm chips. The back-etch of the silicon nanowire is done in 2% wt. Etching in Tetramethylammonium hydroxide (TMAH) solution at 80°C for 18min yields approximately 1.2 μm of back-etch. Directly before TMAH a 2 s dip in BHF is required to remove the 2 nm native oxide on the silicon surface. The etching time was determined from several etch tests and SEM characterizations. It is important to leave part of the nanowire to serve as nucleation point for the InAs nanowires. An example is shown in Fig.2.6. TMAH etches silicon anisotrop-

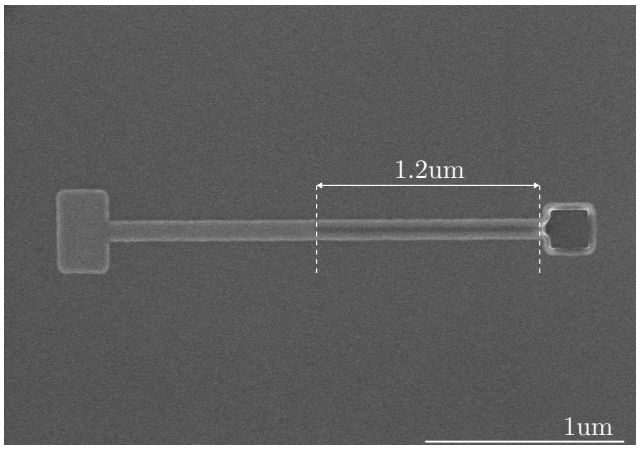

Figure 2.6: SEM image taken by Markus Ritter while developing the Silicon back-etch recipe. A 2% TMAH solution gives an etch rate of approximately 1 nm/s.

ically and exposes {111} planes, which are characterized by a smaller etch rate. Such planes were found to be best suited to reduce the amount of defects in the nanowires[19]. Directly after the back-etch the chip is transferred to the MOCVD chamber where the InAs is grown starting from the Si seed.

In contrast to Molecular Beam Epitaxy (MBE), in MOCVD the growth of crystals occurs by chemical reactions and not physical deposition. The process does not take place in Ultra High Vacuum (UHV), but starts from gas phases at moderate pressure (60 Torr). Gaseous precursors are introduced in the reaction chamber via so called bubblers: in a bubbler a carrier gas (hydrogen in our case) is pumped through the metalorganic liquid, picks up some metalorganic vapor and transports it to the reactor. The amount of metalorganic vapour transported depends on the rate of carrier gas flow and the bubbler temperature. Surface reaction of the metalorganic precursors on the heated substrate creates the conditions for crystalline growth. MOCVD is actually the only suitable process for growing the nanowire inside the silicon oxide template, since deposition is not uniform but occurs at nucleation points (the silicon nanowire in our case) hidden by the mask. The semiconductor growth conditions are tuned to ensure epitaxial growth on the exposed substrate,

but not on the dielectric mask.

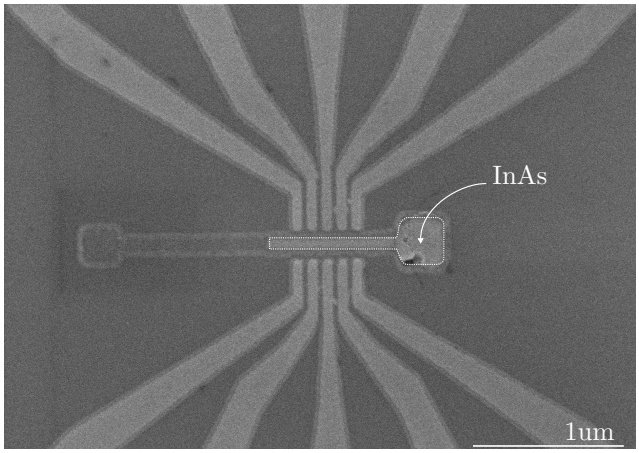

Figure 2.7: SEM image of the InAs nanowire. Overgrowth outside the template has been removed. Devices on this chip were gated using encapsulated TiN.

Selective epitaxy of InAs nanowires is obtained using trimethylindium (TMIn) and tertiarybutylarsine (TBAs) at 550°C with a V/III ratio of approximately 70. The V/III ratio, meaning the ratio between As and In precursors in the chamber, must be properly tuned to avoid inhomogeneities caused by different diffusion properties. Indeed, while In is able to diffuse along the sidewalls of the nanowire during the growth, As is not. That is why the concentration of TBAs must be higher.
The growth rate increases as soon as it becomes easier for precursors to reach the nanowire. Typically what we have done is to grow until the nanowire overgrows outside the template, for then carefully polish the excess. This implies to leave a chip with a back-etch of 1.2 μm in the chamber for about 2.5 h. We also understand that a too deep back-etching of the silicon nanowire would not be beneficial since it would decrease considerably the growth rate. Results are shown in Fig.2.7. Notice that this device has TiN encapsulated gates, and after the growth there is no evidence of the reaction with the surrounding silicon oxide. This means that, if the reaction is indeed the reason for gate-to-contact and gate-to-gate leakage, it must be quite limited compared to what presented in [22], where the oxide is said to be completely dissolved.

2.4 GATES AND CONTACTS LIFT-OFF

As mentioned above, realizing encapsulated gates and contacts would be nice in order to avoid further processing on the chip after nanowires growth. However, it is sometimes worth testing the device first (and hopefully to observe some interesting physics), and then adjust less relevant details.

On the 'second generation' chips we deposited gates and contacts in a lift-off step at the end of the growth using a double-layer mask. In this way one avoids any high temperature step on the electronic connections. The double-layer mask has been realized by spinning 300 nm of AR-P 669.04 (PMMA) followed by 100 nm AR-P 672.03 (PMMA). After each spinning a hard bake at 180°C was performed. The two resists are such that at a given dose the lower layer is overexposed, so that the

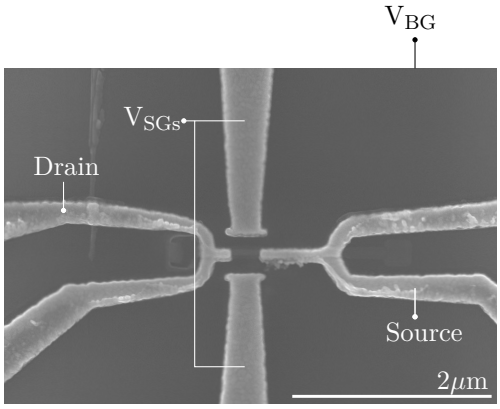

Figure 2.8: SEM image showing a completed device after gates and contacts deposition. In this case gates are much larger than those of previously shown designs since their aim is to tune the chemical potential of the nanowire.

subsequent development produces the desired undercut.

In order to contact the nanowires one needs to open the silicon oxide template prior to the evaporation. This is done once again with a RIE step followed by a BHF dip. Moreover, to stabilize nanowires surface and preventing fast oxidation, the chip undergoes a 10 minutes ammonium sulfide dip and is then directly transferred to the evaporation chamber. This step is crucial in order to ensure ohmic contacts [24]. In principle, it could be avoided by realizing encapsulated contacts. If we were able to pattern contacts on the silicon nanowire before InAs growth, the actual nanowires could then be contacted during the growth itself. We have not explored this route yet. The result after a double-layer lift-off of Ti/Au (20nm/150nm) are shown in Fig.2.8. Here we were able to use a unique double-layer mask for contacts, gates and contact pads since they gate a quite large. Structures like the ones in fig.2.3, whose purpose is to realize quantum dots along the nanowire, require instead a dedicated single-layer lift-off step (and therefore an additional e-beam exposure).

The contacts and gates structure in Fig.2.8 is the one that will be considered in following chapter, where we will characterize electrical transport in our TASE grown InAs nanowires showing evidence of ballistic transport up to a length of 300 μm.

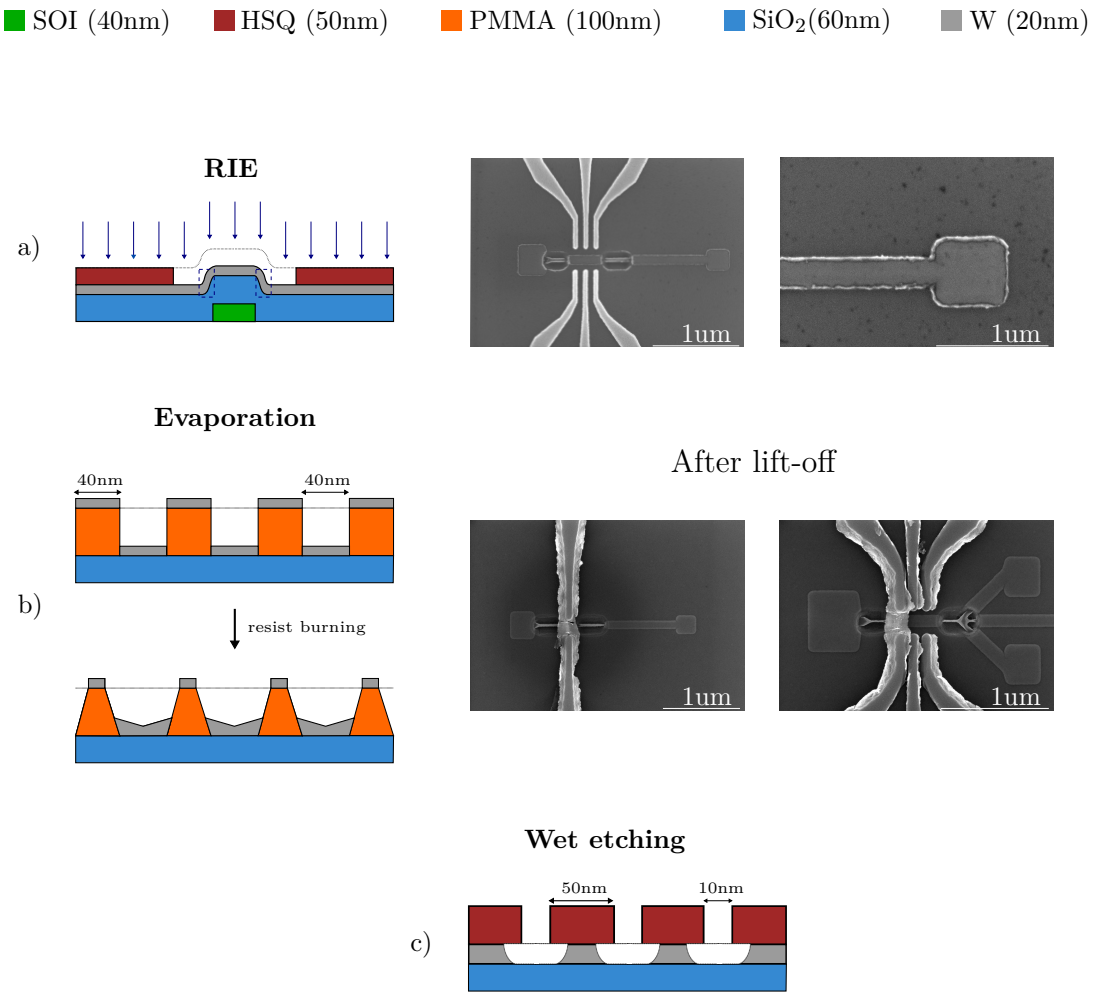

Figure 2.9: Summary of gates patterning techniques and SEM images of the results. Notice that these trials were done on a dummy wafer where a wrong layer was exposed during a lithography step. a) Section. The HSQ pattern is transferred into a tungsten (W) layer by reactive ion etching. Residues remain on the sidewalls of the nanowire where the tungsten effective thickness is larger. b) Sideview. Gates are defined by tungsten evaporation on a 100nm thick resist and subsequent lift-off. Resist burning during the evaporation step causes tungsten to accumulate on the sidewalls. After resist removal the gates flip on top of each other. c) Sideview. HSQ pattern transferred in the tungsten layer by wet etching (H_2O_2). Because of the isotropy of the process under-etching must be taken into account in the mask layout.

3

BALLISTIC TRANSPORT

Ballistic transport in semiconductor nanowires is a key requirement for the observation of MZMs[25]. Let us consider a semiconductor wire with dimensions $t \cdot w \cdot L$ con-

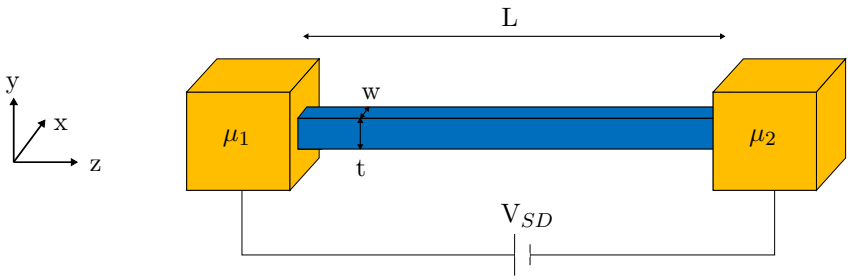

Figure 3.1: Schematic of a semiconductor nanowire to which a voltage bias V_{SD} is applied via two metallic contacts.

tacted by two metallic contacts to which we apply an external bias $eV_{SD} = \mu_2 - \mu_1$, where μ_1 and μ_2 represent the respective Fermi levels. If the dimensions of the semiconductor are large, its conductance is given by $G = \sigma wt/L$, but as soon as they get smaller than the electron mean free path λ, electrical transport cannot be described in terms of scattering mechanism (conductivity σ) anymore. In such regime the phase coherence of electrons is not destroyed by scattering events, and the transport is called ballistic. The ballistic effect can be observed if the elastic mean free path is large compared to the sample size L as long as the sample size L is not much larger than the phase coherence length λ_ϕ. The hallmark of such transport regime is conductance quantization, which is routinely observed in QPCs on 2DEG, but is more difficult to achieve in nanowires due to structural imperfections and surface states.

In order to understand the phenomenon let us recall the simple model of a one-dimensional channel where carriers are confined in two dimensions (x,y) and free to move along the third one (z). If the channel is taken to be much longer with respect to the cross-section, it can be treated as translationally invariant in that direction. The time independent Schrodinger equation for the electron wave function $\psi(\mathbf{R})$:

$$\left[-\frac{\hbar^2}{2m^*}\nabla^2 + U(\mathbf{R})\right]\psi(\mathbf{R}) = \epsilon\psi(\mathbf{R}), \tag{1}$$

becomes separable. Assuming that the confining potential is only a function of $r = (x, y)$, this means the Schrodinger equation can be reduced to a two-dimensional problem by taking $\psi(\mathbf{R}) = \phi(x, y)e^{ik_z z}$:

$$\left[-\frac{\hbar^2}{2m^*}\nabla^2_{x,y} + U(\mathbf{r})\right]\phi(\mathbf{r}) = \epsilon_{x,y}\phi(\mathbf{r}). \tag{2}$$

For an infinitely deep quantum well (good approximation for the interface InAs/SiO_2), the quantization energies are:

$$\epsilon_{x,y} = \frac{\hbar^2\pi^2}{2m^*}\left[\frac{n_x^2}{w^2} + \frac{n_y^2}{t^2}\right], \tag{3}$$

where n_x,n_y = 1,2,3,.. . The total energy will be

$$\epsilon = \epsilon_{x,y} + \frac{\hbar^2 k_z^2}{2m^*} \tag{4}$$

Finally, the spin degenerate density of states for one subband of a one-dimensional channel can be calculated from the number of k-states per unit length $N = 2k_z/\pi$ and the free space dispersion relation $k_z = \sqrt{2m^*E/\hbar^2}$ as:

$$\rho(E) = \frac{dN}{dE} = \frac{1}{\pi\hbar}\sqrt{\frac{2m^*}{E}} \tag{5}$$

Therefore the total density of states reads:

$$DOS(E) = \sum_{n_x,n_y} \frac{1}{\pi\hbar}\sqrt{\frac{2m^*}{E-\epsilon_{x,y}}}\Theta(E-\epsilon_{x,y}) \tag{6}$$

The overall energy structure is summarized in Fig.3.2. Assuming 'reflectionless'

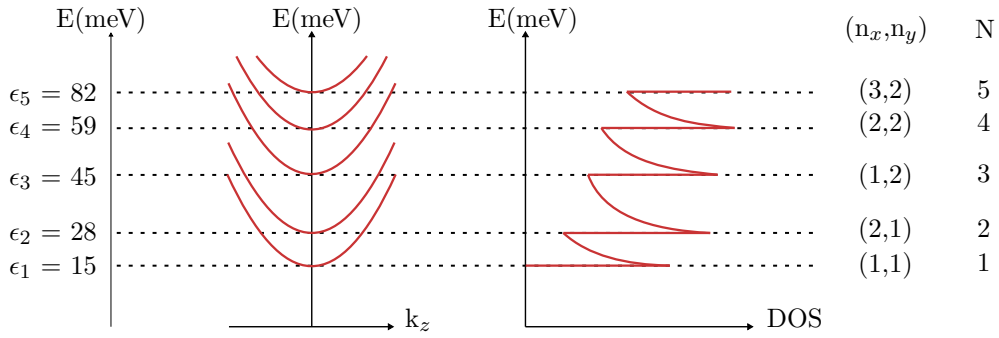

Figure 3.2: Adapted from [26]. Subband quantization and density of states of a nanowire with t = 40nm and w = 60nm. The energy levels are computed according to equation (3). In the longitudinal direction the dispersion relation becomes parabolic.

contacts, meaning that the electrons can be injected in the wire with probability equal to 1, the net current is given by the difference of the right-moving (k_z>0) and left-moving (k_z<0) electrons. Recalling that classically $j = nev$, the contribution from one single mode having cut-off energy ϵ_N is given by[1]:

$$I = wt\frac{e}{2}\int_{\epsilon_N}^{\infty} \rho(E)v(E)\left[f(E,\mu_1) - f(E,\mu_2)\right]\frac{L}{Lwt}dE \tag{7}$$

where the factor 1/2 has been included to consider only left- or right-moving states in each term. To avoid the assumption of reflectionless contacts and perfect channel it is sufficient to introduce a coefficient T(E) inside the integral, accounting for

1 Notice that n should be a density and ρ is defined per unit length. That is the reason for the factor at the end of the integral.

injection and transmission probability.
It is straightforward to show that the factor $\rho(E)v(E)$ reduces to $4/h$. Moreover, at low temperature, the difference of the Fermi functions substantially select the energy range in between μ_1 and μ_2. Finally, to include the contribution of multiple subbands one needs to count the number of modes with cut-off energy smaller than E. We have:

$$I = \frac{2e}{h}\sum_N \int_{\mu_1}^{\mu_2} \Theta(E-\epsilon_N)dE = \frac{2e}{h}\sum_N [\mu_2 - max(\mu_1, \epsilon_N)]. \tag{8}$$

If the number of modes is constant and equal to N in the interval [μ_1,μ_2], then, assuming equal drop on both contacts[2], one can also write:

$$I = \frac{2e^2}{h} V_{\mathrm{SD}} = G_0 V_{\mathrm{SD}}, \tag{9}$$

where the quantity $\mathrm{G}_0 = \frac{2e^2}{h} \approx (12.9\ \mathrm{k\Omega})^{-1}$ is called conductance quantum and μ is the chemical potential of the system.
The nanowire resistance in the ballistic transport regime is then quantized and independent on the wire length. It is important to notice that such resistance does not arises from the wire itself, but it is instead due to the redistribution of the infinite numbers of current-carrying modes of the contacts into the few current-carrying modes at the interface with the nanowire.

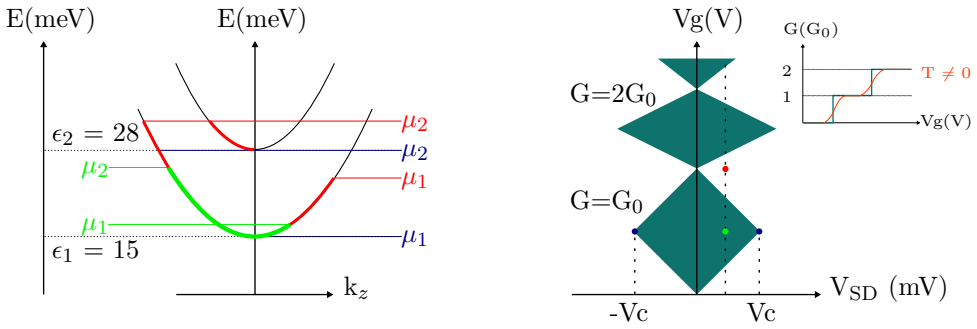

Figure 3.3: Several possible alignments of the contacts Fermi levels with respect to the subbands structure and the resulting quantization of conductance. The Fermi level of the system μ is assumed to be halfway from μ_1 and μ_2. Green) Bias voltage smaller than subbands spacing and bias window inside the first subband. The conductance of the wire is expected to be G_0. Orange) Bias voltage smaller than subbands spacing and bias window partially in the first and partially in the second subband. The conductance of the wire is not quantized in integer multiples of G_0. Blue) Bias voltage equals subband spacing ($\Delta\epsilon = \mathrm{V}_c/\mathrm{e}$). The inset shows the behavior of conductance as a function of the gate voltage at zero and finite temperature.

Assume now we apply a zero DC bias and measure the wire conductance using a lock-in amplifier. If the amplitude of the sinusoidal signal in input is sufficiently

2 More generally, on increasing $\mathrm{V_{SD}}$ the population of the left-moving states increases to μ + meV$_{\mathrm{SD}}$ and the one of the right-moving states decreases to μ - (1-m)eV$_{\mathrm{SD}}$. Here m is a phenomenological parameter between 0 and 1.

small with respect to the applied gate and bias voltage then what we measure is directly the differential conductance $G = \partial I/\partial V_{SD}$. When varying the gate voltage Vg (either the sidegates in Fig.2.8 or a backgate), and therefore the chemical potential of the system, the conductance is expected to increase in integer multiples of G_0. However, for each subband there exist a critical bias voltage V_c above which the corresponding plateaus disappears. In that case (orange point in Fig.3.3) the number of occupied subbands will not be the same for both velocity directions and the conductance will not be quantized in integer multiples of G_0 anymore. This is clear when looking at the expression of the current when μ_1 and μ_2 are in two different subbands (i.e. the first two):

$$I = \frac{2e}{h}[(\mu_2 - \epsilon_2) + (\mu_2 - \mu_1)] = \frac{2e}{h}[(\mu + eV_{SD}/2 - \epsilon_2) + eV_{SD}]$$
$$\rightarrow \quad G = \frac{3}{2}G_0$$

Therefore, when plotting the conductance as a function of both the bias and the gate voltage, a diamond-like structure will appear: inside each diamond G will be quantized in integer units of G_0. From a G-(V_g,V_{SD}) two-dimensional map we should be able to compute the intersubband spacing by looking at those points where μ_1 and μ_2 coincide with subband edges. The situation is summarized in Fig.3.3: intersubband spacing is given by $\Delta\epsilon = V_c/e$ (blue point in Fig.3.3). The effect of increasing temperature is to smooth out the transition until plateaus are basically not visible anymore (see inset of Fig.3.3).

Ballistic transport in TASE InAs nanowires has been investigated using the set-up described in Appendix A1. The sample can be cooled down to 1.6 K thanks to a Physical Property Measurement System (PPMS) which can also apply a magnetic field up to 9 T directed parallel to the cryostat axis. In a typical measurement circuit an AC voltage of variable amplitude and frequency is fed into the device source through a lock-in amplifier. The out coming current is collected by an

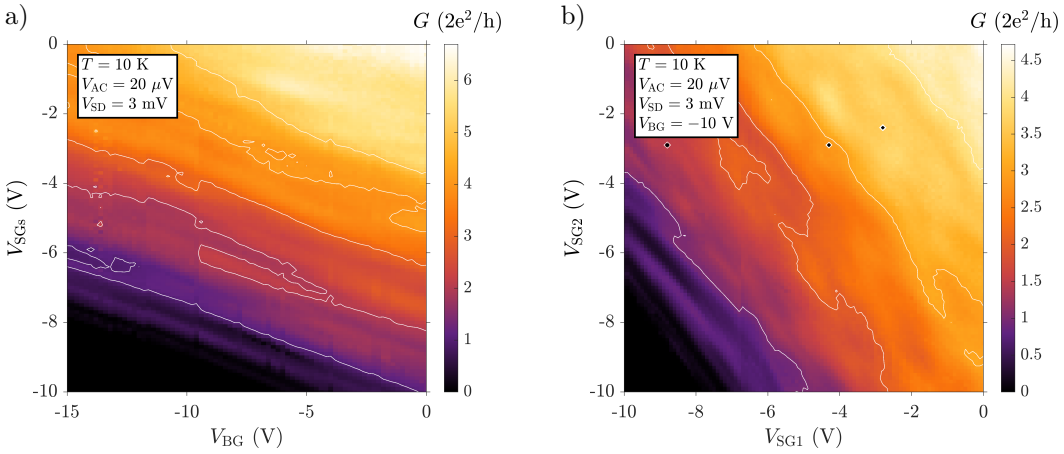

Figure 3.4: 2D Conductance maps. Contour plots at integer multiples of G_0 are shown in both figures. a) Sidegates vs backgate strength: at sidegates voltages above -6 V the backgate is not able to drive the nanowire to pinch-off. b) Sidegates are symmetric in driving the nanowire chemical potential.

IV-converter with variable gain, whose output is read by the lock-in itself. DC bias

is provided by two Yokogawa-GS200 DC sources (range ± 30 V) while gate voltages are fixed by a ultra-stable high-resolution D/A Converter (QDAC, range ± 10 V and less than ±2 μV drift in 10 hours). We did not use four probes for the present measurements since we were limited in the number of available pins on the cryostat breakout box, and we preferred to test as many devices as possible. If plateaus are observed then one can then calculate the contact resistance by shifting the first plateau to 12.9kΩ.
A backgate was realized by metallizing the substrate with a Ti/Pt (10 nm/30 nm) layer. We noticed that the influence of the backgate is weaker with respect to the sidegates. This is confirmed by the 2D map of the conductance as a function of sigate and backgate voltage (see Fig.3.4a). The two sidegates are symmetric (see Fig.3.4b). At zero bias the nanowire conducts while at sufficiently negative bias voltages it is pinched-off. Indeed, in InAs nanowires the Fermi level is typically pinned in the conduction band because of surface states.

Results for a nanowire with L = 300 nm and w = 60 nm are shown in Fig.3.5. The sidegates and the backgate voltages have been swept together from 0 V to -8 V, and the conductance was measured at 4 K, 10 K, 15 K and 20 K. A DC bias of either 3 mV or 5 mV was applied to the device.

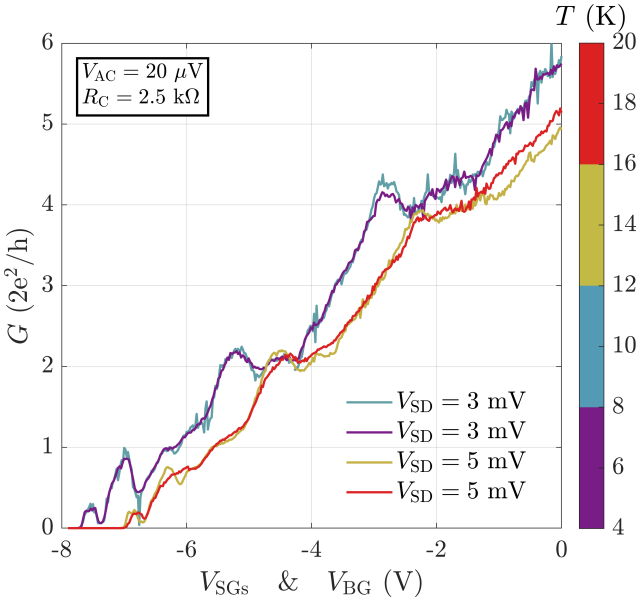

Figure 3.5: L = 300nm, w = 60nm. a) Nanowire conductance as a function of the gate voltages at different temperatures (4 K, 10 K, 15 K and 20 K) and bias voltages (3 mV, 5 mV).

The conductance measurement offers the possibility to highlight some interesting features. A contact resistance of 2.5 kΩ has been subtracted in the plot of Fig.3.5 to match the first plateau. Three plateaus are visible in the two lowest temperature characteristics where a bias of 3 mV has been applied (G_0, $2G_0$, $4G_0$). The third plateau is not visible potentially because the 3rd and 4th subbands are degenerate. This may happen if the effective geometry of the nanowire is slightly different from the designed one. The width of the plateaus is reduced the more the temperature is increased as predicted by theory: the first plateau barely starts in the red and

yellow curves.
Another point to be addressed is the one related to the conductance oscillations and kinks. Deviations from the ideal behavior can be due to several reasons[27]. For example, changing the gate voltage can change the charge of impurity sites, thereby modifying channel transmission (see kinks in the conductance characteristic). Also, the transmission probability T(E) can undergo resonant oscillations if the potential landscape across the wire is not smooth but has local maxima and minima due to coupling to the surrounding. In this case coherent backscattering causes electrons to be transmitted resonantly. Nanowire transmission seems to be dependent on the bias voltage as well. If we assume that coherent backscattering is the reason of the transmission oscillations, then the most immediate way to suppress them is to reduce electron coherence length by increasing the temperature. Indeed conductance oscillations seem to be smoothed out in the 15 K and 20 K characteristics.

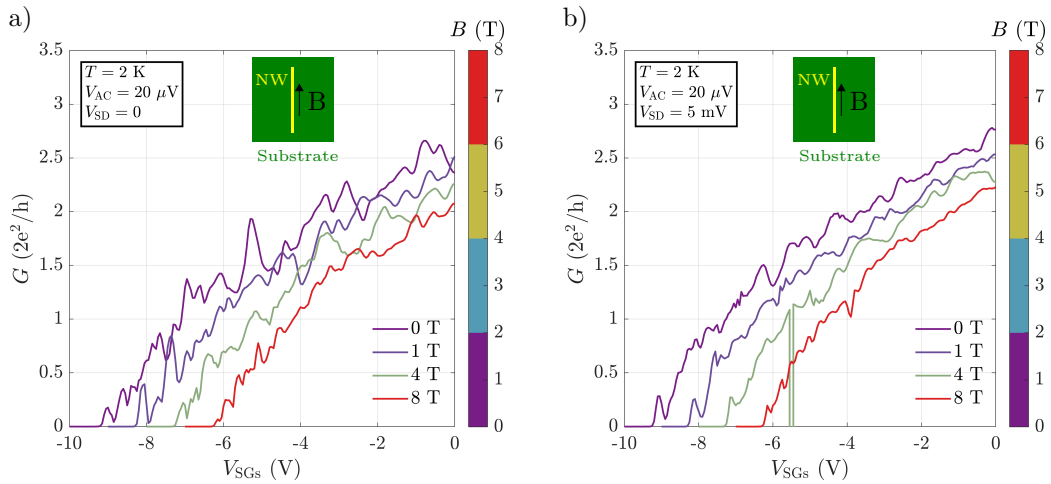

Figure 3.6: L = 300nm, w = 60nm. Curves have been shifted horizontally in steps of 1V to highlight the differences. a) Conductance of the nanowire as a function of the sidegates voltage at zero bias voltage for different parallel magnetic fields. V_{BG} held at 0 V b) The same as in a) but with V_{SD} = 5 mV.

Analogously, such coherent oscillations disappear when increasing the magnetic field. In Fig.3.6 the wire conductance is measured as a function of the sidegates voltage at different magnetic fields. After a certain number of voltage sweeps on the same device, plateaus are observed to disappear. This is probably because of charging-induced damages that reduce the electrons mean free path but preserve the coherence length. However, the amplitude of the oscillations decreases with the magnetic field.
The dependence of the oscillations on the magnetic field is related to the so called Aharonov-Bohm phase, that depends on the magnetic flux thorough a closed electronic path. As a rule of thumb one can assume that modulations of the conductance because of the Aharonov-Bohm phase occur as long as the classical cyclotron radius of the electron $R_c = \hbar k_F/eB$ is large compared to the width of the nanowire [27]. In the previous considerations, B is assumed to be perpendicular to the plane of the wire, but we only applied it parallel to such plane and the wire axis. Nevertheless, some effects were observable probably because the sample was not centered in correspondence of the maximum field uniformity. A more systematic study is

definitely required.
In Fig.3.6b we also notice that such oscillations are reduced with respect to the oscillations in a) when a DC bias is applied . This is probably because we average the measurement over the bias window.

Finally, Fig.3.5 shows two 2D maps of the wire conductance at 2.5 K. The sidegates were swept from 0 V to -8 V (-9 V in the right side plot) and the bias voltage from -30 mV to +30 mV (-20 mV to +20 mV). The backgate was held at -10 V (-5 V). A critical bias voltage of approximately 11 mV can be extracted, in good agreement with the 13 meV subband spacing predicted by theory.
In the plots on the left side the conductance is smoothed out at sidegates voltages below -5 V. This happened because for some errors in the cryostat temperature stabilization. The temperature rose gradually up to 112 K before we were able to solve the issue. The measurement is shown to highlight once again the effect of temperature on the wire conductance.

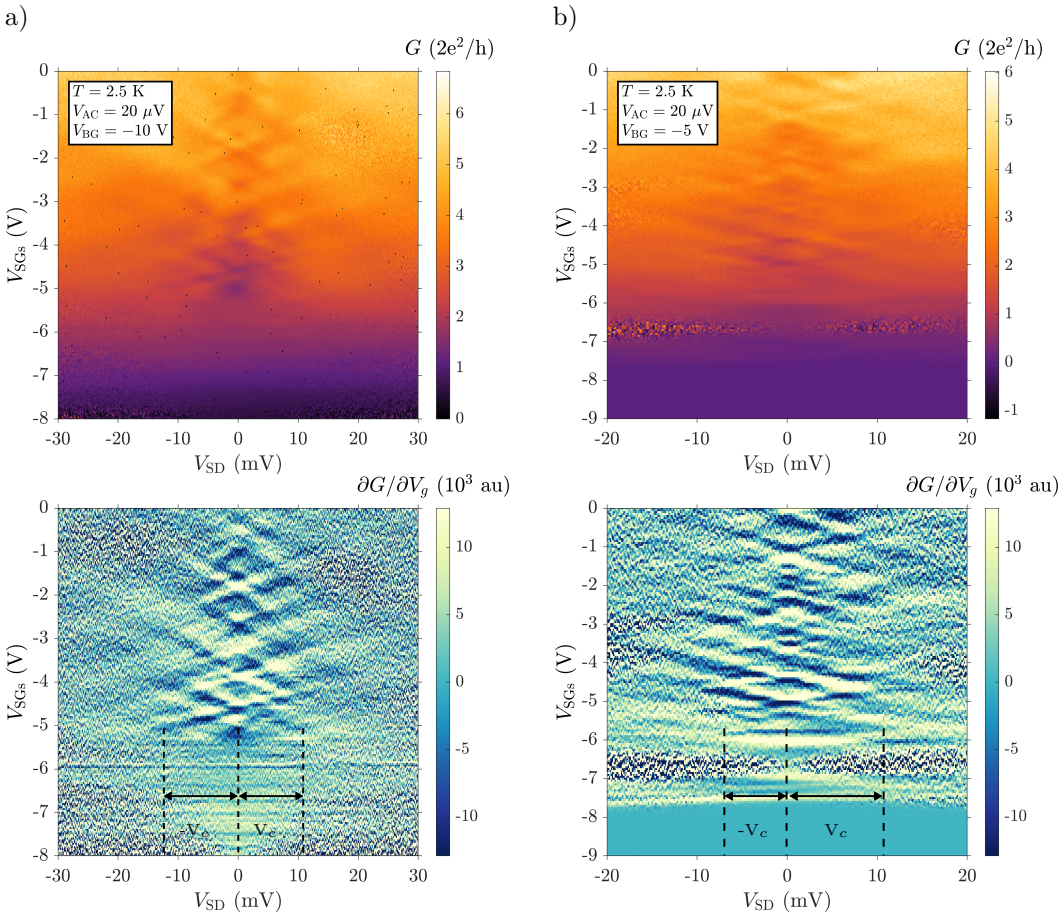

Figure 3.7: a) Two-dimensional map of the conductance as a function of the source bias and sidegates voltage. The backgate was held at -10V and the temperature at 2.5 K. Two highlight transitions features, the same map is plotted below differentiated with respect to the sidegates voltage. b) Same as in a but with V_{BG} = -5 V.

4

CONCLUSION & PERSPECTIVES

In the frame of the present work we have achieved evidence of ballistic transport in TASE grown InAs nanowires integrated on a silicon chip. TASE provides high-quality III–V nanostructures for monolithic integration on Si with low defect densities and surface roughness and allows very good control of the position, orientation and dimensions of NWs. In the next months our research will focus on the following points:

- First of all we will carry on magneto-transports experiment to calculate the effective g-factor of the nanowires. Spin-orbit interaction in semiconductors does not only affect valence bands, but also influences the splitting of the conduction band in the presence of an external magnetic field B [27]. As a consequence of the spin-orbit interaction, the Zeeman energy splitting $\Delta E = g^* \mu_B B$ (involving electrons with different spin) is proportional to a material specific g-factor which is different from the one of free electrons in vacuum (g = 2). The interplay of Zeeman splitting and spin-orbit coupling leads non trivial changes in the band structure which we should be able to address.
  The angle of the magnetic field with respect to the substrate will be varied to reveal g-factor anisotropies. Having a large effective g-factor is important in system coupled to a superconductor in order to reach the topological regime before reaching the critical field of the superconductor.

- We will characterize more complex nanowires networks with the aim of eventually realize braiding operations with Majorana quasiparticles arising from the coupling to a superconductor. The structure design is ready but the devices have not been tested yet. An idea of what could be possible is shown in Fig.4.1.

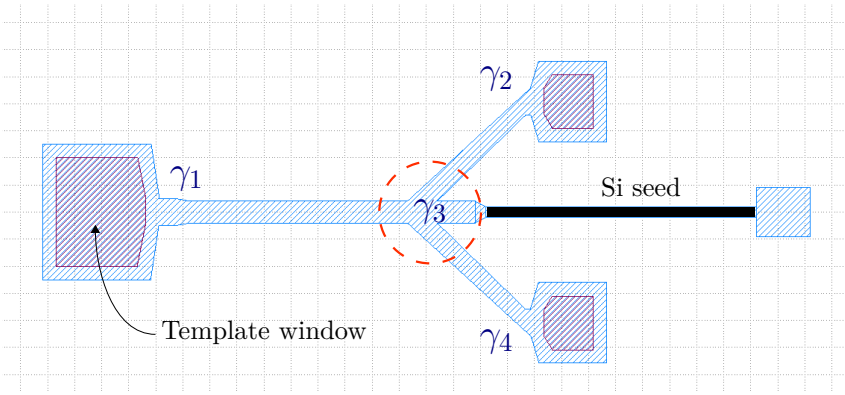

Figure 4.1: Layout of a cross junction of three wires aimed to realize braiding of Majorana quasiparticles. γ_i are MZMs creation operators. The coupling between the wires might be controlled using a proper set of sidegates, whose positions are still to be discussed.

III-V precursors should be able to enter the widows opened in the SiO_2 and fill the entire cross junction. Exchanging of MZM can then be obtained by tuning the coupling among the different arms of the structure via gate voltages.

- Obviously we should be able to find a suitable superconductor coupled to the nanowires. This is not easy but research is going on and possible ideas already came out. One should find a superconductor which is lattice matched with the nanowire (so as to realize an epitaxial interface and to proximitize properly the semiconductor), and which will also withstand the process temperature.

For more than 50 years, the traditional approach to increase the performance of integrated circuits made from CMOS has been to scale down dimensions so as to reduce power consumption and increase signal processing speed. To achieve such miniaturization in the face of exponentially increasing fabrication challenges requires many ingenious ideas and billions in investment.
We are rapidly reaching the end of this path, as current system dimensions and occupation reach the de-Broglie wavelength and single electron levels, meaning not only can quantum effects no longer be ignored but in fact begin to dominate. Quantum technologies are probably the answer to this long expected end of the classical path. Their quest is to turn the challenges of hitting this quantum limit into an opportunity, namely, making use of the quantum properties of matter to bring device technology to a superior level of performance, using novel architecture for computing, communication, and sensing applications. There are many attractive proposals for qubits implementation. To exploit topological states of matter is extremely challenging but also extremely interesting.

A

A1: MEASUREMENT SET-UP

A.1 RACK INSTRUMENTS

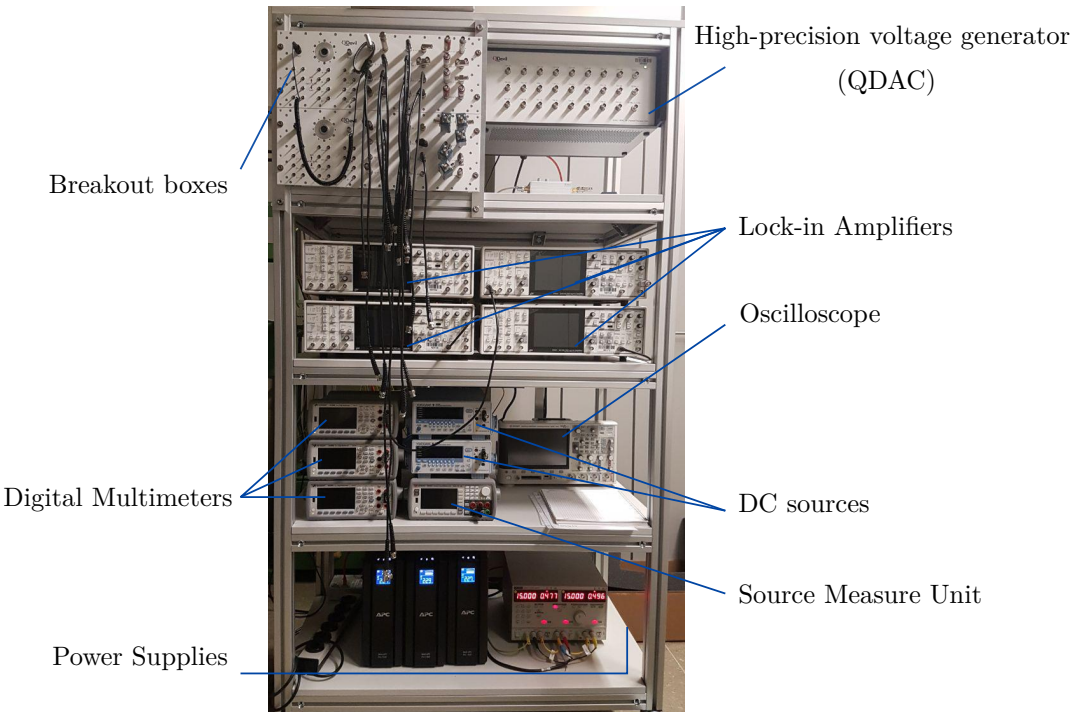

Figure A.1: Summary of all the instrument used for electrical measurements. They were all connected to a computer via ethernet/USB cable and controlled remotely using QCoDeS. The last is an open source Phyton-based data acquisition framework developed by the Copenhagen / Delft / Sydney / Microsoft quantum computing consortium.

A.2 PHYSICAL PROPERTY MEASUREMENT SYSTEM

a) b) c)

Figure A.2: a) DynaCool PPMS used in the present work. It is able to cool down to 1.6 K and is equipped with a b) 12-pin break-out box plus an internal measurement system (not used in the present work). Our group is currently waiting for its own cryostat with cooling capability down to 2 mK, required to bring the system in the topological state of interest. c) Chip carrier and corresponding socket. In the background a ultrasonic-based wire bonder.

A.3 DIP STICK

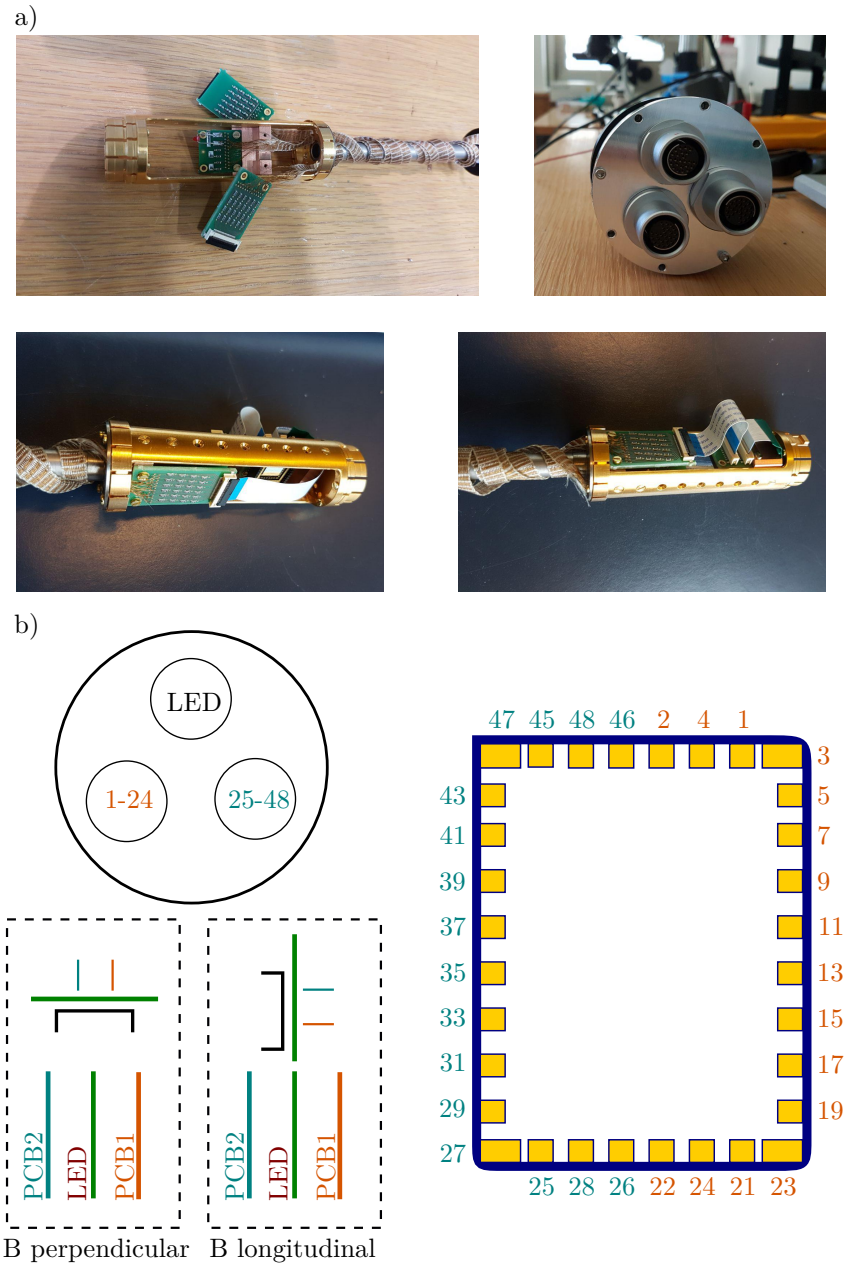

Figure A.3: The PPMS has the limitation that it can control only 12 pins on a chip. This basically means that maximum two devices with four probes and two sidegates can be measured at each cooldown. a) For this reason we built our own dip stick from where the cryostat ground can be easily extracted from the stick itself. The stick is equipped with 48 lines (24 low noise twisted pairs) for measuring and each line has an RC filter with a cutoff frequency at 20 kHz. One additional PCB was used to host a LED and a thermometer (still missing in the picture). b) We used only 32 lines of the 48 available to make the system compatible with the 32-pin chip carrier. The chip carrier can be mounted either parallel or perpendicular to the direction along which the magnetic field is applied.

LIST OF FIGURES

[1] Dong Liang and Xuan PA Gao. Strong tuning of rashba spin–orbit interaction in single inas nanowires. *Nano letters*, 12(6):3263–3267, 2012.

[2] Peter Krogstrup, Henrik Ingerslev Jørgensen, Martin Heiss, Olivier Demichel, Jeppe V Holm, Martin Aagesen, Jesper Nygard, and Anna Fontcuberta i Morral. Single-nanowire solar cells beyond the shockley–queisser limit. *Nature Photonics*, 7(4):306, 2013.

[3] Esteban Bermúdez-Ureña, Gozde Tutuncuoglu, Javier Cuerda, Cameron L. C. Smith, Jorge Bravo-Abad, Sergey I. Bozhevolnyi, Anna Fontcuberta i Morral, Francisco J. García-Vidal, and Romain Quidant. Plasmonic waveguide-integrated nanowire laser. *Nano Letters*, 17(2):747–754, 2017. PMID: 28045536.

[4] Martin Leijnse and Karsten Flensberg. Introduction to topological superconductivity and majorana fermions. *Semiconductor Science and Technology*, 27(12):124003, 2012.

[5] Tommy Li, William A Coish, Michael Hell, Karsten Flensberg, and Martin Leijnse. Four-majorana qubit with charge readout: Dynamics and decoherence. *Physical Review B*, 98(20):205403, 2018.

[6] Hao Zhang, Chun-Xiao Liu, Sasa Gazibegovic, Di Xu, John A Logan, Guanzhong Wang, Nick Van Loo, Jouri DS Bommer, Michiel WA De Moor, Diana Car, et al. Quantized majorana conductance. *Nature*, 556(7699):74, 2018.

[7] M. T. Björk, A. Fuhrer, A. E. Hansen, M. W. Larsson, L. E. Fröberg, and L. Samuelson. Tunable effective g factor in inas nanowire quantum dots. *Phys. Rev. B*, 72:201307, Nov 2005.

[8] Martin Leijnse and Karsten Flensberg. Introduction to topological superconductivity and majorana fermions. *Semiconductor Science and Technology*, 27(12):124003, 2012.

[9] H. Schmid, M. Borg, K. Moselund, L. Gignac, C. M. Breslin, J. Bruley, D. Cutaia, and H. Riel. Template-assisted selective epitaxy of iii–v nanoscale devices for co-planar heterogeneous integration with si. *Applied Physics Letters*, 106(23):233101, 2015.

[10] Morten Kjærgaard, F Nichele, Henri Juhani Suominen, MP Nowak, M Wimmer, AR Akhmerov, JA Folk, Karsten Flensberg, J Shabani, w CJ Palmstrøm, et al. Quantized conductance doubling and hard gap in a two-dimensional semiconductor–superconductor heterostructure. *Nature communications*, 7:12841, 2016.

[11] T Hyart, B Van Heck, IC Fulga, M Burrello, AR Akhmerov, and CWJ Beenakker. Flux-controlled quantum computation with majorana fermions. *Physical Review B*, 88(3):035121, 2013.

[12] Ramón Aguado. Majorana quasiparticles in condensed matter. *arXiv preprint arXiv:1711.00011*, 2017.

[13] Fabrizio Nichele. *Transport experiments in two-dimensional systems with strong spin-orbit interaction*. PhD thesis, ETH Zurich, 2014.

[14] Anindya Das, Yuval Ronen, Yonatan Most, Yuval Oreg, Moty Heiblum, and Hadas Shtrikman. Zero-bias peaks and splitting in an al–inas nanowire topological superconductor as a signature of majorana fermions. *Nature Physics*, 8(12):887, 2012.

[15] Önder Gül, Hao Zhang, Jouri DS Bommer, Michiel WA de Moor, Diana Car, Sébastien R Plissard, Erik PAM Bakkers, Attila Geresdi, Kenji Watanabe, Takashi Taniguchi, et al. Ballistic majorana nanowire devices. *Nature nanotechnology*, 13(3):192, 2018.

[16] Sasa Gazibegovic, Diana Car, Hao Zhang, Stijn C Balk, John A Logan, Michiel WA de Moor, Maja C Cassidy, Rudi Schmits, Di Xu, Guanzhong Wang, et al. Epitaxy of advanced nanowire quantum devices. *Nature*, 548(7668):434, 2017.

[17] S Vaitiekėnas, AM Whiticar, M-T Deng, F Krizek, JE Sestoft, CJ Palmstrøm, S Marti-Sanchez, J Arbiol, P Krogstrup, L Casparis, et al. Selective-area-grown semiconductor-superconductor hybrids: A basis for topological networks. *Physical review letters*, 121(14):147701, 2018.

[18] Henri J Suominen, Morten Kjaergaard, Alexander R Hamilton, Javad Shabani, Chris J Palmstrøm, Charles M Marcus, and Fabrizio Nichele. Zero-energy modes from coalescing andreev states in a two-dimensional semiconductor-superconductor hybrid platform. *Physical review letters*, 119(17):176805, 2017.

[19] Mattias Borg, Heinz Schmid, Kirsten E. Moselund, Giorgio Signorello, Lynne Gignac, John Bruley, Chris Breslin, Pratyush Das Kanungo, Peter Werner, and Heike Riel. Vertical iii–v nanowire device integration on si(100). *Nano Letters*, 14(4):1914–1920, 2014. PMID: 24628529.

[20] RB Marcus and TT Sheng. The oxidation of shaped silicon surfaces. *Journal of the electrochemical society*, 129(6):1278–1282, 1982.

[21] Y-H Kim, YS Chaug, NJ Chou, and J Kim. Adhesion of titanium thin film to oxide substrates. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 5(5):2890–2893, 1987.

[22] LJ Brillson, ML Slade, HW Richter, H VanderPlas, and RT Fulks. Titanium–silicon and silicon dioxide reactions controlled by low temperature rapid thermal annealing. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 4(3):993–997, 1986.

[23] Lei Jin. Preparation and properties of tantalum silicide films on silicon substrates. 2000.

[24] V. N. Bessolov, Yu. V. Zhilyaev, E. V. Konenkova, and M. V. Lebedev. Sulfide passivation of iii-v semiconductor surfaces: role of the sulfur ionic charge and of the reaction potential of the solution. *Technical Physics*, 43(8):983–985, Aug 1998.

[25] Roman M. Lutchyn, Tudor D. Stanescu, and S. Das Sarma. Search for majorana fermions in multiband semiconducting nanowires. *Phys. Rev. Lett.*, 106:127001, Mar 2011.

[26] Vanessa Schaller. Ballistic one-dimensional transport in inas nanowires integrated on silicon. 2016.

[27] T. Ihn. *Semiconductor Nanostructures: Quantum States and Electronic Transport*. OUP Oxford, 2010.