POLITECNICO DI TORINO

College of Engineering

Master Degree Course in Biomedical Engineering

MASTER DEGREE THESIS

BODY DUST
Feasibility study on signal transmission for sub-100µm-size active wireless biosensors

Supervisors:
Prof. Danilo DEMARCHI
Prof. Sandro CARRARA

Candidate:
Gian Luca BARBRUNI

July, 2019

ACKNOWLEDGMENTS

Ed ecco arrivati al termine di un altro importante traguardo della mia vita.
Tanti pensieri, tante ansie, troppe emozioni… difficile per me esprimere quello che sto provando!

"Pensare è facile, agire è difficile e mettere i propri pensieri in pratica è la cosa più difficile del mondo." – Goethe –

Con immensa stima e riconoscenza desidero ringraziare i miei due relatori: Danilo Demarchi, per la sua passione e per il suo aiuto nella stesura di questo elaborato e Sandro Carrara, mia guida all'EPFL di Losanna, per la sua grande professionalità, per i suoi importantissimi consigli e per il suo "amichevole" supporto nella conclusione di questo impegnativo progetto.

Ringrazio ancora il Professor Danilo Demarchi per avermi dato l'opportunità di collaborare con l'Ing. Vladimir Stavrov, direttore di AMG Technologies in Bulgaria, con il quale ho portato a termine il mio primo studio di fattibilità su un reale progetto industriale in collaborazione con MECA.

A sincere thanks to Professor Catherine Dehollain, Professor at EPFL in Lausanne, helpful and extremely competent teacher who has been able to take away any doubts helping me with useful discussions in this challenging project.

Ringrazio enormemente e con massima stima la precisione, l'autorevolezza e la saggezza del Professor Marco Knaflitz, gli importanti consigli sul piano di studio finale della Professoressa Gabriella Balestra e il forte metodo d'insegnamento del Professor Filippo Molinari.

Ricordo e ringrazio ancora il Professor Morbiducci, la Professoressa Bignardi, il Professor Paolo Motto Ros, Simone Aiassa, tutti i docenti, la biblioteca, la segreteria e tutti coloro che hanno contribuito a rendere il mio percorso interessante e stimolante.

Ci tengo moltissimo a ringraziare con tutto il cuore il Prof. Nuvoloni, il Prof. Damiano e il Prof. Villa, miei insegnanti del liceo, grandi persone che hanno sempre creduto in me e incoraggiato il mio lato migliore.

Ringrazio Chiara, Mattia, Alessandro e tutti i colleghi che hanno vissuto con me le infinite ore in laboratorio, lo stress degli esami e gli interminabili progetti.
Ringrazio ancora i colleghi "svizzeri" dell'EPFL, Luca ed Emile, con i quali ho lavorato con grande impegno, professionalità e passione.
Ringrazio tutti i miei amici, Simone, Desiree, Bobo, Francesca, Lotti e Debora.
Un grande grazie a Ste che mi ha aiutato nei momenti di sconforto facendomi sempre sorridere, preoccupandosi per me e credendo sempre nelle mie capacità.

Spiritualmente ed umanamente devo molto a Sua Ecc. Mons. Alberto Maria Careggio, vescovo emerito e a Mons. Andrea Francia che hanno sempre accompagnato la mia crescita nella preghiera.

Ringrazio la filosofia del Judo, il mio primo Maestro De Maria, il carismatico Maestro Berghi, il grande Maestro Pawlowskij e il fortissimo Maestro Piero che mi hanno insegnato a superare le difficoltà della vita "con sorriso" senza arrendersi mai, a piegarsi senza spezzarsi, a cadere una volta ed essere sempre pronti a rialzarsi.

Tutto questo non sarebbe comunque stato possibile se al mio fianco non ci fosse sempre stata la mia splendida famiglia che non bene e nel male ha sempre lottato con me, gioendo e soffrendo giorno dopo giorno: il nonno Carlo, che ha passato tutta la sua vita nel forno creando la focaccia più buona di Sanremo, la "mitica focaccia Barbruni"; la nonna Rosa, la zia Sandra, lo zio Lele e i miei cugini Filippo e Nicola. Un grazie particolare ai miei nonni, Dado e Liliana, che mi guardano dal cielo e che mi guarderanno soprattutto adesso perchè "[…] la morte non è niente […]" – Sant'Agostino –

In ultimo desidero esprimere il ringraziamento più importante ai miei genitori.
Mio papà Gian Carlo, che lavorando notte e giorno, mi ha sempre insegnato i veri valori del sacrificio, della tenacia e della libertà, un uomo di poche parole e quelle poche, anche male organizzate, ma un uomo di tanti fatti e di sinceri e concreti esempi, un uomo forte, tenace e sempre pronto a combattere per il giusto e per il bene della famiglia.
Mia mamma Ale, che con tanta dedizione e impegno mi ha sempre incoraggiato a dare il massimo rispettando gli altri, avendo cura di me stesso e ringraziando la vita per ciò che mi ha offerto. Una donna straordinaria dai saldi principi, una moglie attenta e sempre presente, una mamma gentile, precisa, amorevole e sempre in prima linea per aiutare e consigliare le mie scelte. Con estremo rispetto e stima, posso solo che ringraziare mamma e papà per quello che oggi sono diventato.

E infine ringrazio me stesso, per la determinazione e l'impegno attui a raggiungere il mio obiettivo, la voglia di sfidarmi, la voglia di tentare, il desiderio di arrivare e soprattutto per averci sempre provato ed esserci sempre riuscito.

"Supera te stesso e supererai il mondo" – Sant'Agostino –

Che la forza sia sempre con me… ed anche la massa, l'accelerazione, l'attrito… Buona vita!

CONTENTS

LIST OF FIGURES

<u>*Chapter 5*</u>

LIST OF TABLES

LIST OF EQUATIONS

Chapter 2

(2.1) $$f = \frac{I}{N*C_{tot}*V_{dd}}$$

Chapter 3

(3.1) $$Z_{ref} = \frac{\omega^2 k^2 L_{s1} L_{s2}}{R_{s2}+j\omega L_{s2}+\frac{R_{load}}{1+j\omega C_{res2} R_{load}}}$$

(3.2) $$Z_{ref} = \frac{\omega^2 k^2 L_{s1} L_{s2}}{R_{s2}+j\omega L_{s2}-\frac{j}{\omega C_{res2}}}$$

(3.3) $$Z_{ref} = \frac{\omega^2 k^2 L_{s1} L_{s2}}{R_{s2}+j\omega L_{s2}}$$

(3.4) $$S = P_{EIRP} * \frac{1}{4\pi d^2}$$

(3.5) $$P_{EIRP} = P_t G_t$$

(3.6) $$P_{AV} = A_E S$$

(3.7) $$A_E = G_r * \frac{\lambda^2}{4\pi}$$

(3.8) $$\Gamma = \frac{R_i - R_{ANT}}{R_i + R_{ANT}}$$

Chapter 4

(4.1) $$\frac{\beta_n}{2}(V_{SP} - V_{THn})^2 = \frac{\beta_p}{2}(V_{DD} - V_{SP} - V_{THp})^2$$

(4.2) $$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} V_{THn} + (V_{DD} - V_{THp})}{1+\sqrt{\frac{\beta_n}{\beta_p}}}$$

(4.3) $$\beta_n = KP_n \frac{W_0}{L_0}$$

(4.4) $$\beta_p = KP_p \frac{W_1}{L_1}$$

(4.5) $$C_{in} = \frac{3}{2}(C_{ox1} + C_{ox2})$$

(4.6) $C_{out} = C_{ox1} + C_{ox2}$

(4.7) $t_{PLH} = 0.7\ R_{p2}\ C_{out}$

(4.8) $t_{PHL} = 0.7\ R_{n1}\ C_{out}$

(4.9) $f = \frac{I}{N * C_{tot} * V_{dd}}$

(4.10) $C_{p_{tot}} = 2 * C_p = 2 * \frac{2}{3} C_{ox} WL$

CHAPTER 1

INTRODUCTION

This thesis takes part of an enormous project that starts in 2017 from the Special Session of the IEEE conference BioCAS. The "Body Dust" idea was initiated by Prof. Sandro Carrara, senior scientist at the EPFL in Lausanne and Prof. Georgiou Pantelis from the Imperial College of London. Early Prof. Danilo Demarchi from the DET department of Politecnico di Torino was involved and the first working groups were instituted. I just want to specify that actually this project did not receive any financial support from the international scientific community.

"Body Dust" is a very challenging project that is at its early stages of life. It is a futuristic idea that could potentially complete revolutionize the diagnostic concept as the doctors define it nowadays. Today the routine exams, the more advanced systems to prevent and to perform diagnostics in health diseases at their beginning stage, investigate the human body tissues starting from the external environment… just think to MRI, PET or TC that are commonly used to observe anomalies on tissues or to well recognize cancer. More sophisticated systems start from in vitro analysis of blood: by measuring the concentration of some molecules, protein in blood is possible to make decision for the healthy or unhealthy state of the patient.

Imagine having the possibility to do exactly the same things but through microparticles that navigate into the human body from the internal space, routing to every organ, every tissue but not only: routing to every cell!

Imagine having millions or billions of systems, conceptually in the order of magnitude of a red blood cell that could be simple drink by the patient… It is like drinking a cocktail, a doped cocktail.

All of these particles flow into the human body continuously monitor the patient parameters in real time, in vivo! Through an external detector is possible to ask the dusts the concentration of the molecules that they are measuring and is so possible to observe the evolution of the cancer, the effect of the therapy or the remaining cell after a surgical removal.

This is the first project that could make life to the will note "drinkable electronic": obviously these dusts are not chemical molecules but are thought as real chips, integrated circuits (ICs) battery less involved into a biocompatible packaging. In particular the first important thing to analyze is the possibility to use a material that could cover the IC in order to make it biocompatible and again biodegradable.

Is important that these dusts could enter in some metabolic pathway in order to expel them. If the size of these dusts might approximately be equal to the red blood cell is known that they could be simply expelled through human metabolism.

So, at the present stage, the aim of this project is to investigate the feasibility to develop a fully drinkable and autonomous bio-electronic CMOS sensor in the form of dust particles, capable to identify the source of the disease (tumor mass in particular) and capable to send diagnostic information wirelessly outside the body.

CHAPTER 2

BODY DUST RESEARCH

As I said during the introduction, the aim of the "Body Dust" research is to investigate the feasibility of a future development of new diagnostic systems in the form of "Body Dust" that first of all need to be small enough to support free circulation in human tissue, which requires a total size of less than 10 μm^3, in order to mimic the typical sizes of a blood cell (remember that red blood cells have around 7 µm diameter). This requirement in terms of size is currently unfeasible observing the present state-of-the-art in CMOS technology.
The core idea is the design of a fully packaged CMOS cube, as illustrated in Fig 2.1, which integrates all the IC ever built.

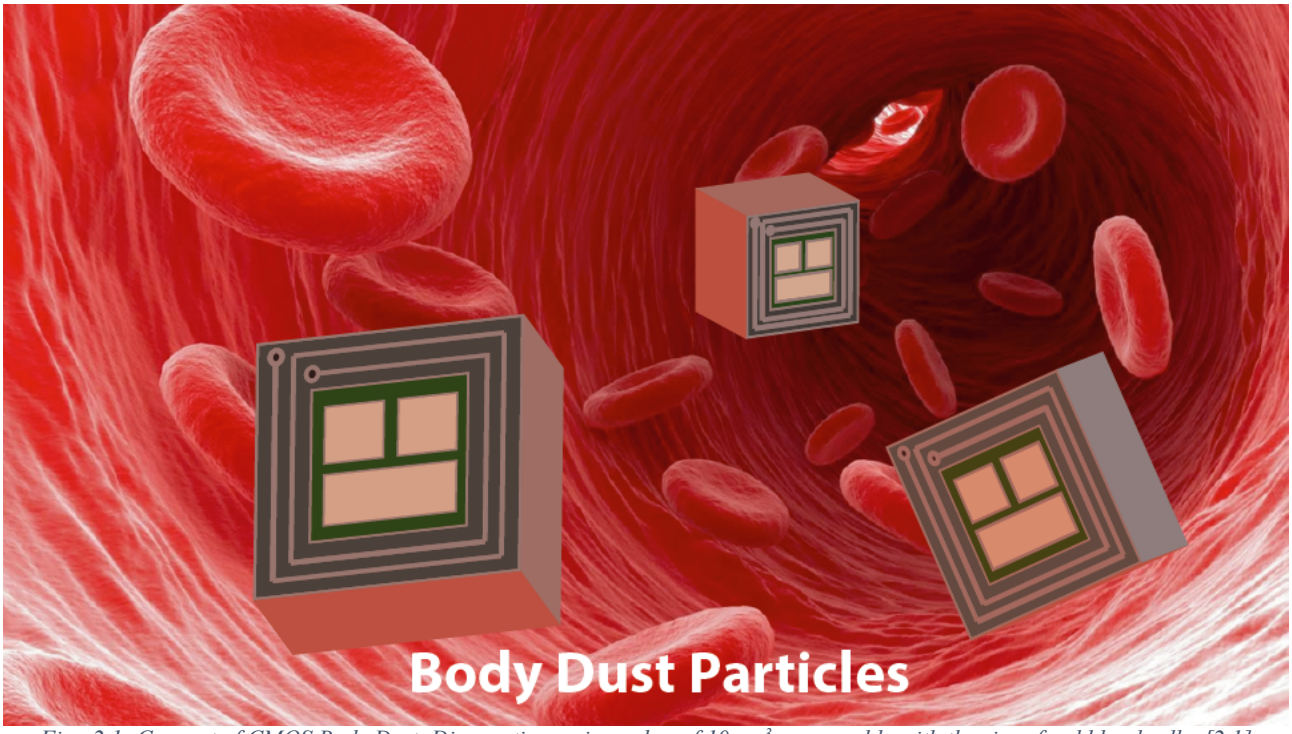


Fig. 2.1: Concept of CMOS Body Dust. Diagnostic sensing cubes of 10 μm^3 comparable with the size of red blood cells. [2.1]

This CMOS cube has to be capable of providing diagnostic through sensing of specific molecules, data-telemetry, low-power consumption and biocompatibility.
In 2012 compact CMOS circuits for glucose sensing have been realized at a size of 0.36 mm^2 [2.2] and the design could be simplified for "Body Dust" application. Micro-coils with 50 µm of lateral size have been published in 2016 [2.3] to provide power in implantable micro-stimulators. Biosensors with working electrodes radii of almost 2.5 µm have been published in 2014 [2.4] and successfully tested for glucose detection and in 2016 a biocompatible packaging in epoxy-resin to protect telemetric diagnostic devices [2.5] have been discovered.
Considering the described researches, the first prototype of the CMOS Body Dust cube is presented in the following Fig. 2.2 and in the following section the main issues related to this new design will be presented.

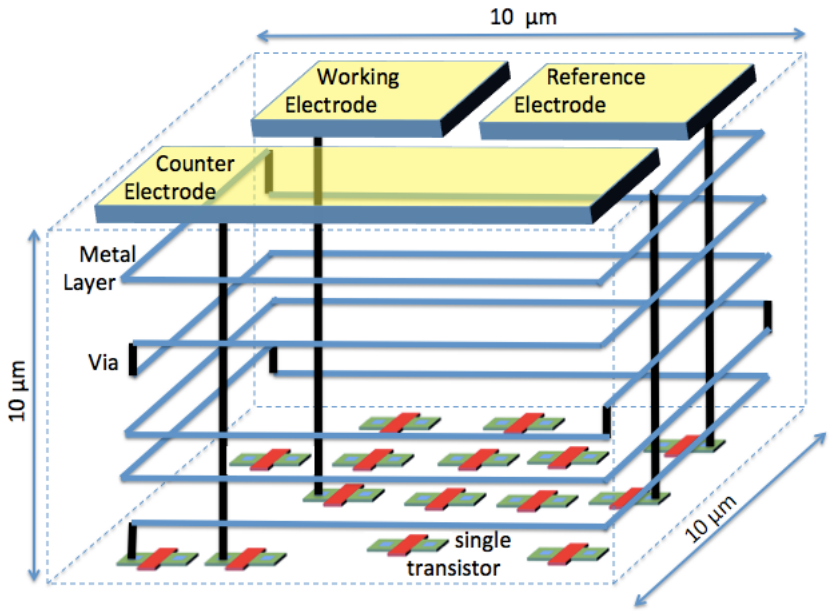


Fig. 2.2: First prototype of the CMOS Body Dust cube [2.1].

2.1 STATE-OF-THE-ART

During this paragraph I want to introduce the state-of-the-art about the main issues related to this new project design: integrated potentiostat, powering systems, nano-biosensors on chip and packaging.

2.1.1 STATE-OF-THE-ART: POTENTIOSTATS

The most common approach for biosensing application is the amperometric method: a redox reaction normally generates electric current that is proportional to the concentration of the target biomolecule. As is shown in Fig. 2.3, in general a circuit, called potentiostat, is required to apply a voltage to the reference electrode (RE) with the aim to generate a cell current measured through a working electrode (WE).

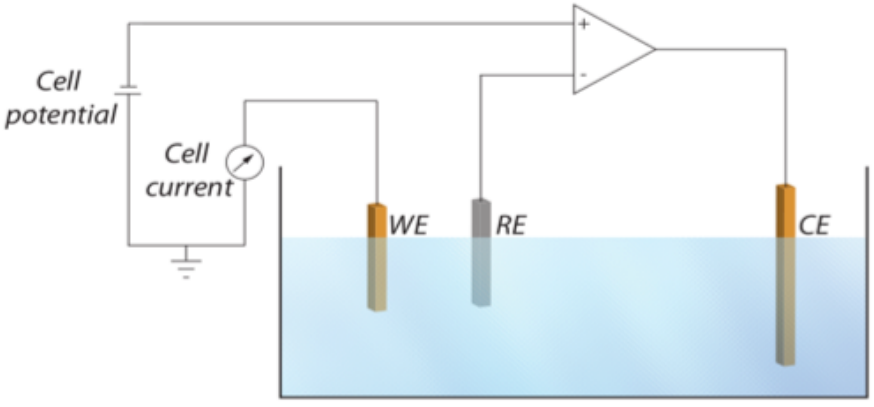


Fig. 2.3: Three-electrode electrochemical cell with potentiostat (reprinted from [2.1]).

In order to read the measured current some instruments are typically required:

- Transimpedance amplifier (TIA) to convert the measured current into a voltage.
- Analogue to digital converter (ADC) in order to sample the received voltage preparing it for the data transmission.

In order to achieve to implantable applications, except the low-power consumption, there are some others important parameters that need to be taken into consideration: input resolution and dynamic range, which defines the range of current that can be measured as the smallest one. A summary of the state-of-the-art performances of fully-integrated potentiostats found in literature is presented in the following Table 2.1.

Method	Input resolution - Max input (Dynamic range, dB)	Power (µW)	Digital output	Reference
Resistive TIA	22 pA - 1 µA (93)	90	No	[2.6]
Sigma-delta	100 fA - 0.5 µA (140)	3,4	Yes	[2.7]
Switch-Capacitor OpAmp integrator	60 pA - 10 µA (124)	3000	No	[2.8]
Current-mode	8.6 pA - 350 nA (92)	4	No	[2.9]

Table 2.1: Performance of some fully-integrated potentiostats (reprinted from [2.1]).

As the table presents, the TIA is the simplest circuit with a good input current resolution while the circuits in the sigma-delta modulator have the better resolution without the need to changing the gain.

2.1.2 STATE-OF-THE-ART: MICRO COILS

Micro-coils are generally fabricated in two different versions:

- Copper trace (10 µm wide and 2 µm thick) directly fabricated on a substrate and then passivated with $Si0_2$.
- Bending an ultra-fine wire of copper with less than 50 µm in diameter.

In 2016 [2.3] the realized coils have a profile of 50x100 μm^2 with a length of 2000 µm and support power levels around 0.5 mW, well enough for powering quite complex CMOS full-systems for multiplexed detection of human metabolism.

2.1.3 STATE-OF-THE-ART: NANO-BIOSENSORS

Antibodies and aptamers are largely used for detecting cancer biomarkers, such surfaces with highly dense bundles of CNT (Carbon NanoTubes) are extremely powerful in terms of sensing performances for both enzyme-mediation and direct detection of human metabolites. In the last years several approaches have been adopted in order to incorporate CNT onto the sensing electrodes like CVD (Chemical Vapor Deposition) growth [2.10], electrochemical deposition [2.11] or micro-spotting [2.12]. The following Fig. 2.4 presents an example of how the CNT can move the sensitivity into the right pharmacological range of concentration of CP (cyclophosphamide), well known cancer chemotherapy compound.

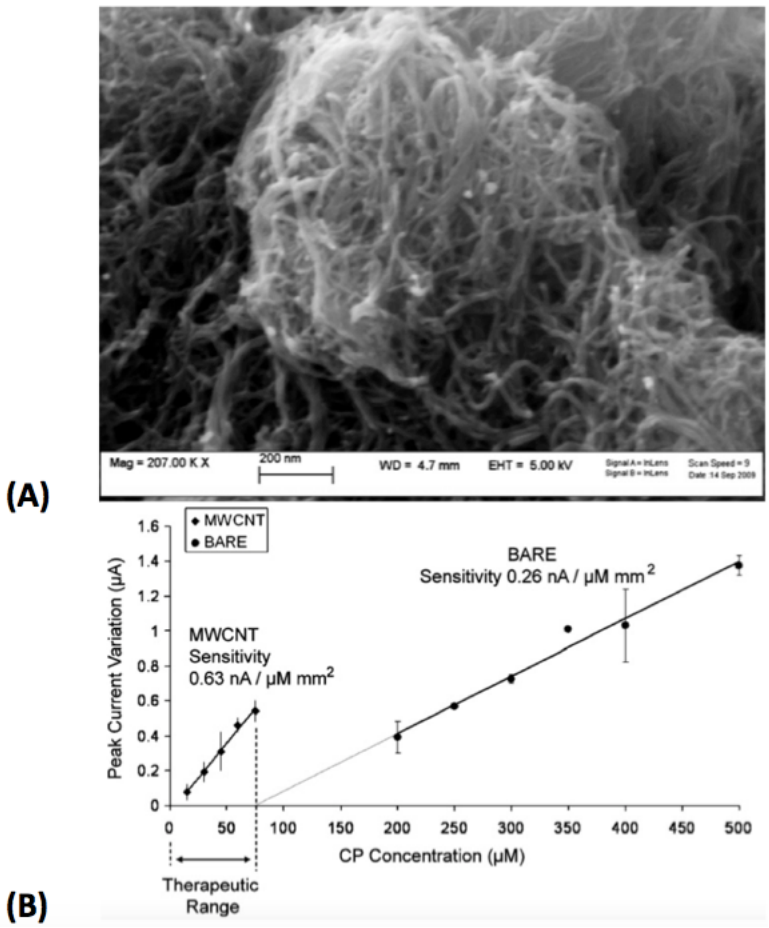


Fig. 2.4: Multi-walled CNT on sensing electrodes (A) and detection of chemotherapy compound with or without MWCNT (B) [2.1].

With the electrochemical deposition, in [2.13] they have successfully obtained sensors with high-performance by also transferring nano-Pt structures by reaching a maximum sensitivity of 51.6 µA/(mM cm^2) in order to detect not only glucose or potassium but also several other endogenous and exogenous molecules as related to human metabolism.
In order to realize small biochips for portable, wearable, implantable or injectable electronic for human health continuous monitoring, the designed IC needs to directly integrate nanostructured biosensors to provide high performance on real human samples. Another time using MWCNT is possible to monitor several human molecules by integrating proper proteins or enzymes.

2.1.4 STATE-OF-THE-ART: PACKAGING

Biocompatible packaging is one of the most important things to do for implantable or injectable electronics because hosting body needs to be protected by inflammatory reactions. Fully sealed packaging has been proposed in biocompatible silicone [2.14], semi-permeable membranes for sensing aims by using polycarbonate [2.15] or epoxy-resin [2.16]. The biocompatibility of the obtained membranes has already been tested with experiments on mice and published in [2.5].

2.2 PROPOSED ARCHITECTURE

The first complete system architecture for "Body Dust" system on chip is proposed in the following Fig. 2.5.

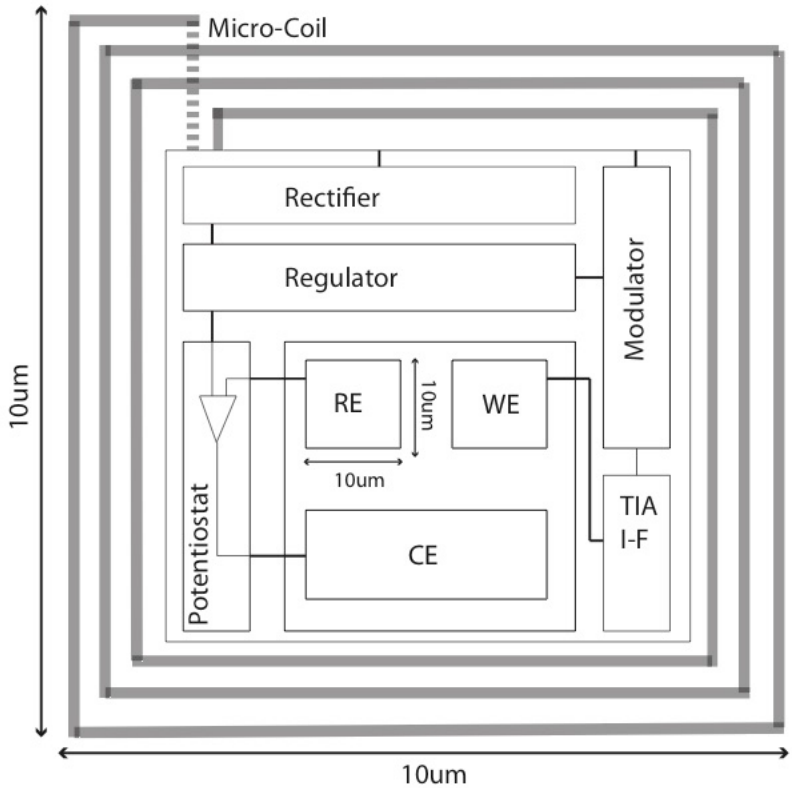


Fig. 2.5: First "Body Dust" first complete architecture for the sensor frontend [2.1].

In particular it is made up of the following elements:

- A three-electrodes set containing counter (CE), working (WE) and reference (RE) electrodes.
- A transimpedance amplifier (TIA) connected to the working electrode to convert the measured current into a voltage: high gain, low noise, high dynamic range (> 120 dB) from 1 pA to 100 µA are needed.
- A potentiostat to provide a stable bias to the RE need to have a sufficient bandwidth to allow cyclic voltammetry.
- A modulator as a I-to-f converter to convert the sensed current from the TIA to a frequency-modulated signal, which drive the transmission coils through backscattering.
- A power rectifier to extract power and generate a regulated supply from the signal received by the coils.

On the top of such CMOS die, an array of aluminum electrodes is formed in order to realize the proper electrodes, which allows the platinum deposition (Fig. 2.6).

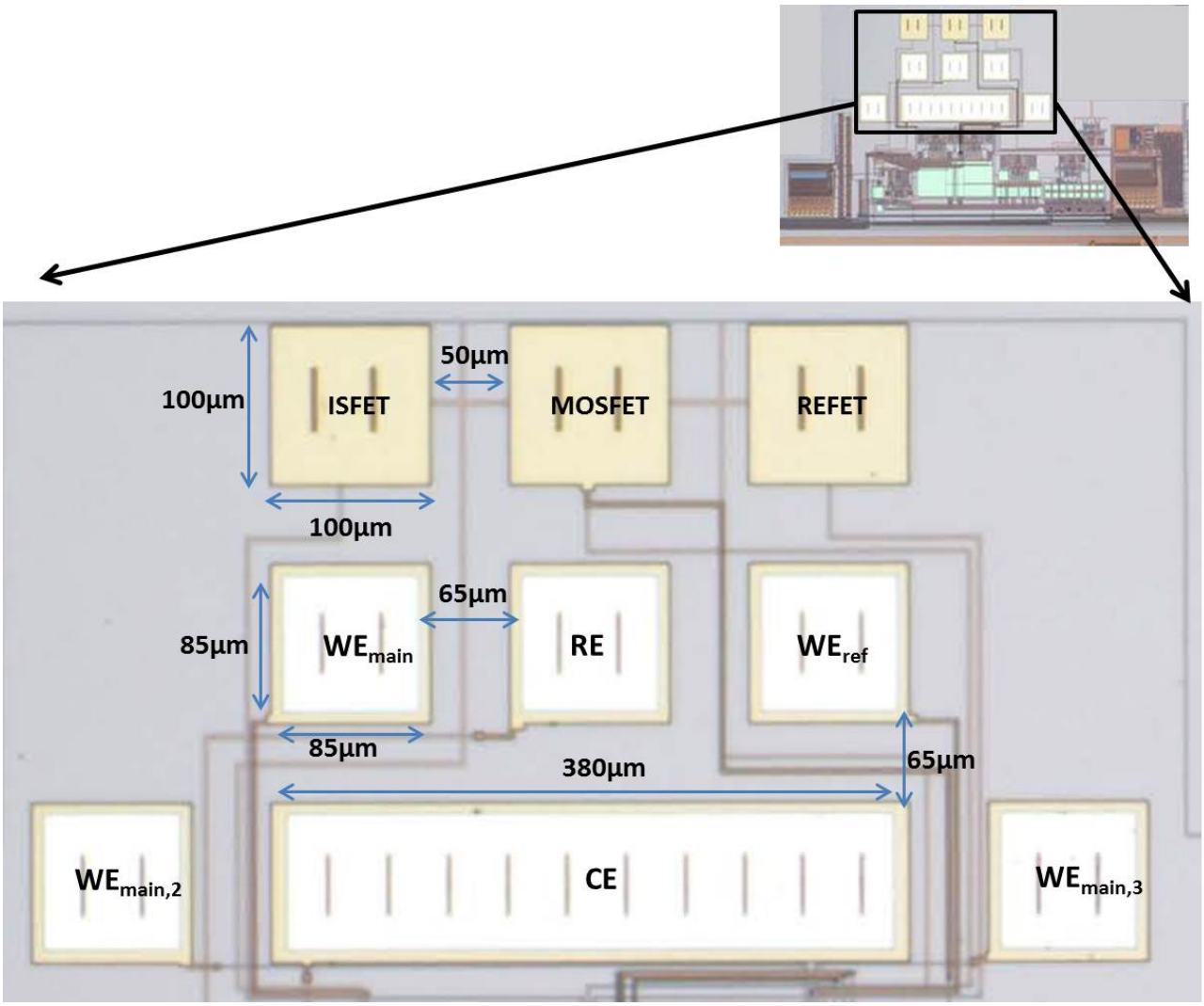


Fig. 2.6: Aluminum electrodes created on the surface of a 0.35 µm CMOS chip [2.1].

These aluminum electrodes are then directly connected to the IC by underneath metal layers to form a complete monolithic solution.
A first design for the CMOS architecture to interface a glucose biosensor has been already proposed by [2.17] containing: an AC-DC rectifier, a band-gap reference, a voltage regulator, a potentiostat, a current to frequency converter, a pulse generator and a back-scattering unit (Fig. 2.7).

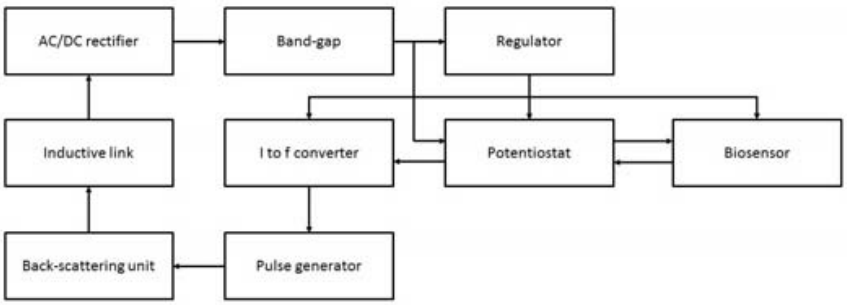


Fig. 2.7: System block diagram [2.17].

In particular the paper asserts that: "[...] the estimated current at the counter electrode ranges from 1 to 5 nA considering a sensor sensitivity of $1.8 * 10^{-7}\ A/mmol * mm$ and glucose concentrations in human blood ranging from 2 to 7 mmol/mm^3.".
The measured current will be addressed to a Voltage Controlled Oscillator (VCO) that modulates its oscillation frequency according to the well note equation:

$$f = \frac{I}{N * C_{tot} * V_{dd}} \tag{2.1}$$

In which N is the number of the stage of the ring, C_{tot} is the overall capacitance over every stage, Vdd is the voltage supply provided to the ring and I is the measured current.
The measured current sensitivity of the designed chip was 7 kHz/nA [2.17].
By a simple product the quasi-digital signal, that need to be processed through the modulation block, has its upper limit near to 35 kHz.
Because of the point of the research I decide to maintain a higher limit in order to be sure that the future modifications on the sensing block could not influence the communication circuit that I design. The upper limit and so the maximum frequency of the considered signal will be so set at 100 kHz.
In order to simplify the concept: the concentration of glucose (or other molecules, if the biosensor is differently functionalized) is measured through the biosensor and the designed potentiostat in a current form (nA). After that the current is converted into a train of pulses and, therefore, is possible to obtain the concentration of the molecule that the signal was representing (glucose concentration, for example).
Of course, once acquired that frequency, the further need of the system is to send out data and, therefore, a further CMOS communication-system is needed (may be in form of further layer in the hypothesis of a 3D CMOS integration), which is the aim of this thesis together with a properly defined communication protocol. Some constraints need to be taken into consideration for the communication: first of all, the upper limit of the measured current and so the upper limit of the incoming frequency (approximately 100kHz). After that is important to choose the proper transmission method: there are several possibilities, using waves in the radio frequency band and so RFID transponders, piezoelectric US system (the one that is chosen), electromagnetic (EM) coupling in the order of GHz or a linking coil. Each of them has pros and cons, but I will discuss about them after in the Chapter 3. In particular the two possible communication methods for this type of application are the backscattering or the load modulation and so, the design ends with the choice of the proper wavelength: Radio-Frequency (RF) or UltraSounds (US) communication. Despite its completely inefficiency through air and bones and its beam-forming I decide to exploit the US solution because of its advantages in terms of available power, link efficiency and safety: observing the next Fig.2.8 is possible to conclude that both for FDA intensity limit and tissue attenuation for biomedical application in general, the US can be used in a very-large-scale applications.

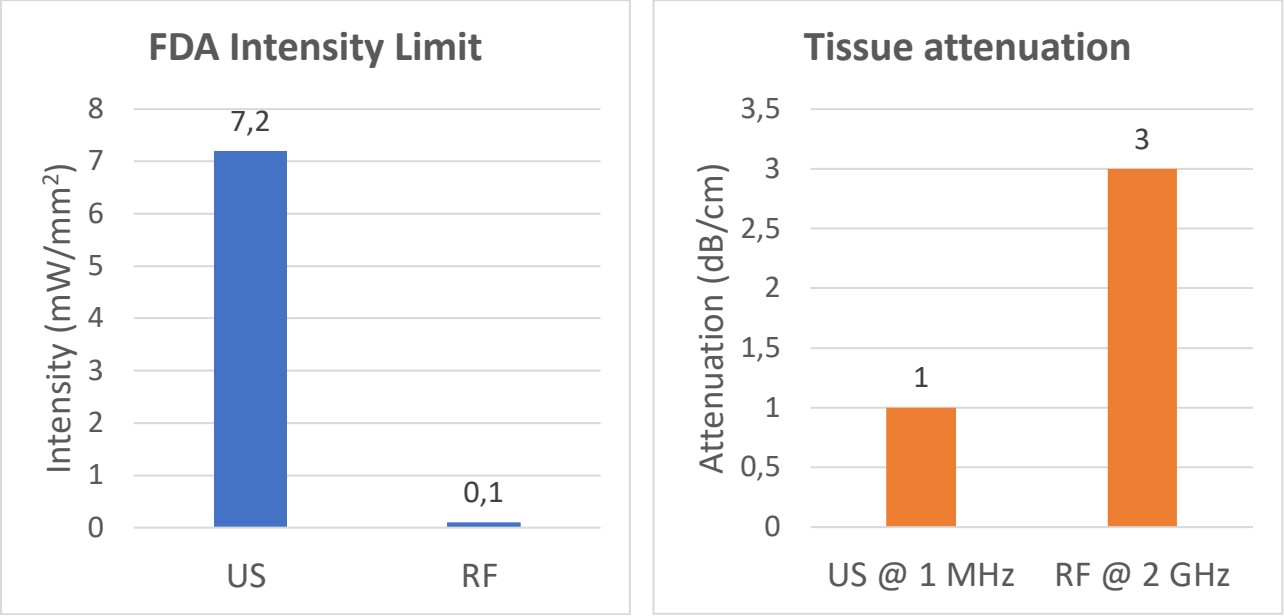


Fig. 2.8: UltraSounds (US) and RadioFrequency (RF) comparison in terms of FDA intensity limit (left) and tissue attenuation (right).

Moreover, a similar approach has been followed by [4.7] in which an US Load Shift Keying (LSK) modulator for deep implanted medical devices has been realized. In this work, the transducer model is taken from [4.7] (also implemented in [4.9]) because of its equal f_0 operating frequency and scalable dimensions for our application. In the Body Dust system, the transponder is so a battery-less system that retrieves the DC power supply by rectifying and regulating the incoming US signal.
So, recapping, from the external stage, the central station, is possible to launch a wave in order to call an interrogator put inside the chip: their properties change accordingly on the measured current and so the reflected wave changes too. It is then possible to calculate the concentration of the molecule that was measured by the sensor placed on the top of the CMOS die.
In particular there are two important constrains: the energy that the complete system requires and the sizes of the full-IC (a target constrain is the physical size of a cell, of a red blood cell). From the engineering standpoint, these two constrains do not necessarily go in the same direction.
Before moving in detail on the discussion about wireless data transmission, I want then to present, in the following Fig. 2.9 and Table 2.2, the actual available data about power consumption and total area of the block that I have presented in the last Fig. 2.7.

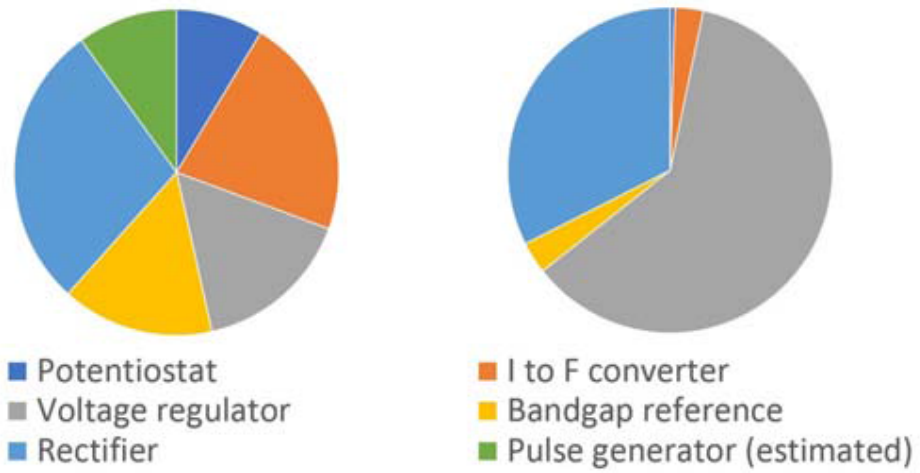


Fig. 2.9: Best case total area (left) and power consumption (right) of each block [2.17].

	Area [μm^2] (best case)	Power [μW]	Power [μW] (best case)	Area [μm^2]
Potentiostat	8.7	0.141	0.124	12
I to f conv.	22	0.836	0.836	22
Rectifier	28.44	9.655	9.655	28.44
Voltage regulator	15.9	18.170	5.7	24
Band-gap ref.	15.2	0.939	0.939	15.2
Pulse generator	10	—	—	10
Total	100.24	29.741	17.254	111.64

Table 2.2: Total area and power consumption of the architecture blocks [2.17].

These results, published in 2017 by [2.17] show that it could be possible to realize a system in a total area of about 10x10 μm^2 that is very close to the real size of a red blood cell. This was the first step towards checking the feasibility of the "Body Dust" concept but now, I will start with the discussion about the feasibility to design a 3D integrated chip.

2.3 3D INTEGRATION

A more sophisticated idea is to make 3D CMOS integration in order to have the third dimension of the cube and so dividing the work into different layers of integration (Fig. 2.10).

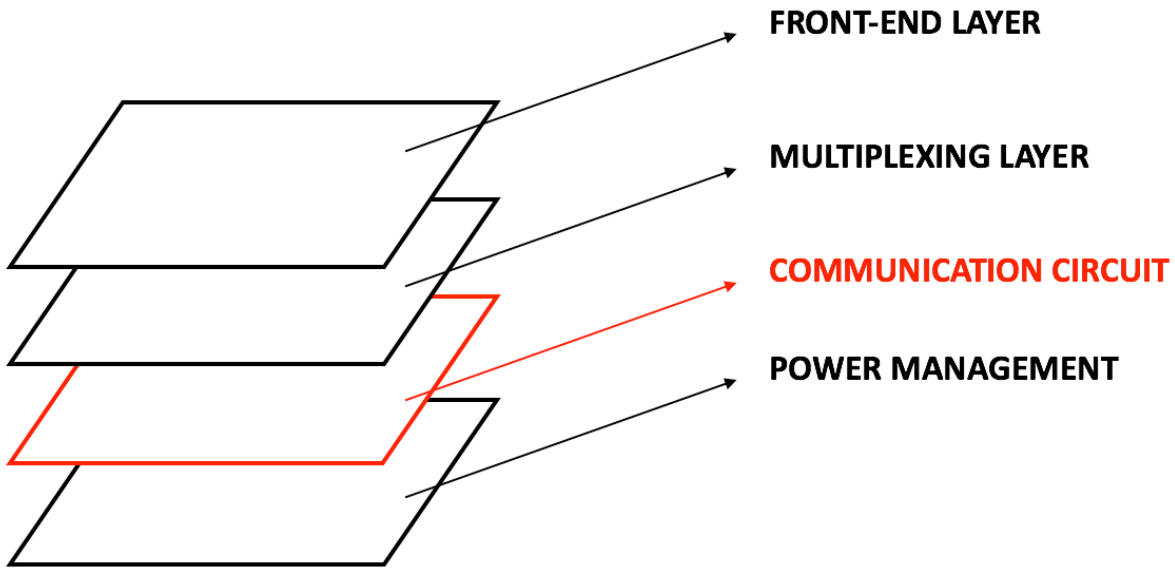


Fig. 2.10: "Body Dust" four layers 3D integration.

Through this method is possible to think about having different biosensors working together in order to detect, from the front-end layer of the same cube, different human metabolites concentrations.

2.3.1 MULTIPLEXING LAYER

A multiplexing layer is needed in order to transmit only one signal at a time. In this layer a word generator (simple counter) is used to discriminate the signal type and the proper muxer is used to collect all the signal as inputs and to transmit them, one by one, to the communication circuit, that will be the third layer of the proposed architecture. The aim is so to treat five different signals that came from five different biosensors mounted on the top metal of the front-end layer to measure respectively glucose, lactate, glutamate and two different drugs concentrations.

2.3.2 POWER MANAGEMENT

The CMOS cube need to be powered in a proper way: in particular, using US wave as input carrier, a piezoelectric material is needed both to receive power and to transmit data. Another element that is needed for sure in this layer is the rectifier to provide the proper DC voltage (considered as 1.8 V in this phase of research) to all the circuit.

CHAPTER 3

WIRELESS DATA TRANSMISSION

The design and realization of implantable, injectable or ingestible devices, are at the boundary between different domains. In particular for what concern the communication: they are at the boundary between the Wireless Body Area Network (WBAN) and the external environment (Fig. 3.1).

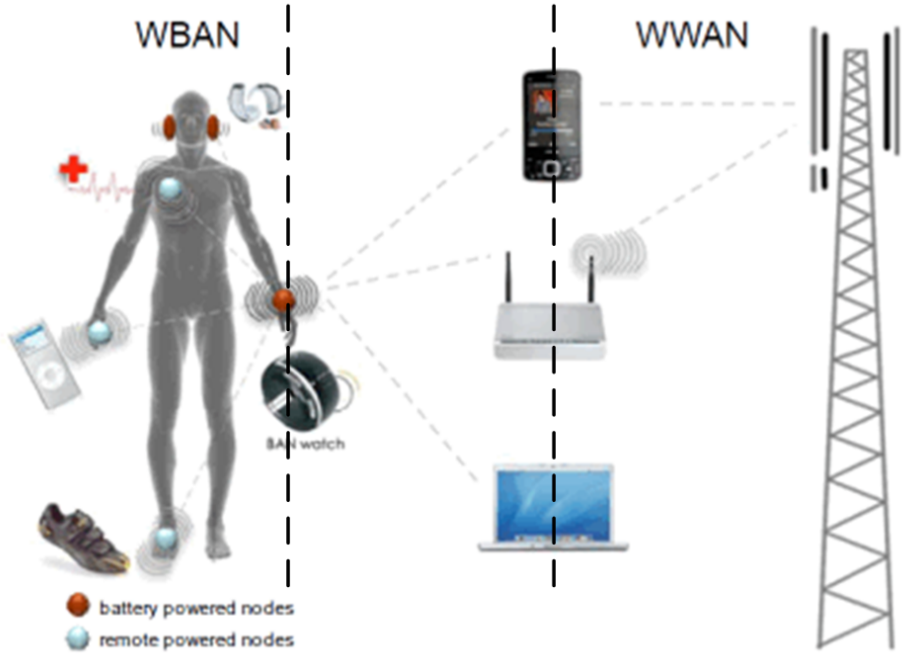


Fig. 3.1: WBAN (Wireless Body Area Network) and WWAN (Wireless Wide Area Network) [3.1].

In particular for wireless communications several aspects need to be taken in consideration:

- Architecture of sensor nodes for short distance communication:
  - Back-scattering or Load modulation (RFIDs).
  - Impulse Radio Ultra-Wideband (IR UWB).
  - Super-regenerative transceivers.
  - Wearable sensor networks.
- Remotely powered wireless circuits: RF by magnetic coupling, EM coupling, electro-acoustic coupling (US).
- Ultra-Low-power wireless communications with specific frequency range for the ICs (MHz to GHz).

One possible communication method is the reflected power, wireless and battery less operation in which the power consumption of the tag is minimize and the aim is the generation of the carrier at the base station by backscattering the incident wave (Fig. 3.2).

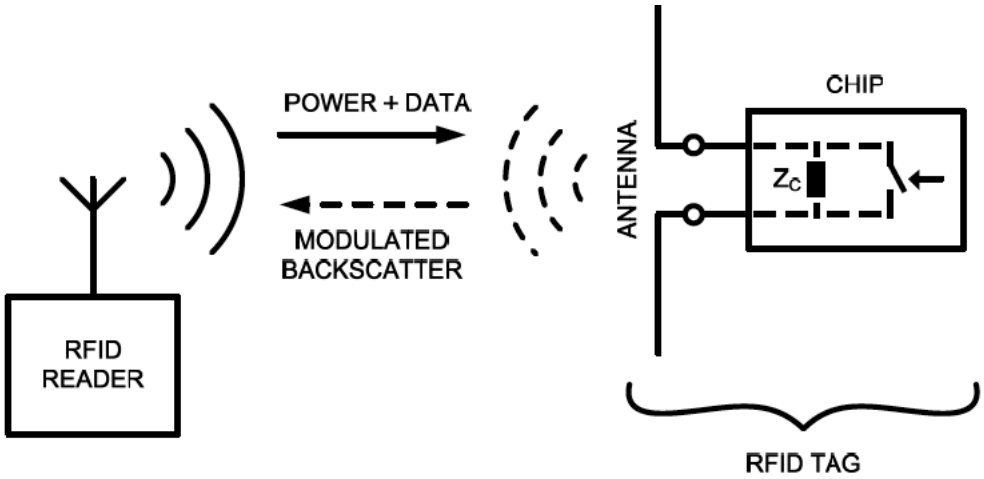


Fig. 3.2: Communication by reflected power [3.2].

In particular for what concern the chip properly, I want to propose here an example of blocks architecture for an Ultra-Low-power RFID tag (Fig. 3.3).

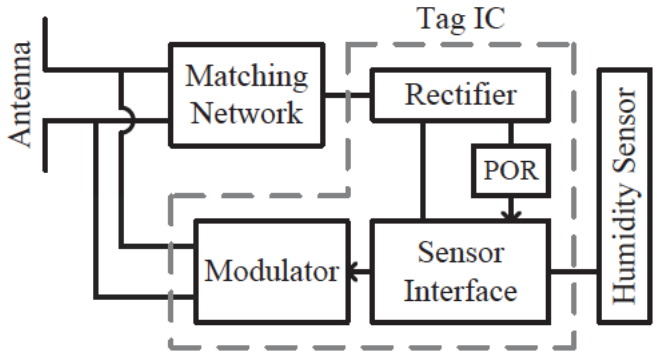


Fig. 3.3: Ultra low-power RFID tag [3.3][3.4].

In the situation described above, the tag is designed for capacitive sensor applications with a printed humidity sensor. The readout is fully digital with particular low voltage supple (down to 0.8V) and Ultra-Low-power consumption (12 µW). The full circuit is realized with the same technology I use (UMC 0.18 µm CMOS) for a wireless data transmission with distance range up to 4 m.
In order to be more exhaustive and general, the next Fig. 3.4 shows a complete and simple schema of the main blocks for remotely-powered sensing chips.

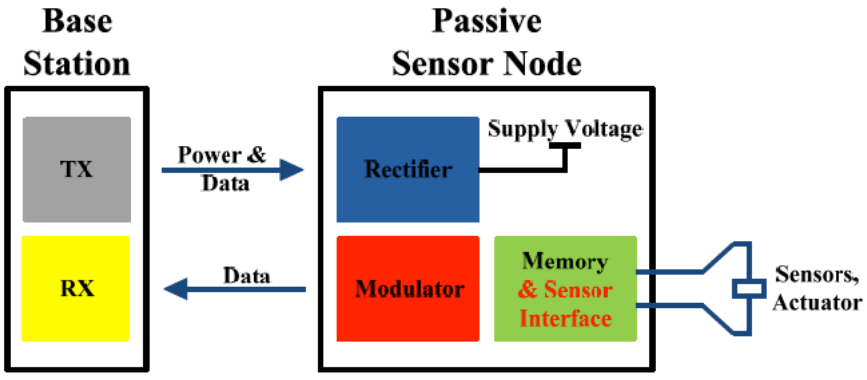


Fig. 3.4: Remotely-powered sensing chip [3.1].

There are two different approaches for data transfer:

1) One single frequency for remote power and data communication: in this case, a simple transmitter in the sensor node provides communication by load modulation or backscattering. The power transfer is interrupt during the data transmission and this situation is always a trade-off between the optimization of the link for power transfer and for data communication (Fig. 3.5).

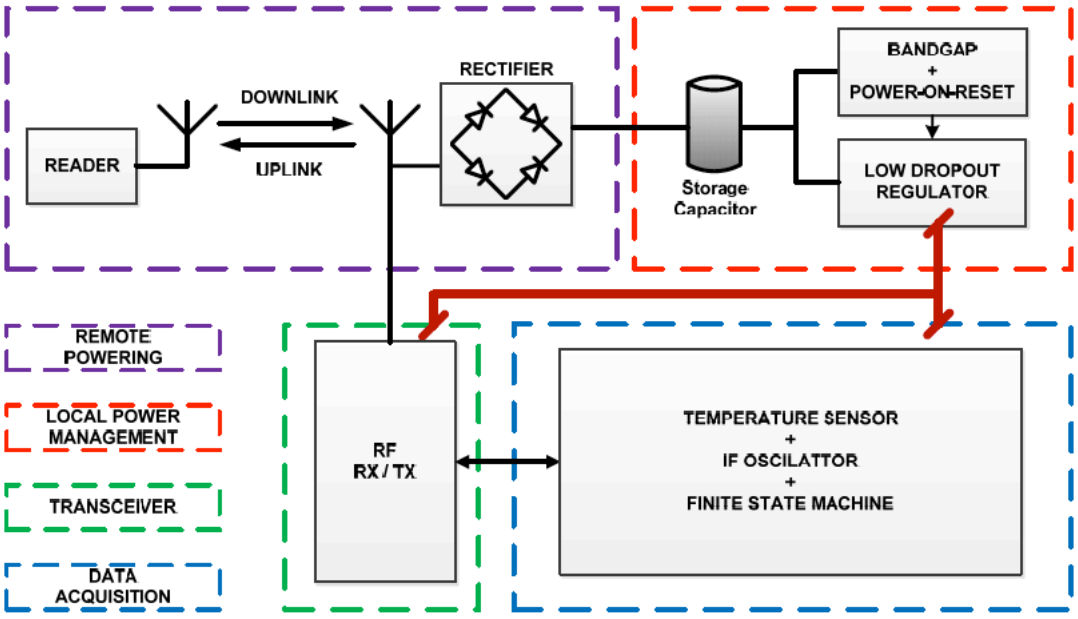


Fig. 3.5: Single frequency approach [3.1].

2) Dual frequency approach: in this case one frequency is used for remote power and another one to provide data communication. With this method, extra power is required due to the active transmitter of the sensor node and an extra antenna is needed for the data communication. On the contrary the power transfer could be independent from the data communication (Fig. 3.6).

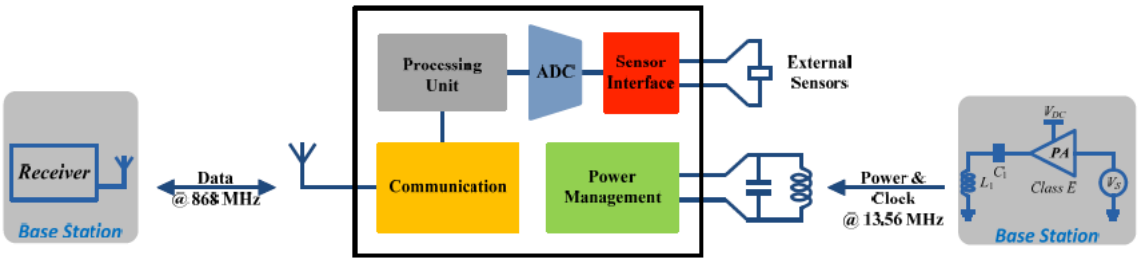


Fig. 3.6: Dual frequency approach [3.1].

3.1 LOAD MODULATION

The basic electrical configuration to implement the load modulation method is the inductive coupling. As it is shown in Fig. 3.7, there are two sides of the entire system: the reader (external node) and the tag (internal chip).

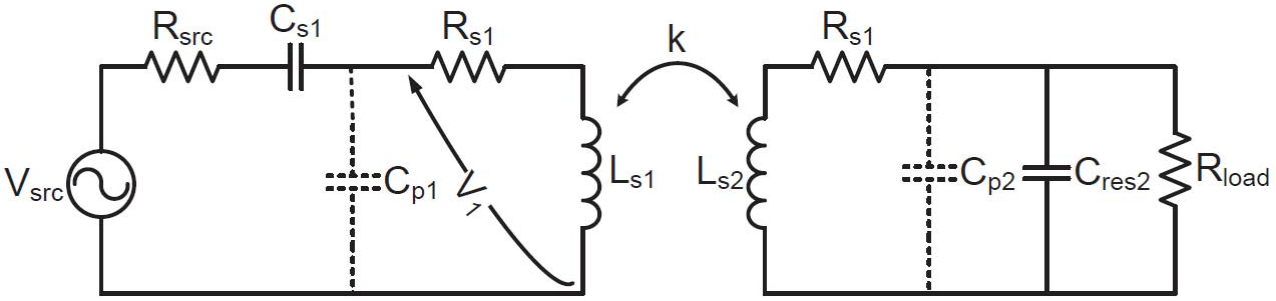


Fig. 3.7: Inductive coupling [3.1].

In the reader side (left): R_{src} and V_{src} are respectively source resistance and voltage, while R_{load} of the tag side (right) is the properly load. L_{s1} and L_{s2} are the inductance of the coils, C_{s1} and C_{res2} are the capacitance to resonate with coils, C_{p1} and C_{p2} are the parasitic capacitance of the coils, R_{s1} and R_{s2} are the resistive losses of coils and k is the coupling coefficient.
On the primary side there is a series resonant circuit while on the secondary side there is a parallel resonant circuit and the inductive link is made by two coils resonant.
Data communication by load modulation is provided by the definition of two states for a binary communication:

- First state corresponds to maximum power transfer (R_{load}).
- Second state is created by modifying the value of the load.

The principle of this binary communication is to use one single switch in series or in parallel with the load to change its value. The position of the switch is controlled by the data signal (Fig. 3.8).

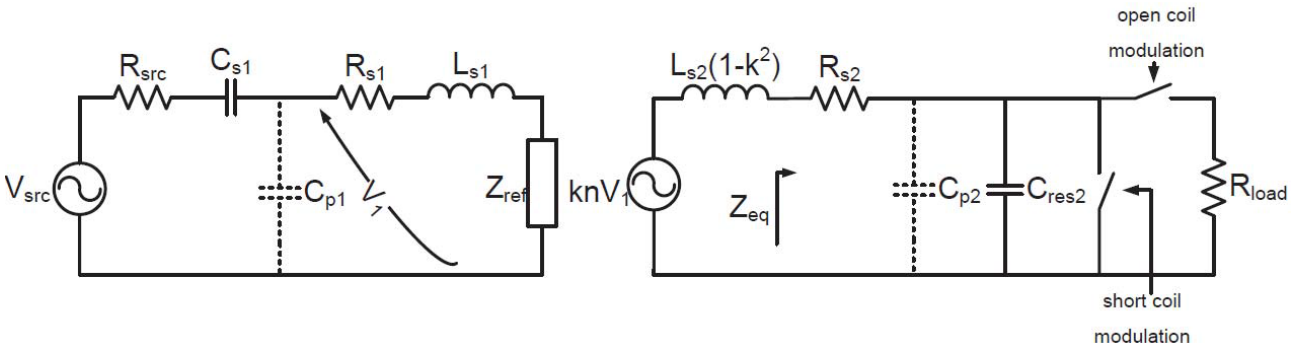


Fig. 3.8: Two possible architecture for load modulation (series or parallel switch) [3.5].

- Single switch in series with the load: when it is closed there no effect on the R_{load} because the R_{ON} of the switch is negligible. When the switch is opened R_{load} is disconnected from the rest of the circuit and here is possible to achieve the load modulation.
- Single switch in parallel with the load: when the switch is opened there are no effects on R_{load} but when the switch passes to the closed condition R_{load} is shortened and the load modulation is performed.

In particular the reflected impedance Z_{ref} on the primary side can be expressed by the following equation 3.1 (parasitic capacitance of the two coils are neglected).

$$Z_{ref} = \frac{\omega^2 k^2 L_{s1} L_{s2}}{R_{s2} + j\omega L_{s2} + \frac{R_{load}}{1 + j\omega C_{res2} R_{load}}} \tag{3.1}$$

If the first architecture is considered (switch in series), the modulation, as I mentioned before, is performed when the switch goes into the opened condition, and in this case the impedance of the equation 3.1 became the one in following equation 3.2.

$$Z_{ref} = \frac{\omega^2 k^2 L_{s1} L_{s2}}{R_{s2} + j\omega L_{s2} - \frac{j}{\omega C_{res2}}} \tag{3.2}$$

Considering, on the contrary, the second architecture with the switch in parallel, here the modulation is performed when it goes on the closed condition and the impedance became the one in the following equation 3.3.

$$Z_{ref} = \frac{\omega^2 k^2 L_{s1} L_{s2}}{R_{s2} + j\omega L_{s2}} \tag{3.3}$$

So, concluding, by modifying the reflected impedance (choosing one of the two proposed architectures) is possible to modify also the voltage V_1 on the primary side, because it is affected by R_{load}: in one state, called "high state", the amplitude of the voltage V_1 on the primary coil is higher than in the other state entitled "low state". Principal drawbacks on load modulation are the impossibility to go deeply in human tissue due to the high attenuation and the completely inefficiency of the link when the two sides are not perfectly parallel (the transmission efficiency is ideally up to 0% when the secondary side is rotated at 90° with respect to the first one). Load modulation is actually used for subcutaneous implants or wearable systems.

3.2 BACKSCATTERING

Backscattering modulation is particularly suited when the power constraints are not the same on both sides of the radio link, for example for biomedical applications and wireless memory tag [3.6][3.7]. The application of backscattering into the "Body Dust" project could be as well presented in the following Fig. 3.9.

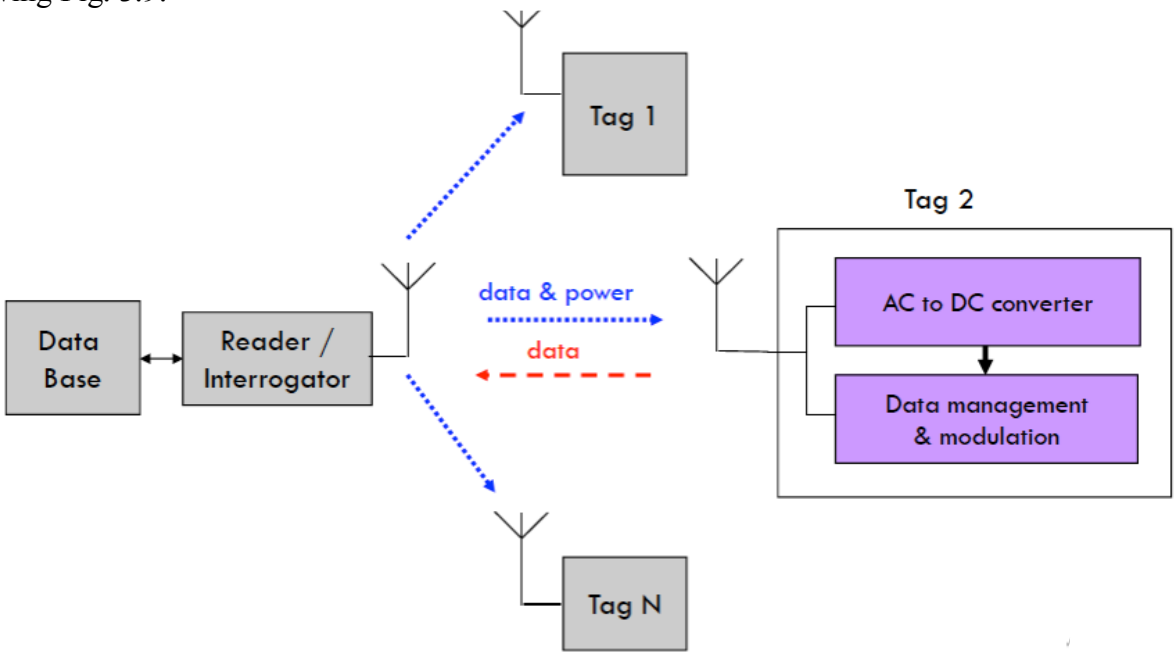


Fig. 3.9: Backscattering for remotely powered tags [3.1].

So, in this case is possible to modulate the incoming signal without using an inductive link but simply measuring the properties of the wave reflected by the tag.

3.2.1 INDUCTIVE COUPLING

Inductive coupling is generally used for near-field regions:

- $d < \frac{\lambda}{2\pi}$
- The typical frequency bands are between 125 kHz and 14 MHz.
- The effective operation distance is less than 10 cm.
- Higher energy efficiency at short distance.
- Load modulation operation is the mostly used for data communication.

In general, inductive coupling (magnetic field operation with coils as antennas) or capacitive coupling (electric field operation with metallic surfaces as antennas) are performed. The available power at the input tag is a function of d^{-6}.

3.2.2 ELECTRO-MAGNETIC COUPLING

The Electro-Magnetic (EM) coupling is generally used in far-field regions (Fig. 3.10):

- $d > \frac{\lambda}{2\pi}$
- The typical frequency bands are between 868 MHz and 3 GHz.
- The maximum effective operation distance is about 15 meters.
- Higher data bit rate due to the larger frequency bandwidth available.
- Backscattering operation is the mostly used for data communication.

In far-field the typical antennas are made by n-poles typed like monopole, dipoles of folded dipole. In general, the available power at the input of the tag is a function of d^{-2} and λ^2.

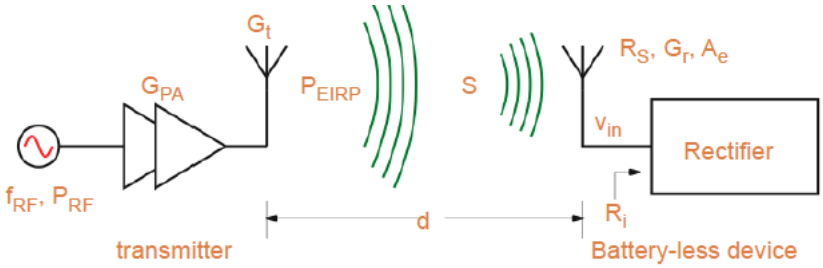


Fig. 3.10: Estimation of the input power in far field [3.8].

The power density at the tag antenna is described by the following equation 3.4.

$$S = P_{EIRP} * \frac{1}{4\pi d^2} \tag{3.4}$$

Where P_{EIRP} is the irradiated power defines as following equation 3.5.

$$P_{EIRP} = P_t G_t \tag{3.5}$$

The collected power by the tag antenna, or the real power available to the load is defined by the equation 3.6.

$$P_{AV} = A_E S \tag{3.6}$$

In which A_E is the antenna opening defined as follows (equation 3.7).

$$A_E = G_r * \frac{\lambda^2}{4\pi} \tag{3.7}$$

G_t is the gain of the transmitted antenna while G_r is the gain of the receiver one.

3.2 BACKSCATTERING DATA COMMUNICATION

As I have already explained before, in the backscattering communication the carrier is generated in the interrogator node also called reader. The tag, or transponder, modulates and reradiates the incoming signal from the interrogator when there is a high impedance mismatch (Fig. 3.11).

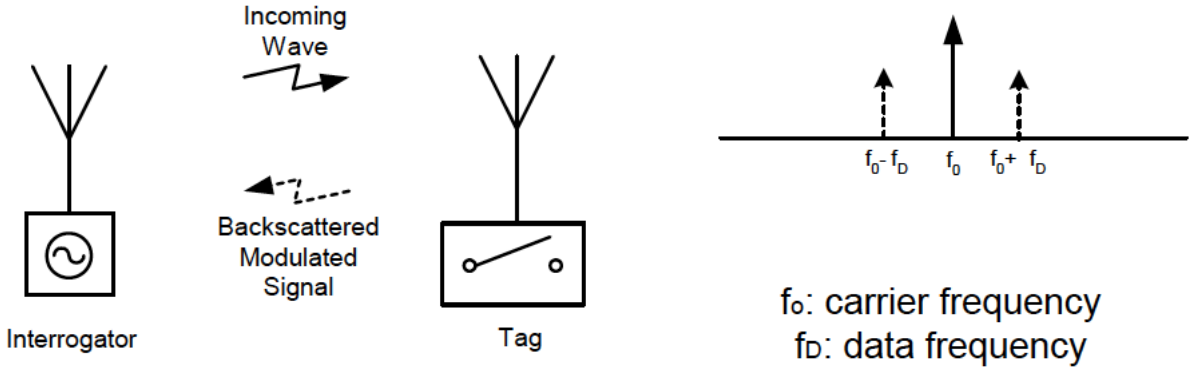


Fig. 3.11: Backscattering data communication principle (left) and modulation of the RF carrier (right) [3.1].

In this situation, the power consumption of the tag is minimized because it does not include an oscillator to generate the carrier, but it is a simple modulation of the received one.
In particular, a binary configuration is possible:

- If the data bit is equal to 1 the load is mismatched to the tag antenna and all the power of the incoming signal is reflected to the interrogator.
- If the data bit is equal to 0 the load is matched to the tag antenna and all the power of the incoming signal is adsorbed by the tag.

Obviously the two situations are complementary and so the two possible configurations are presented in the following Fig. 3.12.

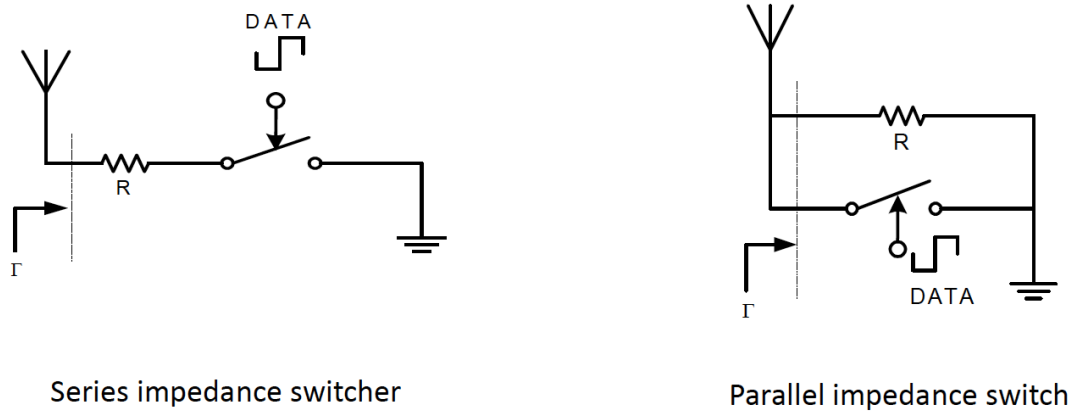


Fig. 3.12: Series and parallel impedance switcher [3.1].

The reflection coefficient Γ at the antenna-tag interface can vary both in amplitude and in phase and so two basic binary modulation types are possible.

3.2.1 ASK MODULATION

ASK is the Amplitude Shift Keying (Fig. 3.13).

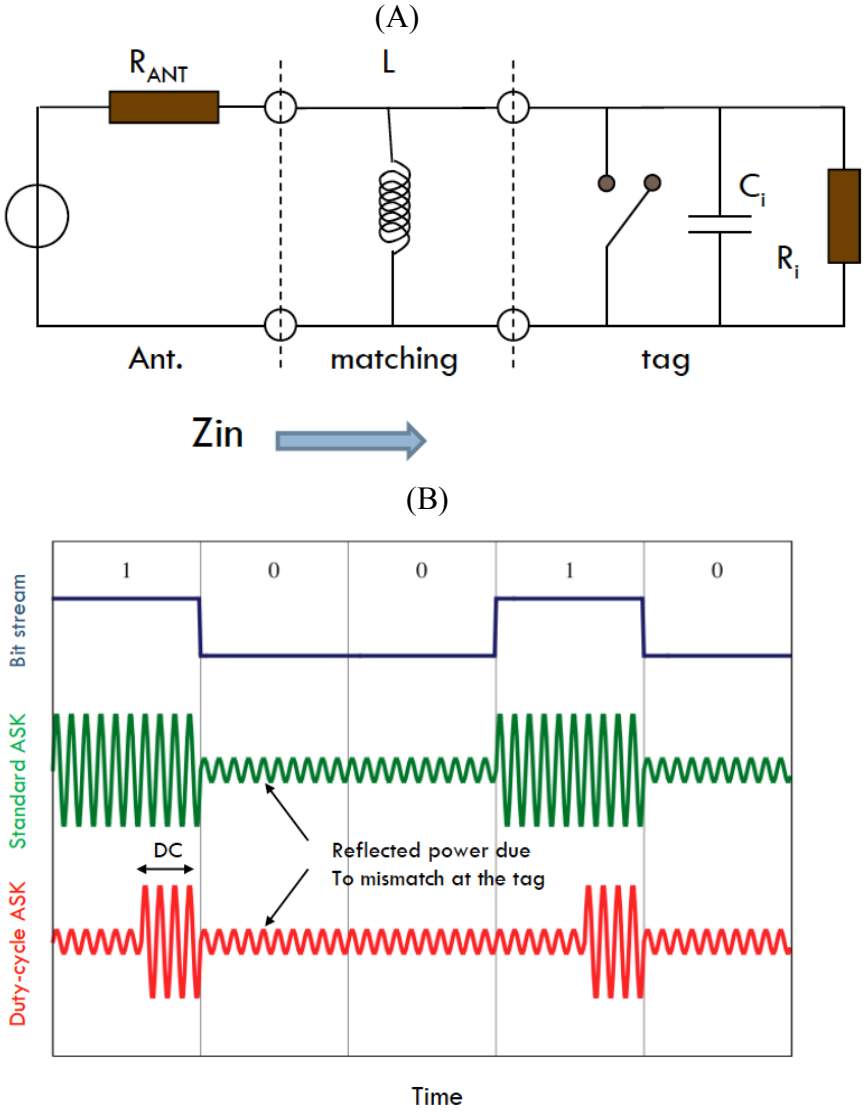


Fig. 3.13: ASK modulation: electrical configuration (A) and reflected modulated signal (B) [3.1].

In this type of modulation when the transmitted bit is 1 the switch is closed while when the transmitted bit is equal to 0 the switch is open.
This is the simplest modulation and it will be used as OOK modulation (On-Off Keying) in the proper communication circuit (Chapter 5).

3.2.2 PSK MODULATION

PSK (Phase Shift Keying) is a little bit complicated in terms of electrical circuit analysis (Fig. 3.14).

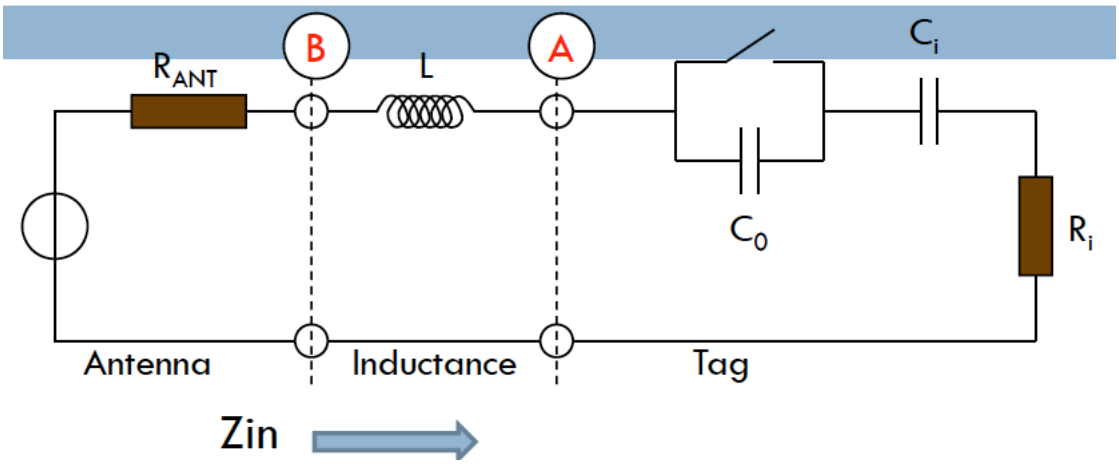


Fig. 3.14: Electrical model of PSK modulation [3.1].

Observing the figure above, in B both the adsorbed active power and the reflected active power are constant while in A the voltage at tag input is however not constant. The reflected signal is modulated by the switch that in this case is in parallel with a capacitive component and, in particular, when the switch is closed bit 1 is transmitted while when it is open bit 0 is transmitted (Fig. 3.15).

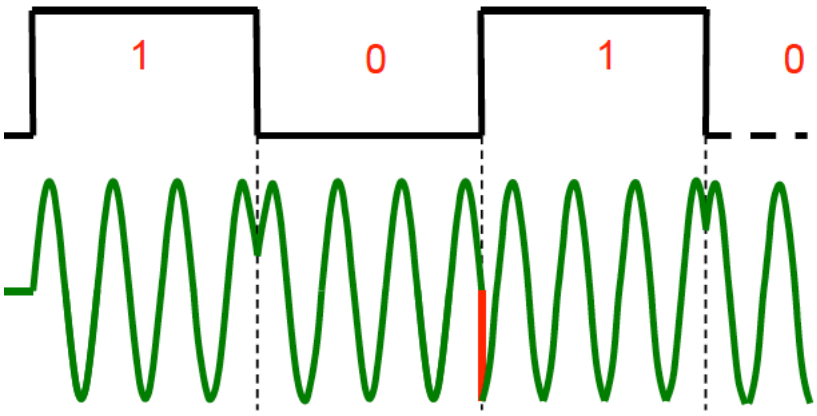


Fig. 3.15: PSK reflected modulated signal [3.1].

The two introduced modulation methods need to be compared in terms of performances in order to understand if one is preferable with respect to the other. In particular in [3.8] the BER (Bit Error Rate) is taken as an indicator of the performances of the two different modulations (Fig. 3.16). In order to be clear $BER = 10^{-4}$ means that 1 bit is not correct over 10000. Random noise could be a potential crucial point for the transmission because can make the translate of the signal by the receiver very difficult: in particular the transition time periods (between the two different logical states) may become very hard to recognize. So, the BER influences a lot the transmission efficiency introducing random errors that may converge in misunderstanding on the translation.

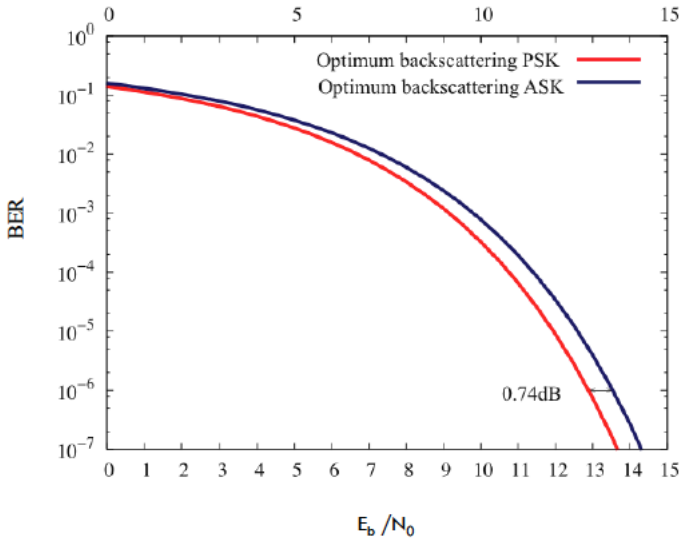


Fig. 3.16: ASK and PSK comparison by BER [3.9].

In the figure above there are two parameters on the x-axis: E_b is the average energy per bit and N_0 is the noise level at receiver input.
The real responsible of the modulation is the reflection coefficient Γ (equation 3.8).

$$\Gamma = \frac{R_i - R_{ANT}}{R_i + R_{ANT}} \tag{3.8}$$

The matching condition is achieved when $\Gamma = 0$ and $\alpha = 1$ (Fig. 3.17).

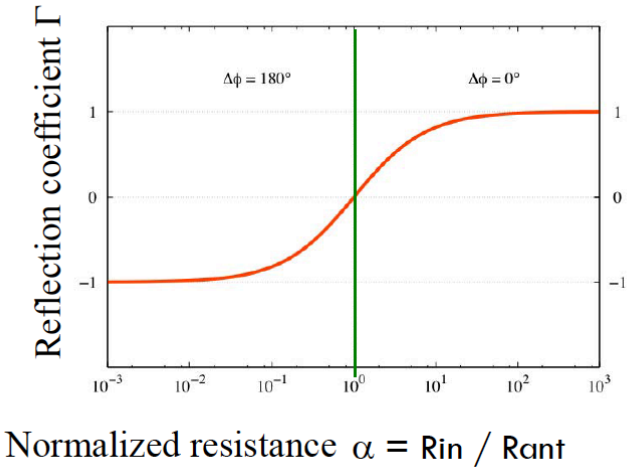


Fig. 3.17: Reflection coefficient [3.1].

CHAPTER 4

CMOS DESIGN

4.1 CMOS IC design

The proper design of the communication circuit is implemented through Cadence Virtuoso IC6.1 and the technology I chose is UMC 180 nm CMOS. The idea is to start with this Process Design Kit (PDK), that is relatively elderly and cheap, because the issue at this starting point is to understand the limits of the testing circuit in terms of occupied area and power consumption. As the architecture is successfully obtained, is so simple to reproduce it using more advanced technologies scaling all the protocol from 180 nm to 130 nm for example.
CMOS (Complementary Metal Oxide Semiconductor) IC (Integrated Circuit) design process consist on a specific flowchart that all the designers need to follow (Fig. 4.1).

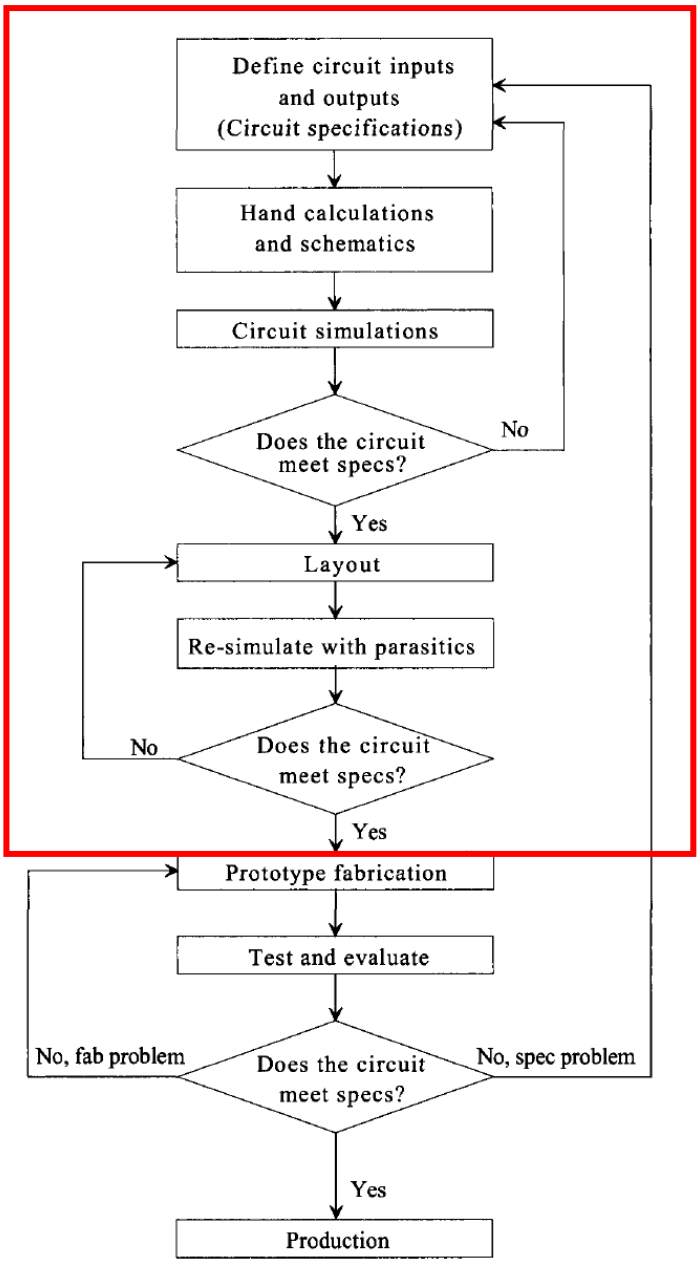


Fig. 4.1: Flowchart for the CMOS IC design process (reprinted from [4.1]).

The issue of this thesis is to perform the task described in the red box of the chart above. I have already explained the specification of this research in the Chapter 2, the inputs of the circuit are:

- the processed signal extracted by the sensor;
- the digital word that is needed in order to discriminate different meaningful signals. This word will be considered as a 3 parallel input that came from the multiplexing layer of the complete IC project.

An entire CMOS project could be inserted into the very large scale integrated (VLSI) circuit chip, which will contain thousands or millions of metal oxide semiconductor field effect transistors (MOSFETs). In the following Fig. 4.2, there is a simple illustrated description of the fabrication flow for NMOS e PMOS transistors separated by FOX (Field OXide) as isolators.

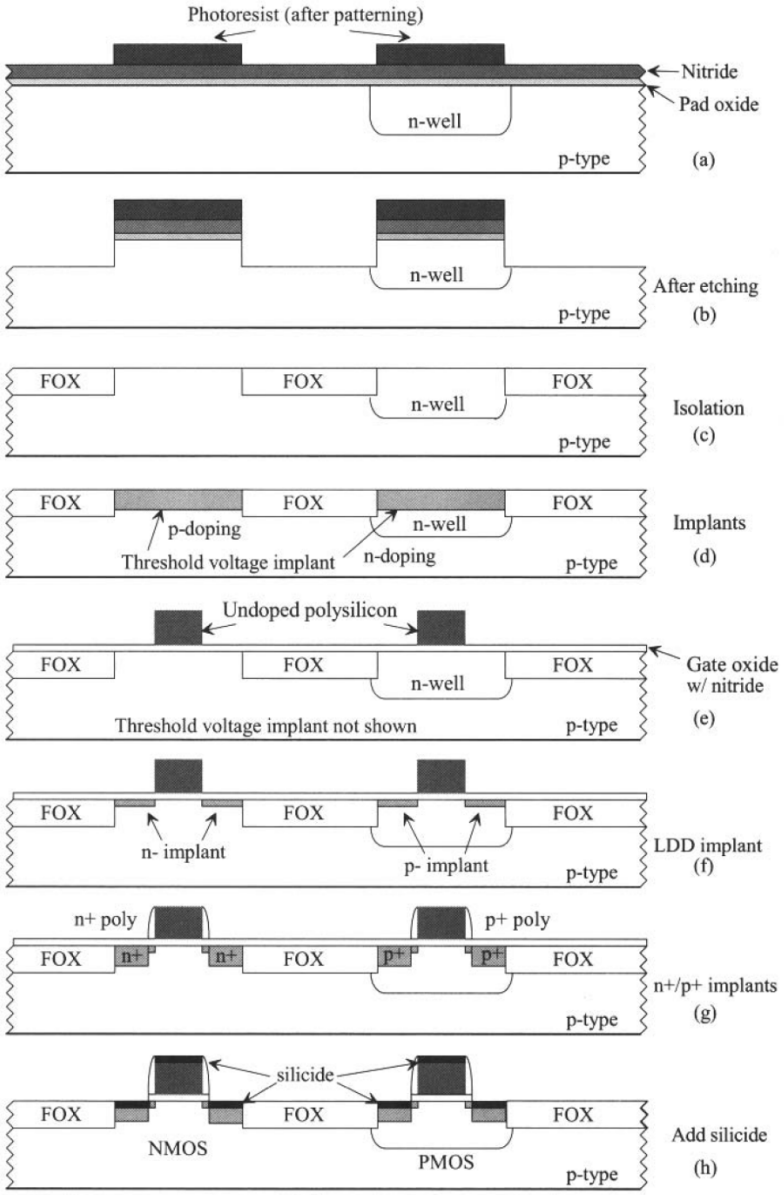


Fig. 4.2: General NMOS e PMOS process flow [4.1]

Writing about MOSFETs it is important to define the symbols and a global way to call them in order to be clear and exhaustive. The general symbols to represent NMOS and PMOS devices are the ones shown in Fig. 4.3.

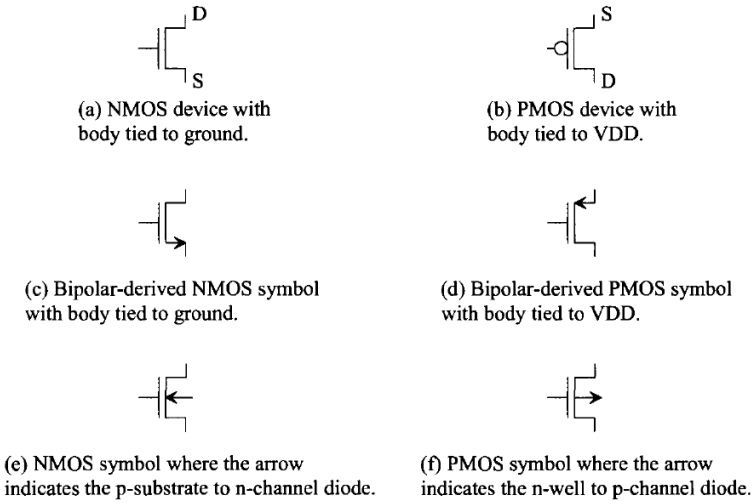


Fig. 4.3: Symbols to represent MOSFETs. (a) and (b) NMOS e PMOS in which bulk terminal is supposed connected do ground (NMOS device) or VDD (PMOS device). Drain and source are interchangeable. (c) and (d) bipolar-derived symbols where the arrow represents the direction of drain current flow (derived from a bipolar junction transistor symbol). (e) and (f) NMOS e PMOS schematic drawn view of the simulator used where the arrow in the bulk terminal represents the p-substrate (or p-well) to n-channel diode (NMOS) or the p-channel to n-well diode (PMOS). [4.1]

In particular the symbols in Fig. 4.3e-f are the perfect explanation of the real MOSFETs (Fig. 4.4).

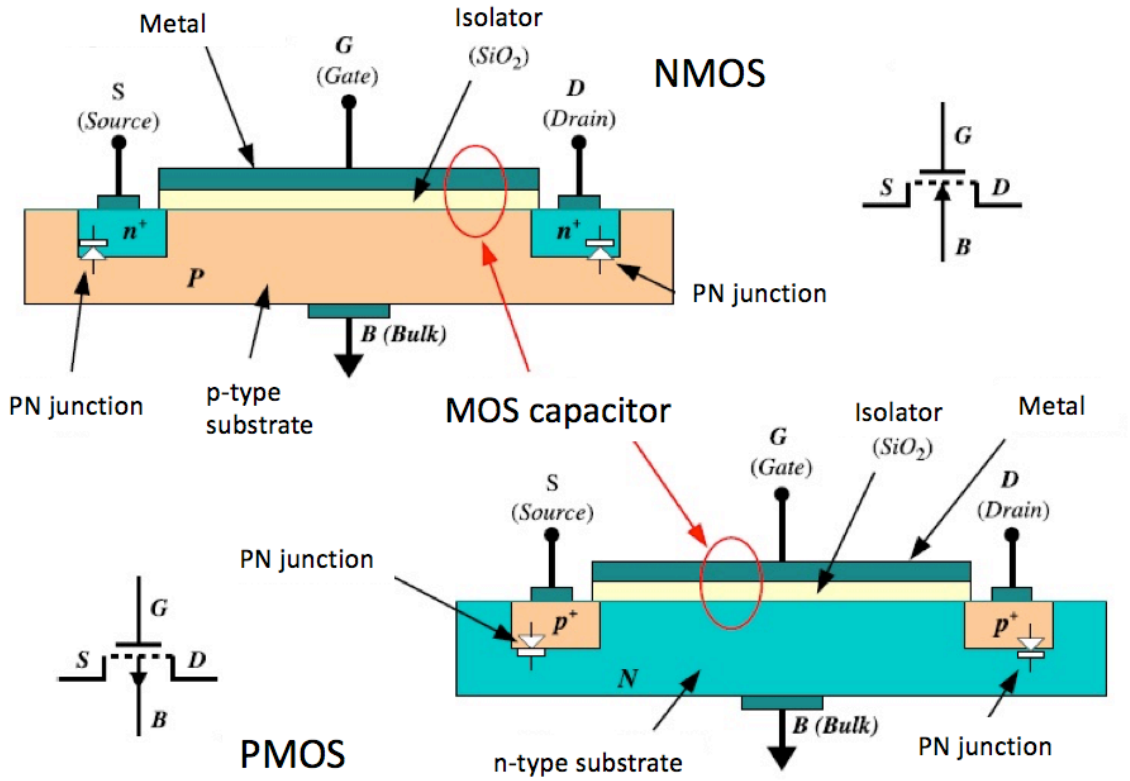


Fig. 4.4: NMOS e PMOS transistors

4.2 CIRCUIT LIBRARY

Approaching for the first time to CMOS design, the first important thing to do is to create a starting library with all the digital component, all the logical ports and all the stable elements in order to start thinking on the organization of the circuit. All of these elements are simply made using the described transistors in a properly correct way. The first three components are so: inverter, NAND (AND) and NOR (OR). These three ports (five, in reality) are probably the most important: they are the first pieces to completely build most digital circuits.

4.2.1 INVERTER (NOT)

The inverter is the simplest element made using only two transistors, one NMOS and one PMOS, creating four pins: input (IN), output (OUT), ground (gnd) and voltage supply or Vdd (Fig. 4.5.).

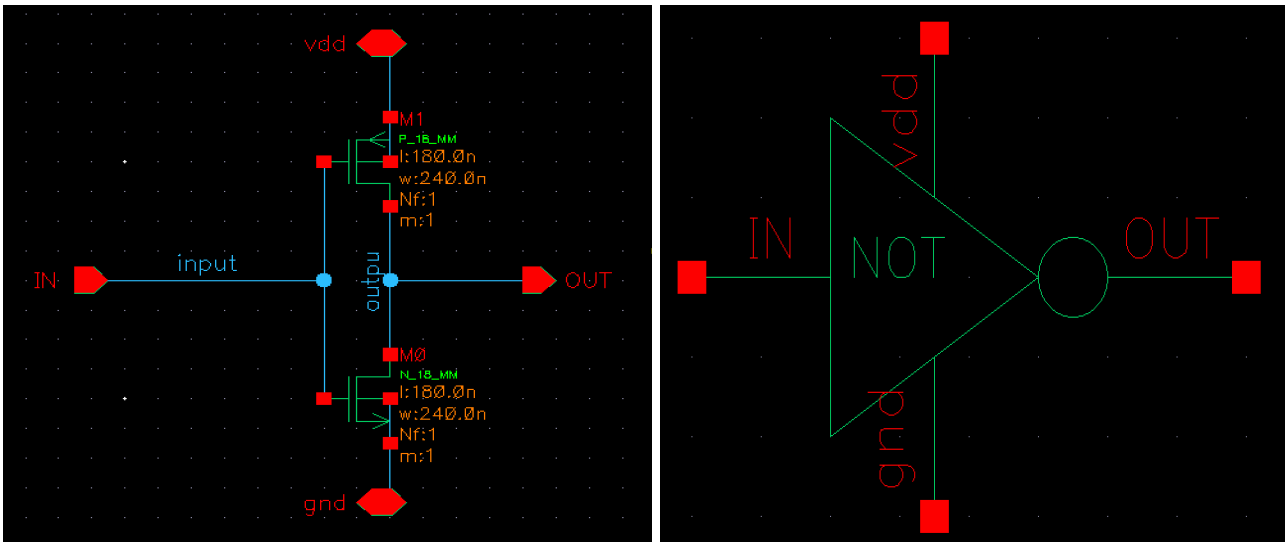


Fig. 4.5: CMOS inverter schematic (left) and logic symbol (right).

The inverter performs the simple logic operation of A to not(A) as Fig. 4.6 shows. When the input to the inverter is connected to ground, the output is pulled to VDD through the PMOS device M1 (and M0 shuts off). When the input terminal is connected to VDD, the output is pulled to ground through the NMOS device M0 (and M1 shuts off).

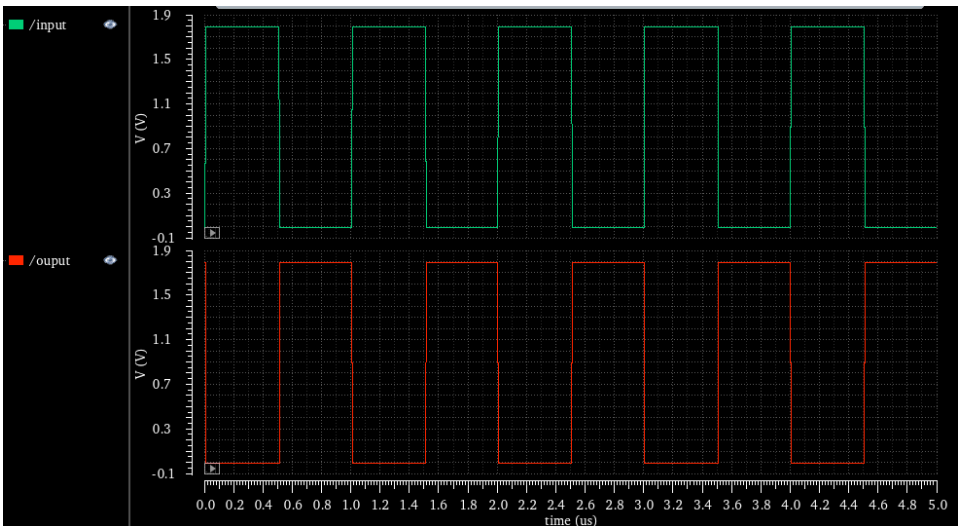


Fig. 4.6: Transient analysis of minimum size inverter.

For the inverter I will extend the discussion introducing all the important parameters to control the characteristics of the inversion. All of these considerations are also valid for all the elements that I will introduce later.
In particular, as the components are not ideal, switching from high logic level (1) or Vdd supply voltage to low logic level (0) or ground (gnd) and vice versa are time dependent. In general, it is possible to describe the transfer characteristic of the inverter highlighting the switching point (Fig. 4.7).

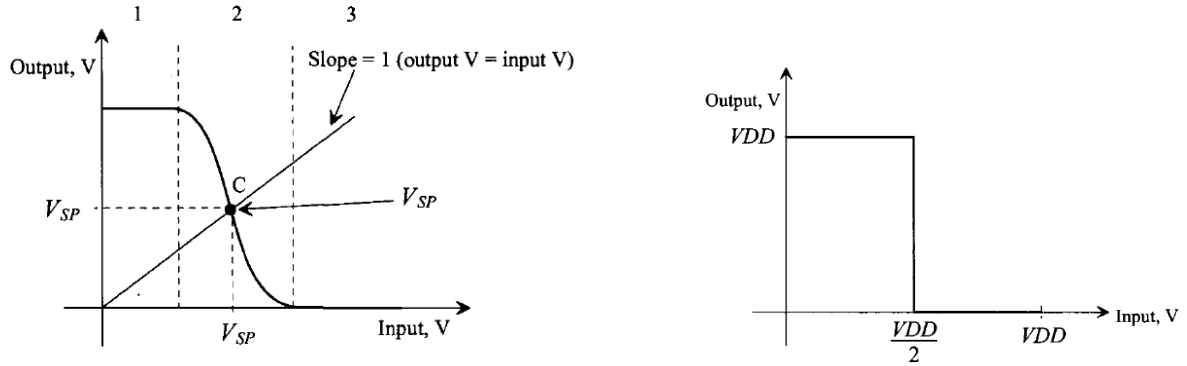


Fig. 4.7: Transfer characteristic of the CMOS inverter highlighting the switching point (left) and ideal transfer characteristic (right) [4.1].

As the figure shows, it is possible to divide the real voltage transfer plot wave in three different regions:

- In region 1 the PMOS is on while the NMOS is off.
- In region 2 the two MOSFTEs are both on.
- In region 3 the PMOS is off while the NMOS is on.

At the point C (inverter switching point) both M0 and M1 are in the saturation region. The ideal switching point voltage V_{SP} is exactly the half of the supply voltage Vdd but, in reality, it depends on many factors. Since the drain current at the switching point must be equal for both NMOS and PMOS is possible to calculate the switching point by simple manipulation of the equation 4.1 below:

$$\frac{\beta_n}{2}(V_{SP} - V_{THn})^2 = \frac{\beta_p}{2}(V_{DD} - V_{SP} - V_{THp})^2 \tag{4.1}$$

Obtaining the following result:

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}}V_{THn} + (V_{DD} - V_{THp})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \tag{4.2}$$

In which V_{THn} and V_{THp} are typical values voltage supply dependent, β_n and β_p depends on the sizes, length (L) and weight (W), of the CMOS devices. In particular:

$$\beta_n = KP_n \frac{W_0}{L_0} \tag{4.3}$$

$$\beta_p = KP_p \frac{W_1}{L_1} \tag{4.4}$$

Where KP is the transconductance parameter of the CMOS devices ($\frac{\mu A}{V^2}$).

Concluding, by varying the relative sizes of the two transistors is possible to shift the switching point and so modify the transition times from one logic level to another.
This effect has its electrical explanation by observing the electrical model of the inverter in Fig. 4.8 below.

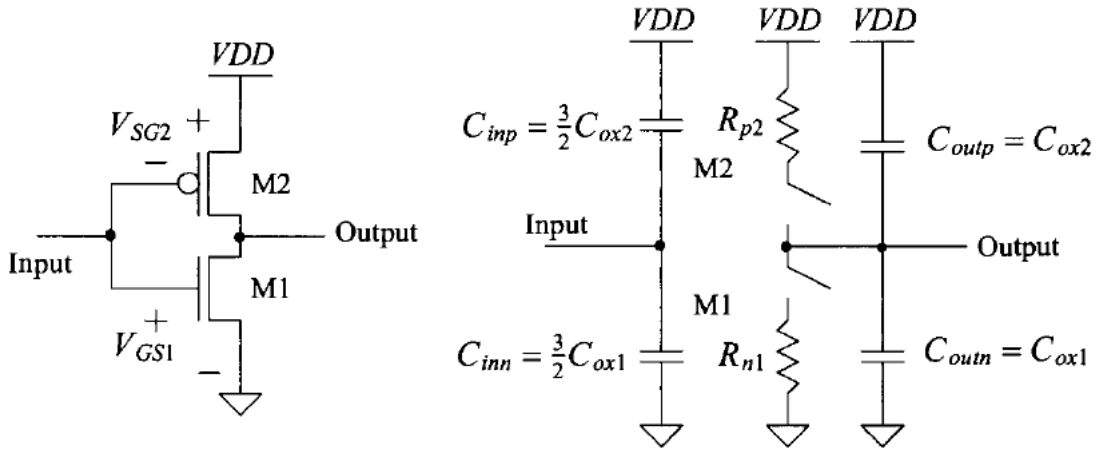


Fig. 4.8: The CMOS inverter switching characteristic using the digital model. [4.1]

As the figure shows there are two total capacitances that came from the input and output connections and two resistances in series with the two switches that are the simplest electrical model of the transistors (notice that here the switches are shown both open but in practice one of them is close making the output connection with Vdd or gnd).
The total effective input capacitance is:

$$C_{in} = \frac{3}{2}(C_{ox1} + C_{ox2}) \tag{4.5}$$

While the total output capacitance is:

$$C_{out} = C_{ox1} + C_{ox2} \tag{4.6}$$

And so, the intrinsic propagation delay of the inverter is simply:

$$t_{PLH} = 0.7\, R_{p2}\, C_{out} \tag{4.7}$$

$$t_{PHL} = 0.7\, R_{n1}\, C_{out} \tag{4.8}$$

The real effect that is noticeable by varying the ratio between β_n and β_p is to increase or decrease the intrinsic propagation delay.
The figure below shows exactly, qualitatively, the effect of all of this discussion through a simple simulation in Cadence in which the width of the PMOS is increased from the minimum value for the UMC 180 (240 nm) to four times that value (960 nm). Maintaining equal lengths, this operation modifies the ratio between the bethas (β_n/β_p) and the effect is the shifting of the switching point and consequently the modification of the propagation delay.

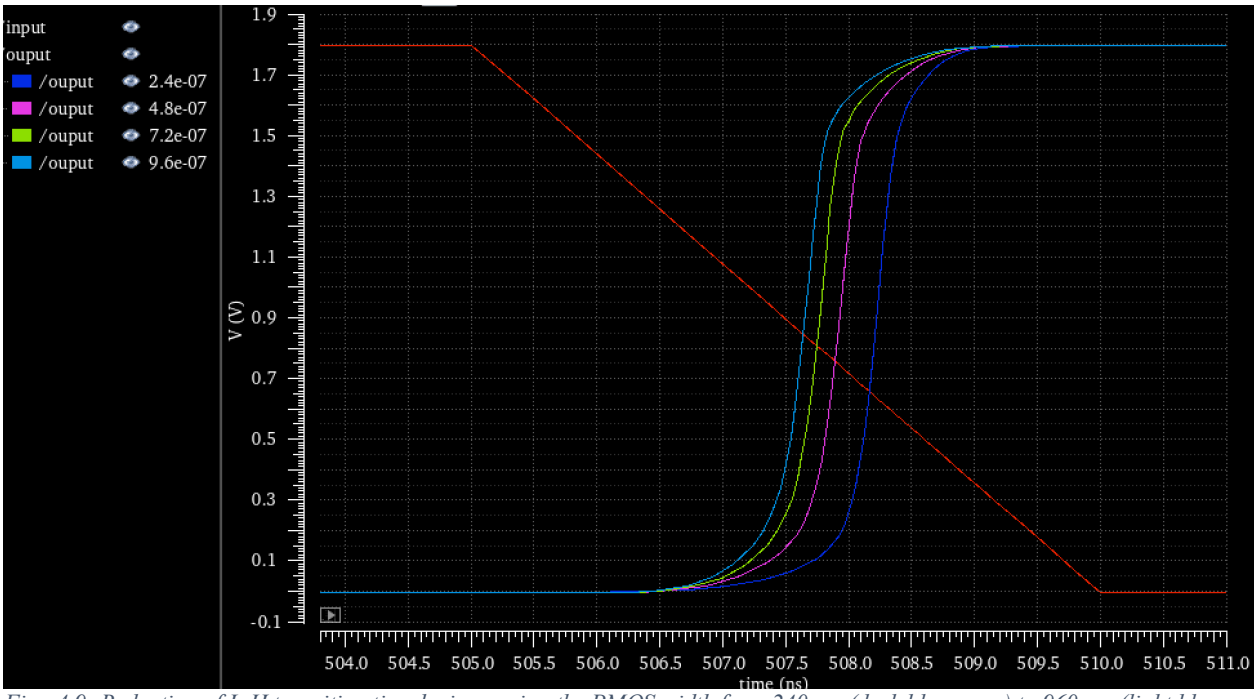


Fig. 4.9: Reduction of L-H transition time by increasing the PMOS width from 240 nm (dark blue wave) to 960 nm (light blue wave).

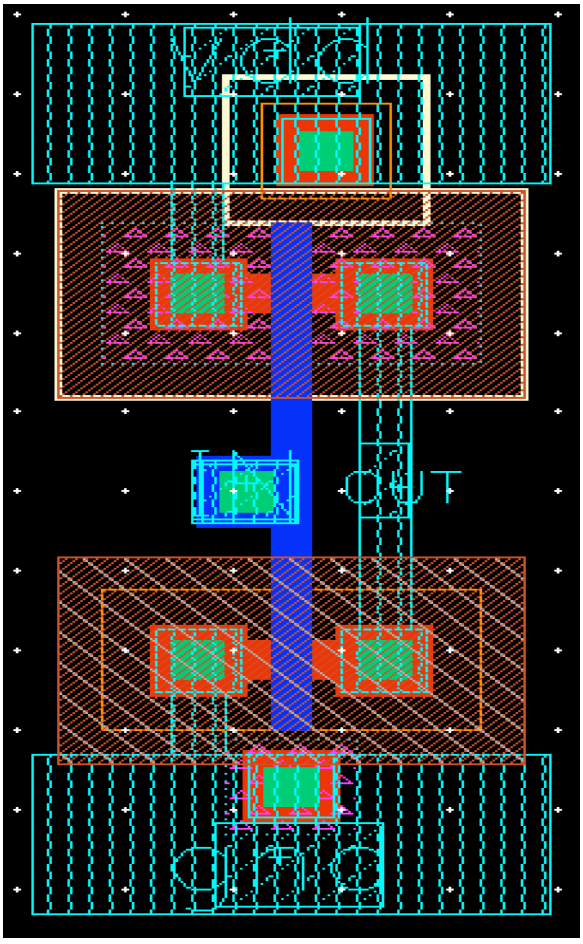


Fig. 4.10: Inverter layout

The two input and output capacitances of whose above will be automatically generated after the extraction of the parasitic capacitances from the layout of the inverter device.
In particular in Fig. 4.10, the layout of the inverter is shown: all the circuit connections are made using ME1 (light blue) and PO1 (dark blue). Two VIAs are created, N-WELL implant for the voltage supply Vdd and P-WELL diffusion for the ground (Fig. 4.10).

After designing the inverter, I used Assura in order to verify DRC (Drawing Rule Check) and LVS (Layout Versus Schematic).

Now running Quantus QRC, it is possible to extract all the parasitic capacitances and so making another time the simulation in order to observe if the parasitic capacitances influence the functionality of the device.

In the Fig. 4.11 below the extracted view is presented.

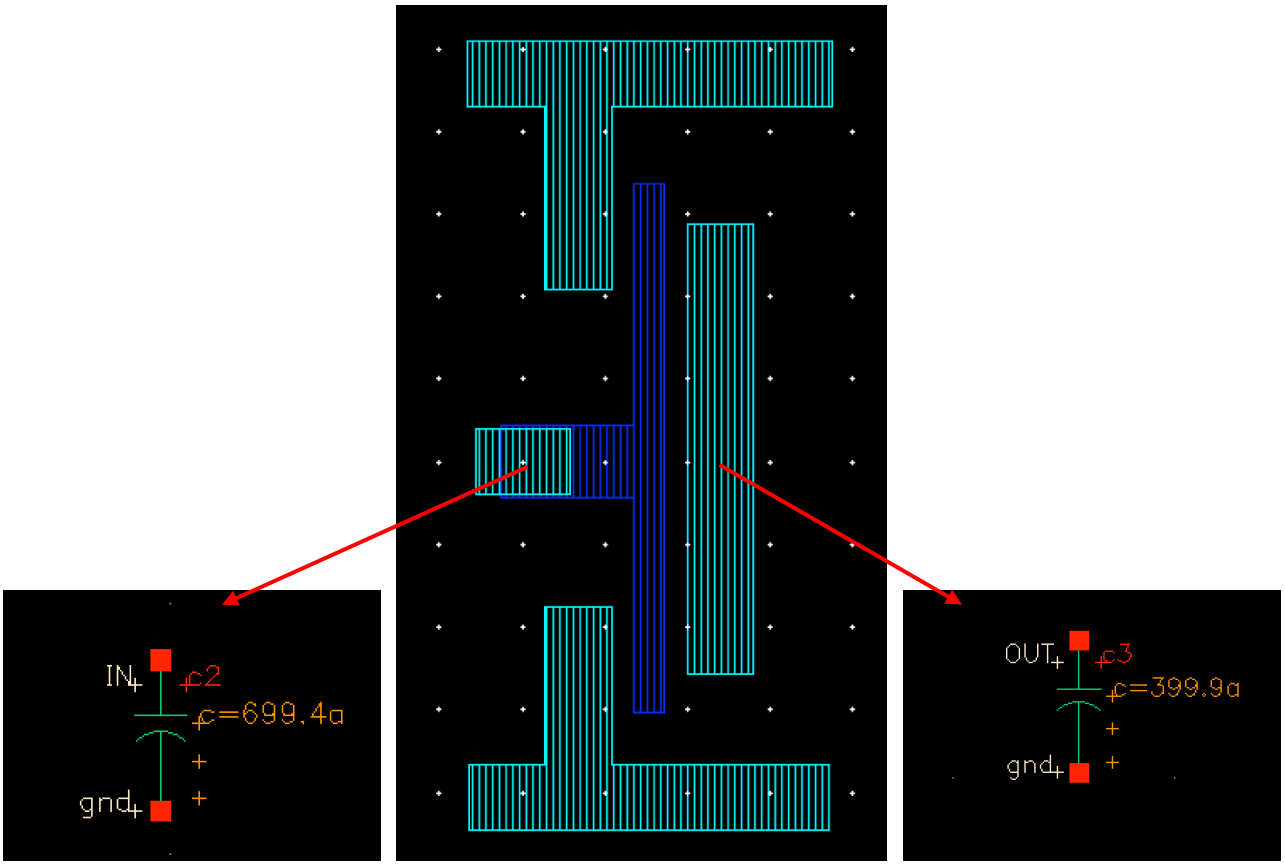


Fig. 4.11: Extracted view of the CMOS inverter (center). Input parasitic capacitance (left) and output parasitic capacitance (right).

At this point the post-layout simulation is performed and the result are shown in Fig. 4.12.

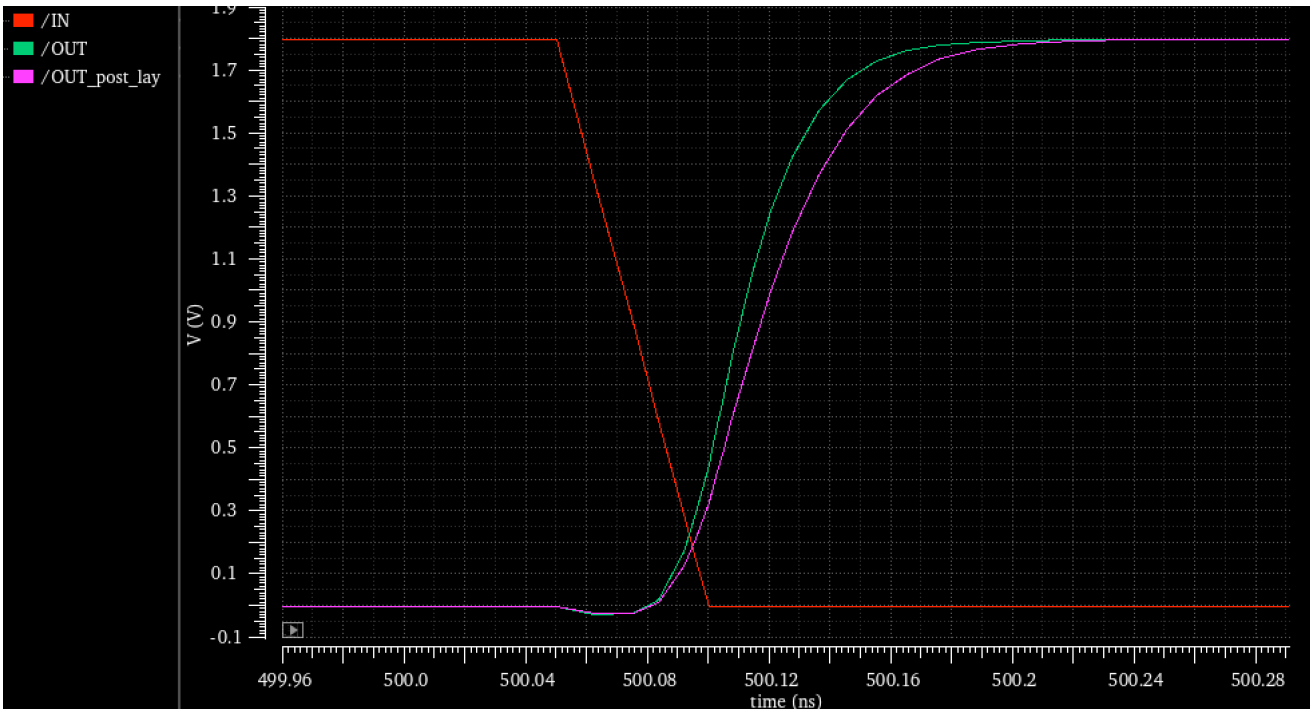


Fig. 4.12: Pre and Post-layout simulation of an inverter. Differences for rise timing between the two outputs.

As the figure shows there are some small difference between the outputs before and after the insertion of the parasitic capacitance. This is an important aspect that need to be taken into consideration for the custom design of the full circuit because here, for the inverter alone, the parasitic capacitances do not influence too much the output because the metal net connections are very small (proportional to the device sizes) but they could not be negligible for more complicated devices.
The following sections are organized showing in the order the component schematic: the symbol view, the transient analysis, the layout design, and the extracted view.

4.2.2 NAND

NAND port is composed by four transistors, two NMOS and two PMOS. Here the number of pins change accordingly to the number of inputs that the port can analyze: instead of the standard two inputs cell (Fig. 4.13) is possible to increase the number of inputs to 3, 4, 8 and so on.

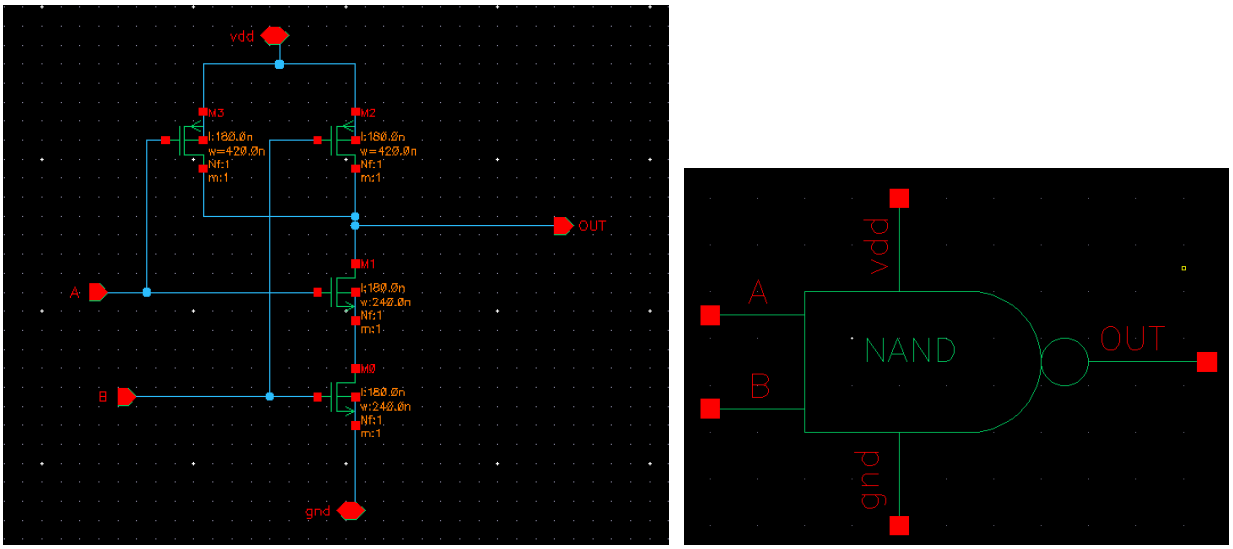


Fig. 4.13: CMOS NAND schematic (left) and symbol view (right),

If the two inputs are A and B the NAND perform the logical not(AB). In Fig. 4.14 the result of the simulation is shown using two a-phased squares waves as inputs.

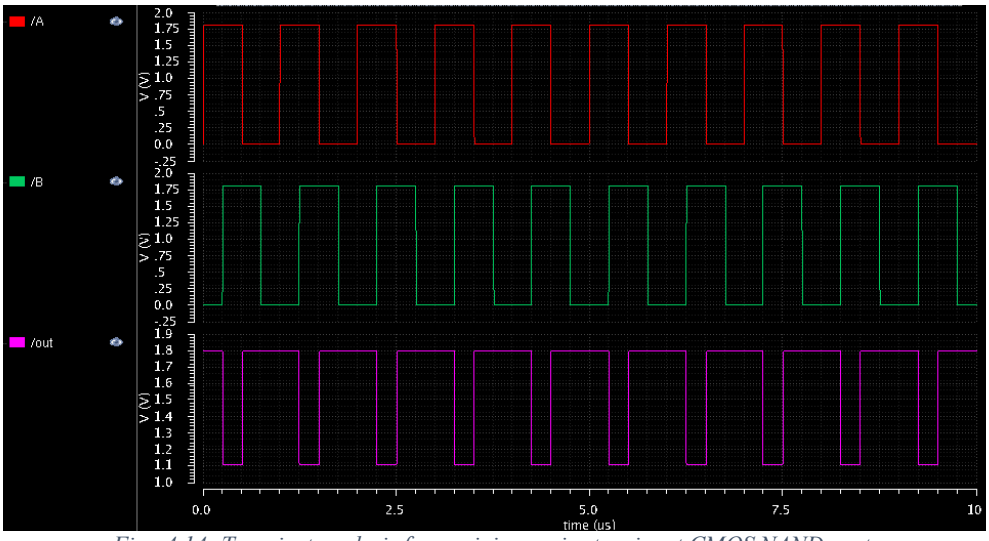


Fig. 4.14: Transient analysis for a minimum size two input CMOS NAND port.

The layout of the two input NAND gate is presented in the following Fig. 4.15. It is important to observe that the design is made trying to reduce the sizes and so overlapping the transistors.

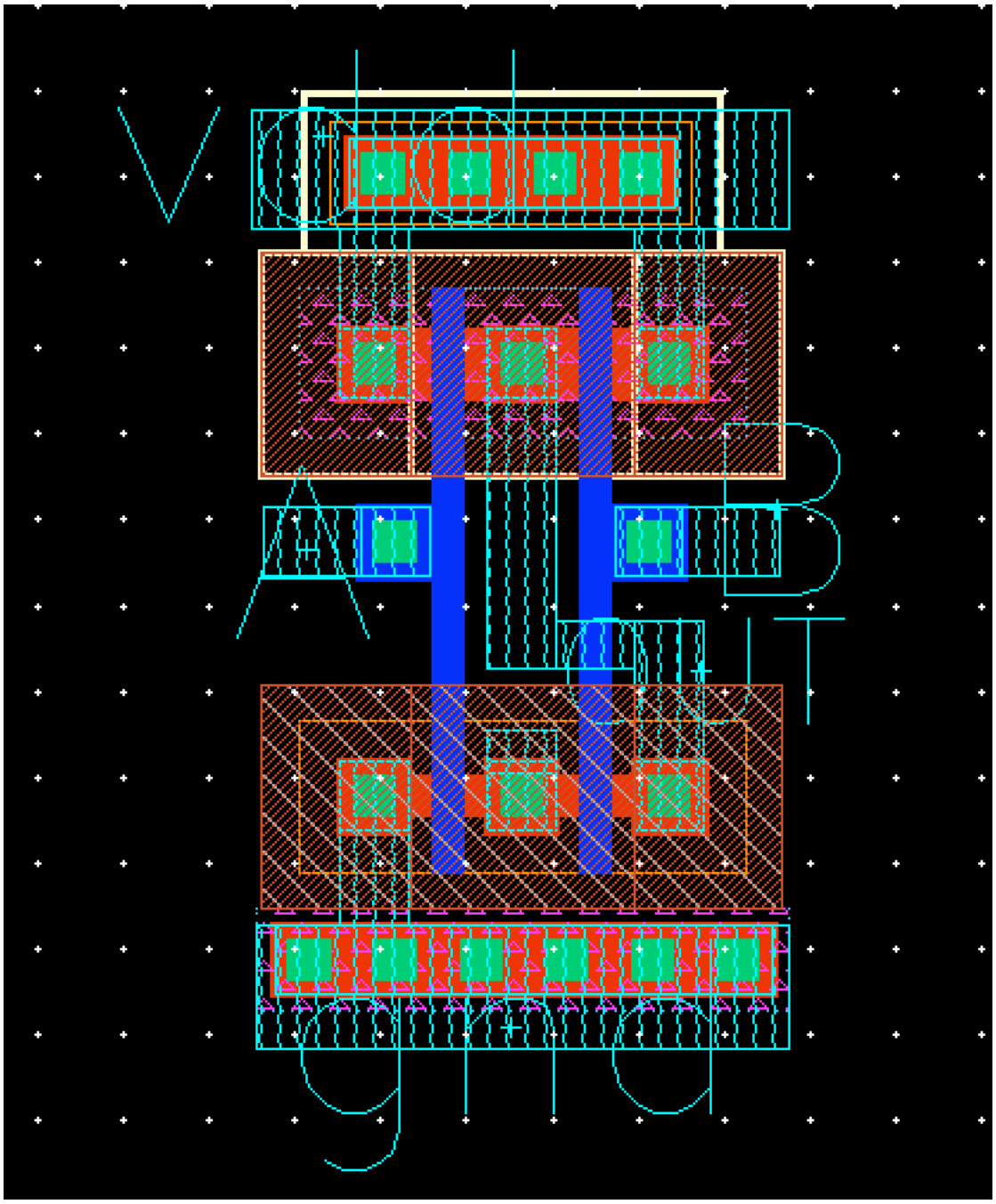


Fig. 4.15: NAND layout.

By extracting the parasitic capacitances (Fig. 4.16) is possible to observe also in this case some small differences between the simulations pre and post-layout caused by the capacitors.

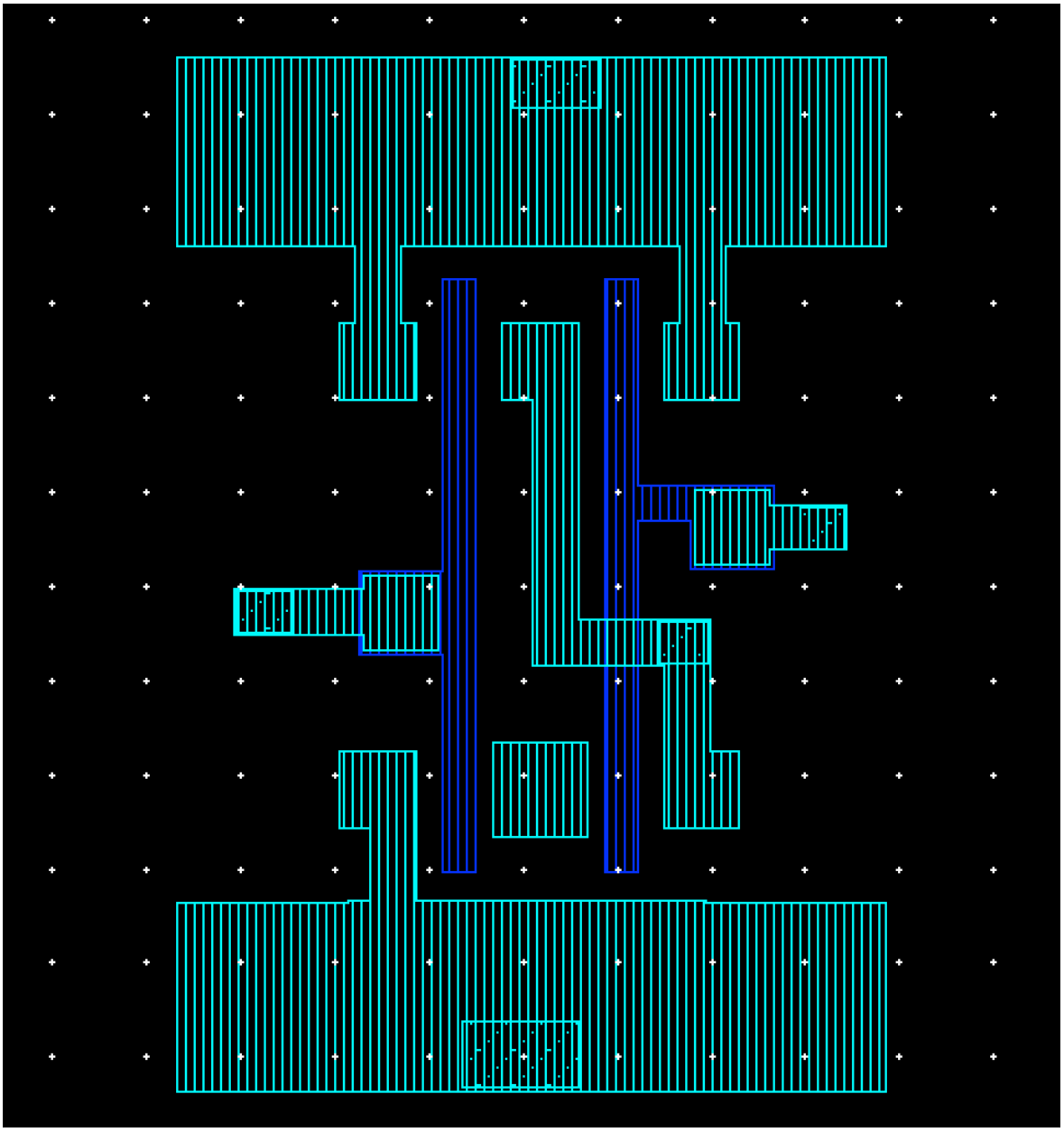


Fig. 4.16: Extracted view of NAND.

4.2.3 AND

In order to design the AND port a simple combinational operation is performed. The output is the same of the NAND one but inverted. In the Fig. 4.17 the schematic and symbol views are presented.

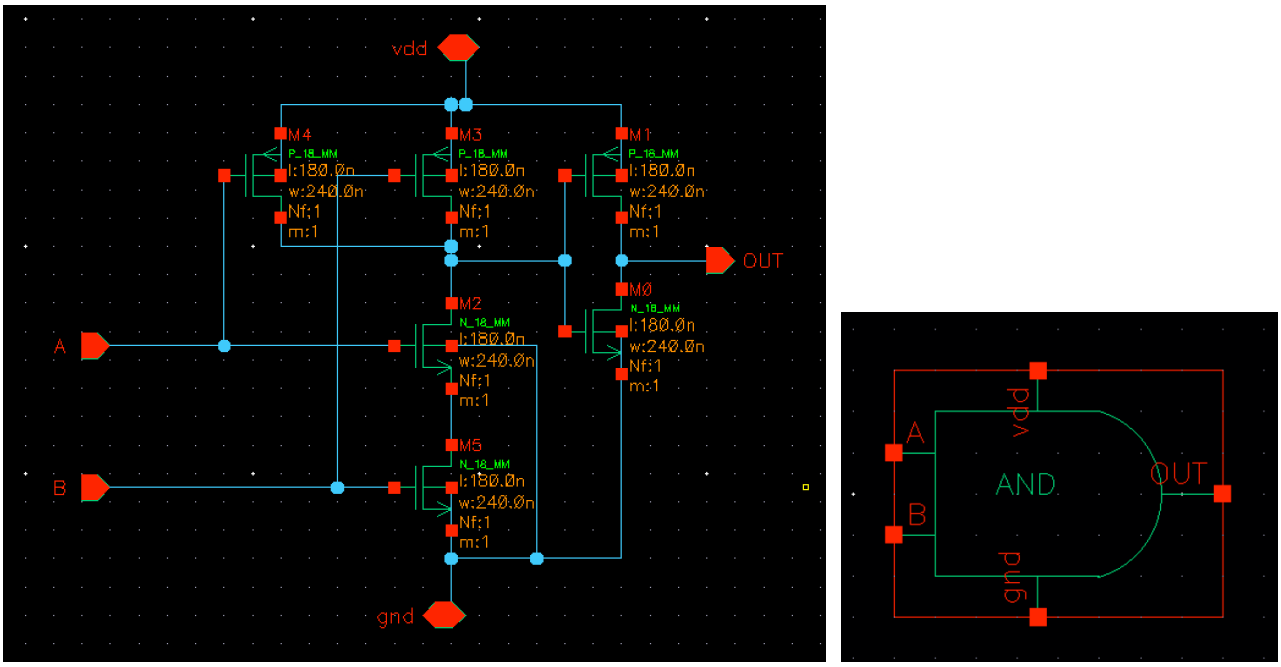


Fig. 4.17: AND schematic view (left) and symbol (right).

Here, below, in the Fig. 4.18, the transient analysis of a simple two inputs AND port is shown, using the same square waves than before to analyze the output that is exactly the same of the NAND one but inverted.

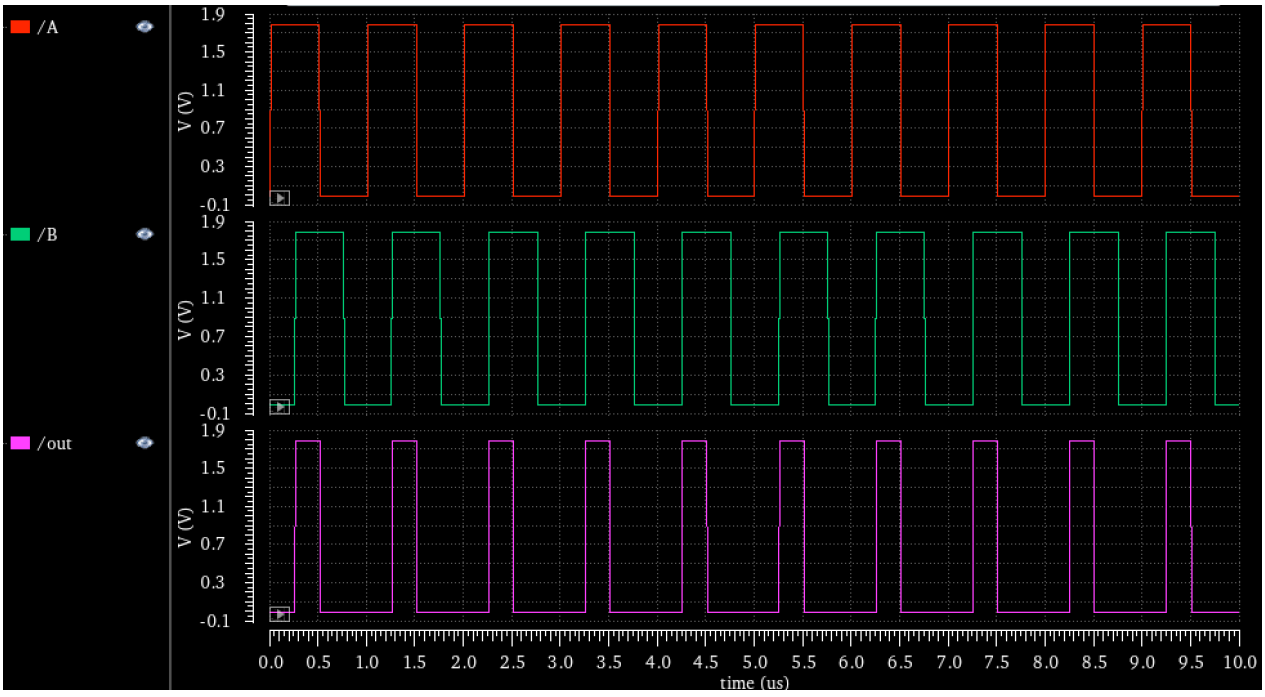


Fig. 4.18: Transient analysis for a minimum size two input CMOS AND port.

The layout of the AND is presented in the Fig. 4.19 and the extracted view is show in the next Fig. 4.20.

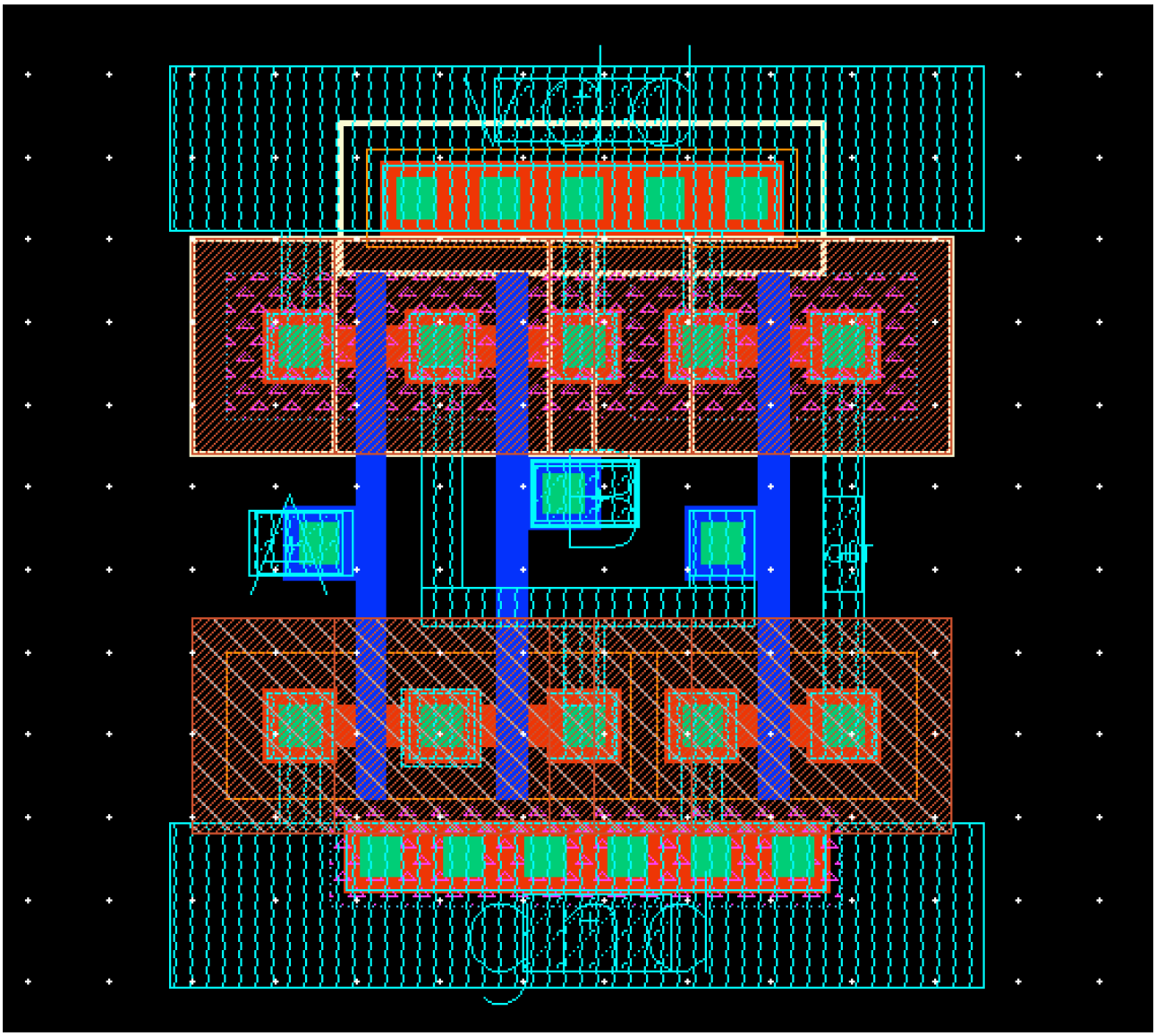


Fig. 4.19: AND layout.

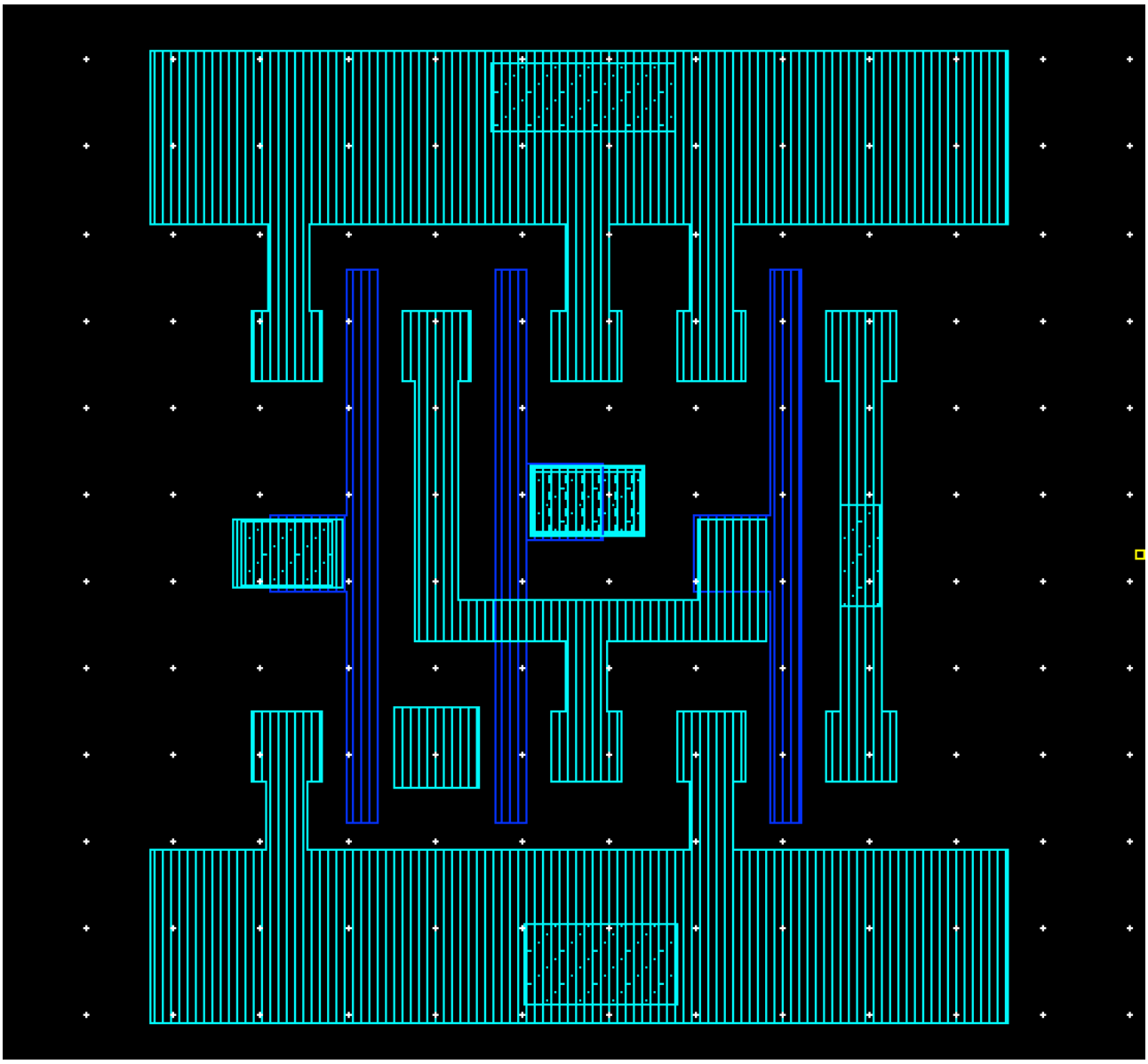


Fig. 4.20: Extracted view of AND port.

4.2.4 NOR

The NOR port is usually composed by four transistors, two NMOS and two PMOS. Also here, the number of pins change accordingly to the number of inputs that the port can analyze: instead of the standard two inputs cell (Fig. 4.21) is possible to increase the number of inputs to 3, 4, 8 and so on.

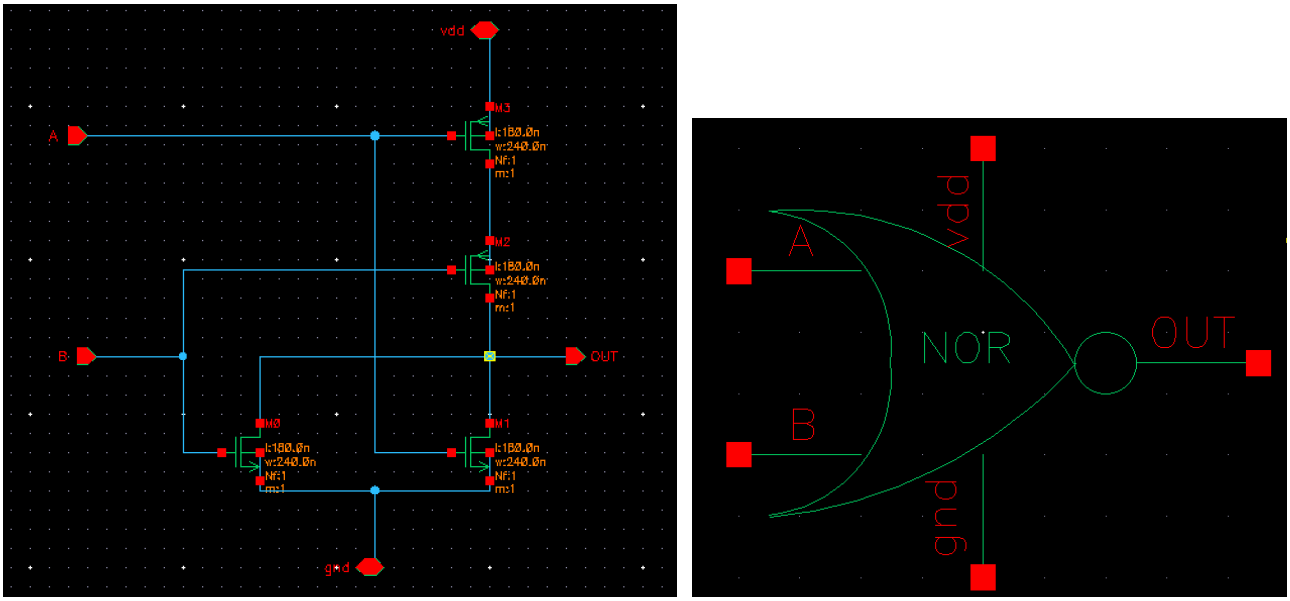


Fig. 4.21: CMOS NOR schematic (left) and symbol view (right),

If the two inputs are A and B the NOR gate perform the logical not(A+B). Fig. 4.22 shows the result of the simulation using two a-phased square waves as inputs.

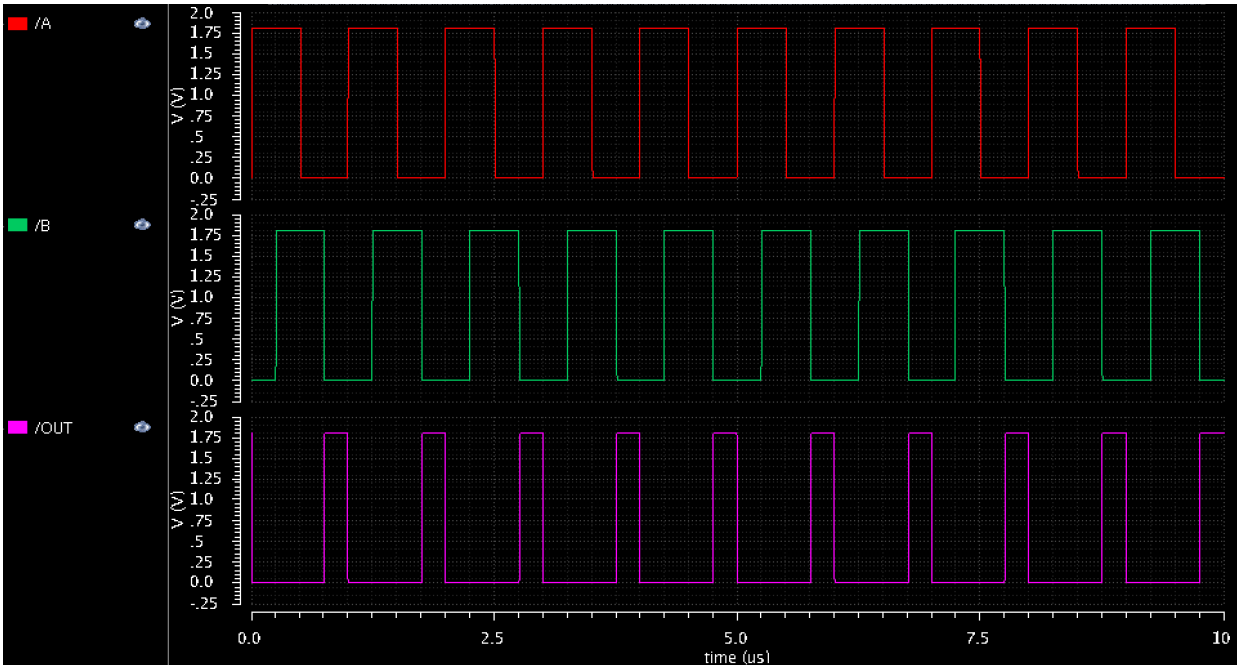


Fig. 4.22: Transient analysis for a minimum size two input CMOS NOR.

Fig. 4.23 shows the layout of the two inputs NOR. It is important to observe that also in this case the design is made trying to reduce the sizes and so overlapping the transistors.

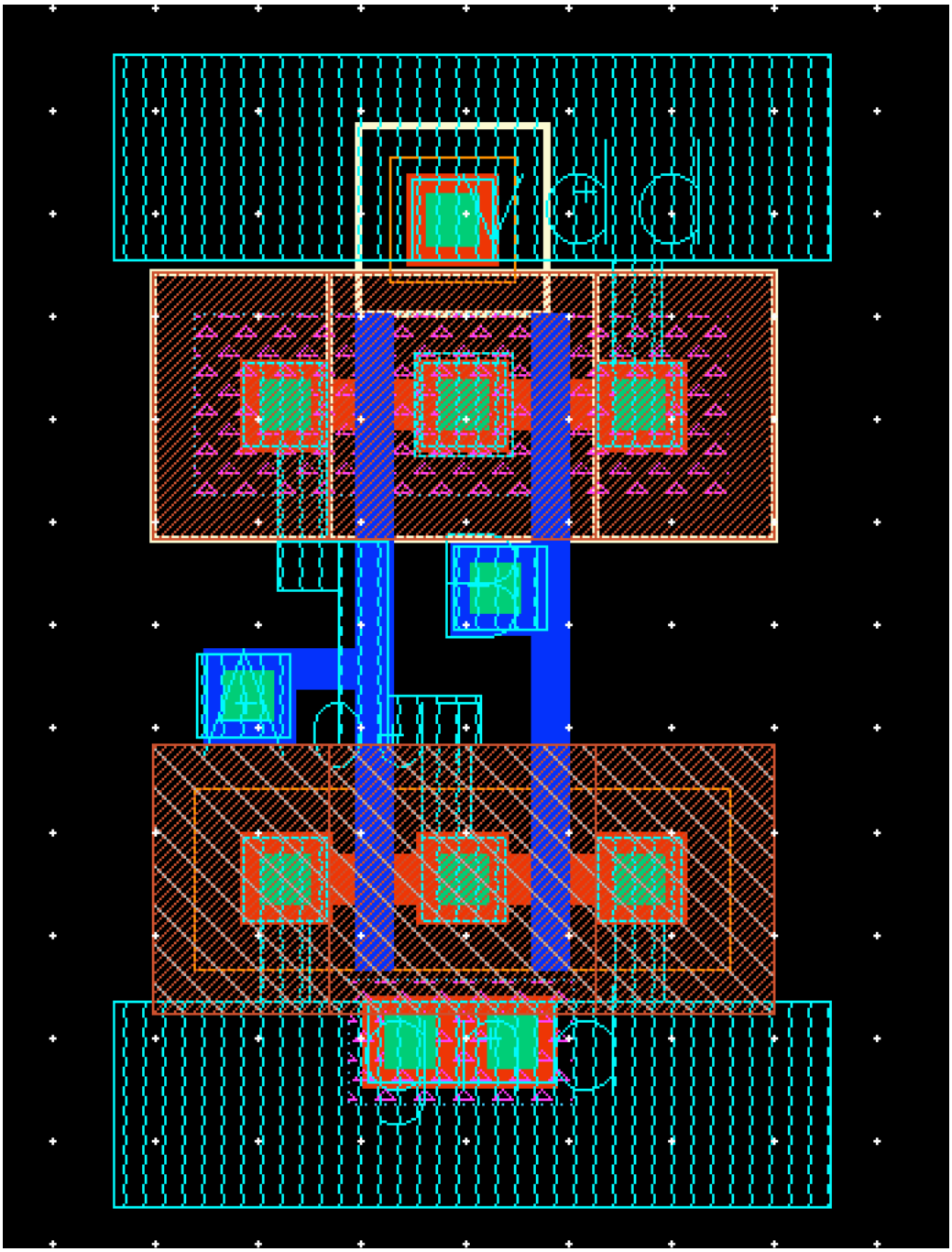


Fig. 4.23: NOR layout

By extracting the parasitic capacitances (Fig. 4.24) is possible to observe also in this case some small differences between the simulations pre and post-layout caused by the capacitors.

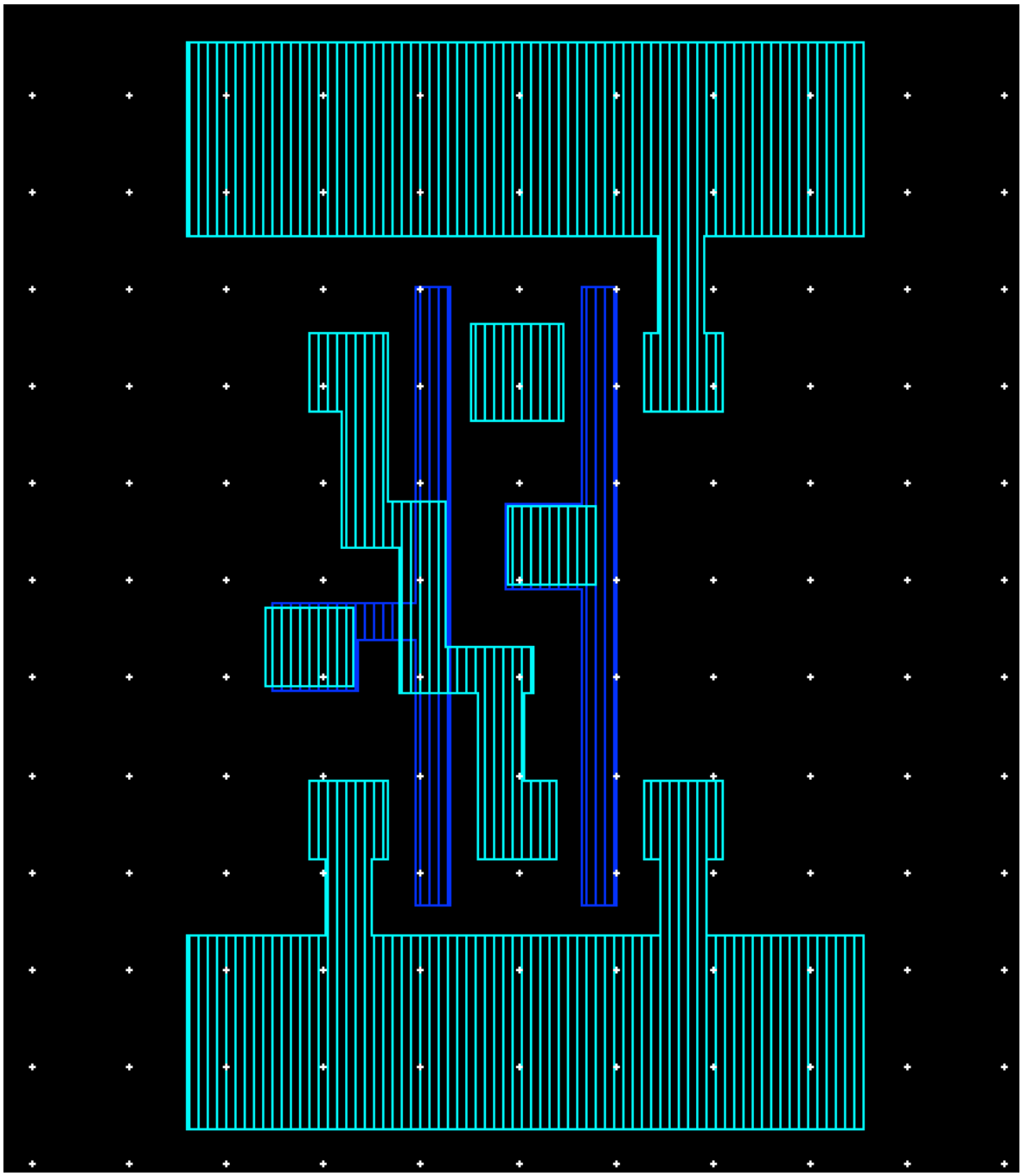


Fig. 4.24: Extracted view of a NOR.

4.2.5 OR

In order to design the OR, a simple combinational operation is performed. The output is so that of the NOR one but inverted indeed. In the Fig. 4.25 the schematic view is presented in a different form with respect to the AND one. In this case, I use the NOR and inverter already made instead of the transistors. Fig. 4.26 shows the symbol view.

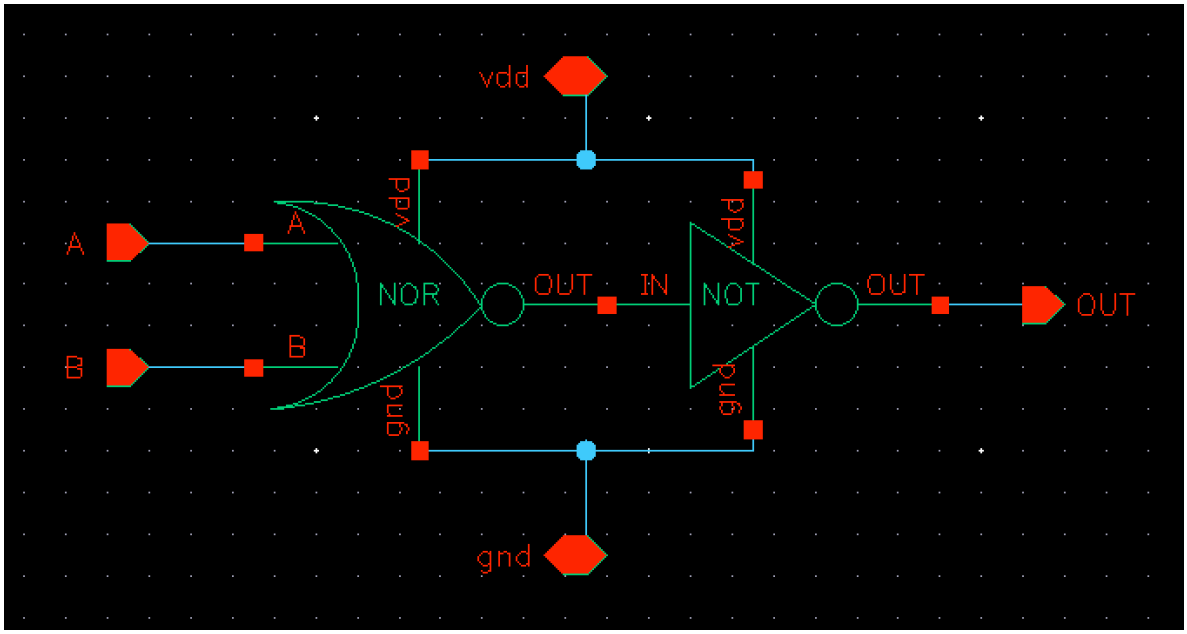


Fig. 4.25: OR schematic view.

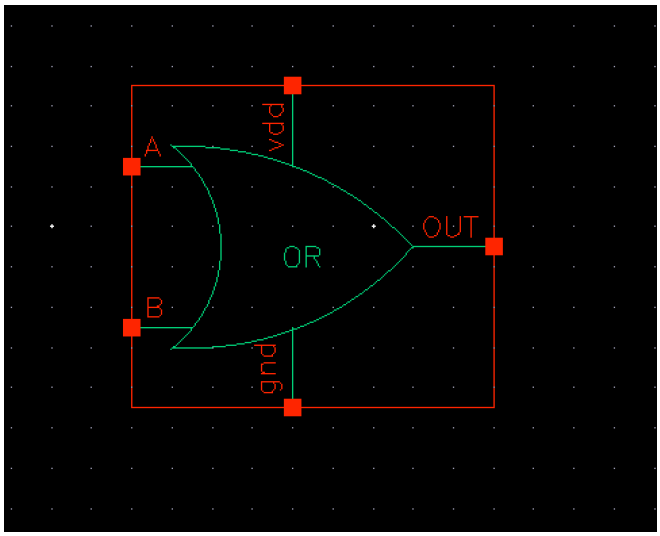


Fig. 4.26: OR symbol view.

Here, below, in the Fig. 4.27, the transient analysis of a simple two inputs OR is depicted using the same square waves used for the NOR simulation: the output is exactly the same of the NOR one but inverted indeed.

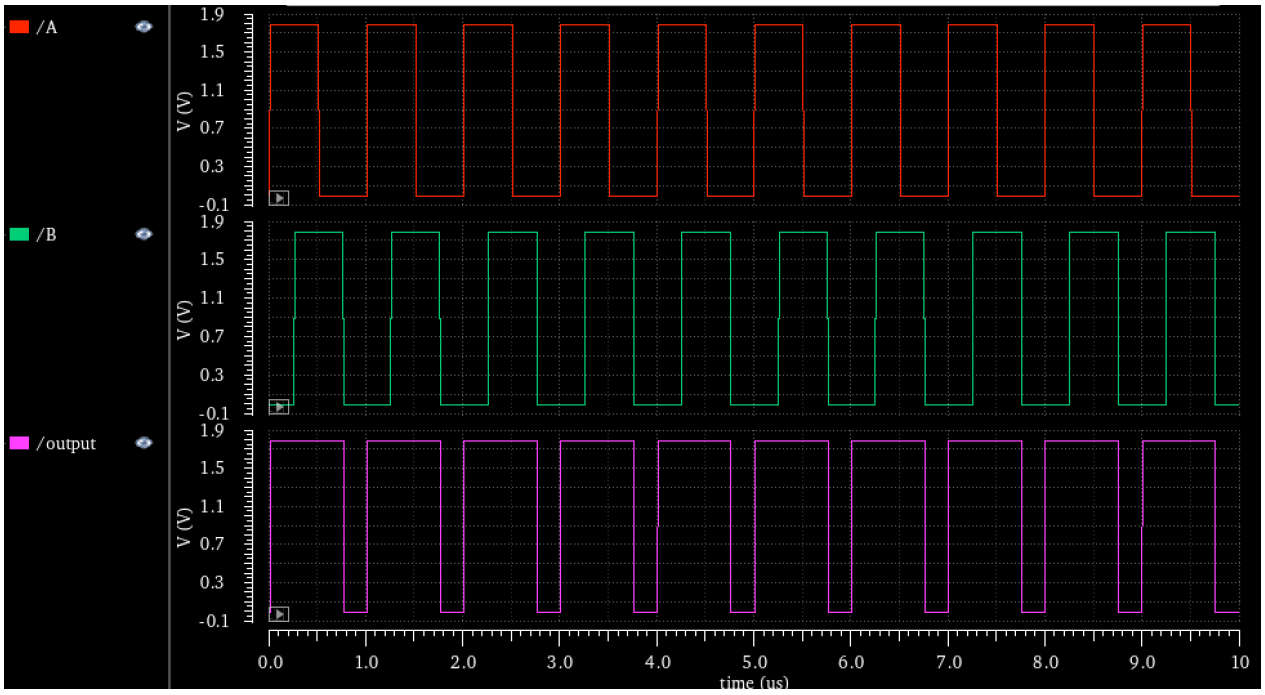


Fig. 4.27: Transient analysis for a minimum size two input CMOS OR.

The layout of the OR is presented in the Fig. 4.28 and the extracted view is shown in the next Fig. 4.29.

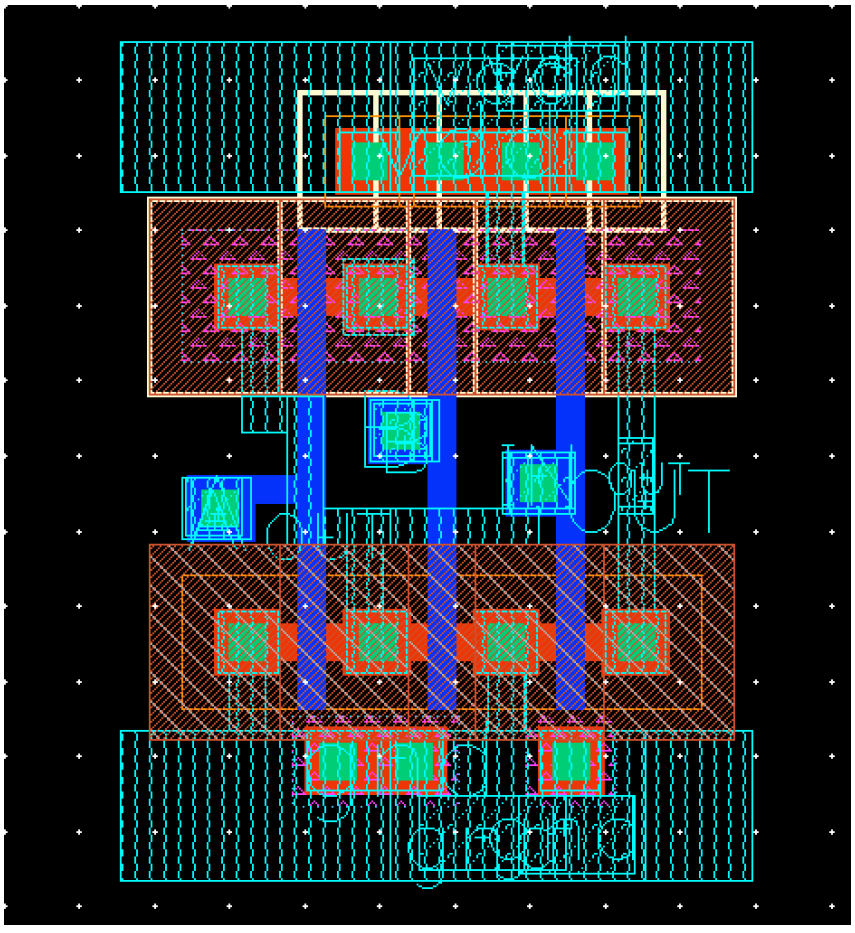


Fig. 4.28: OR layout.

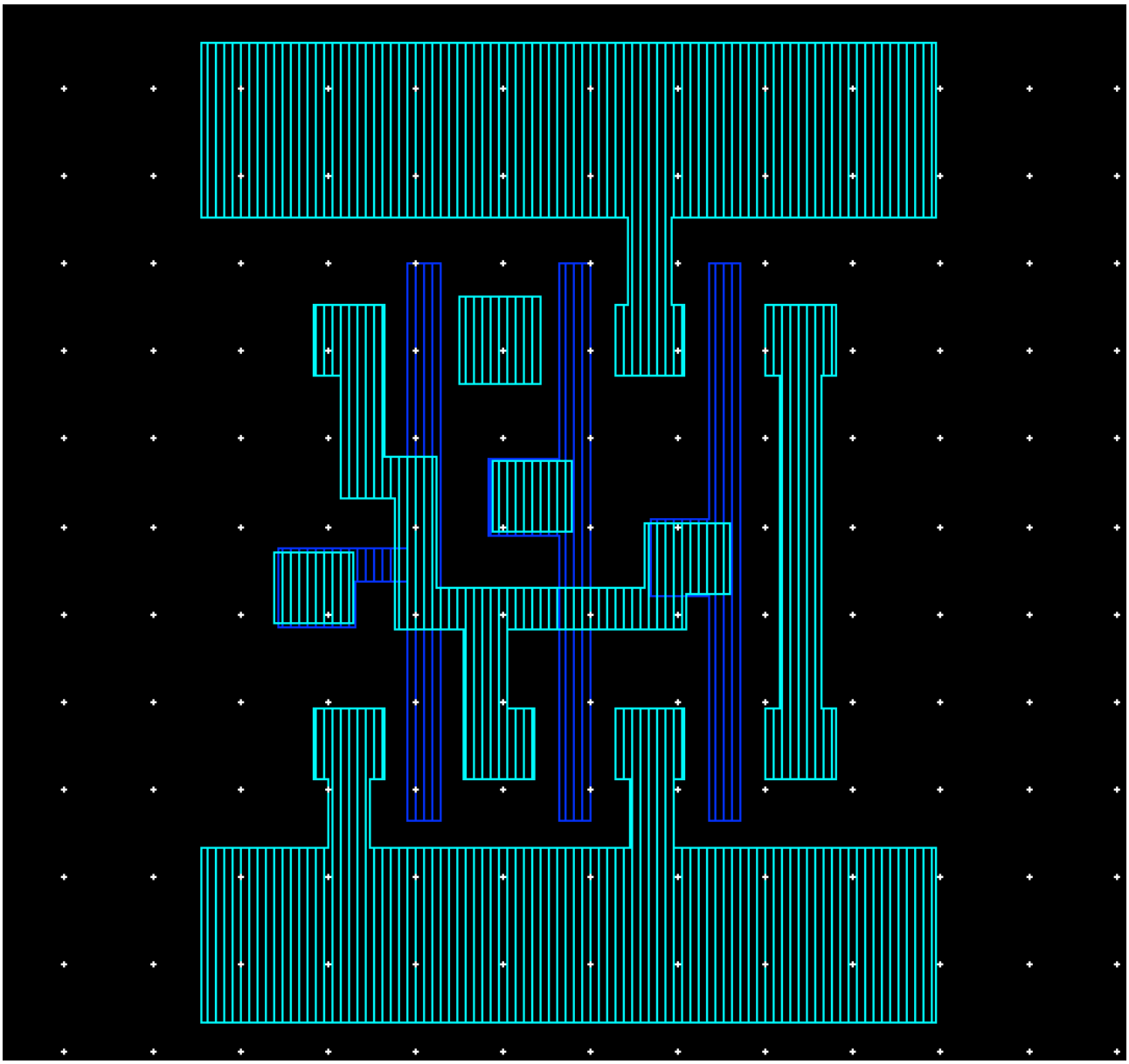


Fig. 4.29: Extracted view of an OR.

4.3 COMMUNICATION CIRCUIT DESIGN

The starting library is then completed with the previous components design and, therefore, it is possible to start the design of the proper communication circuit. The situation is the one described in the Fig. 4.30 below: the incoming wave is considered as a quasi-digital signal between 0 V (gnd) and 1.8 V (Vdd) with 10 µs period (100 kHz frequency) and duty cycle of 50%. The output of the circuit must be a digital signal that contain almost 3 bits for the digital word coming from the multiplexing layer to discriminate different types of extracted signals and almost 1 bit for the header in which the information of the synchronization with the rising edge of the incoming signal is stored.

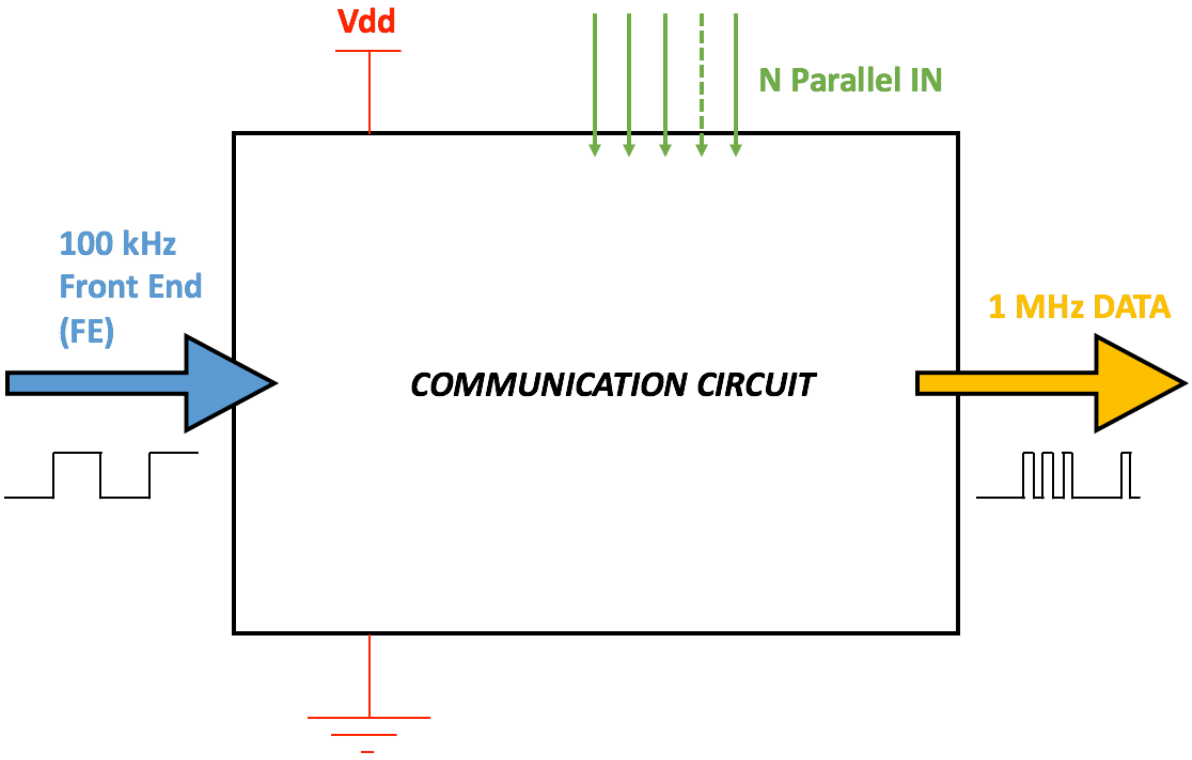


Fig. 4.30: Specification of the communication circuit.

The functioning of the system is very simple and clear: whenever a rising edge of the incoming quasi-digital signal is detected a train of pulses is generated accordingly to the digital word provided from the parallel inputs. The frequency of these pulses need to be chosen taking into consideration the electrical model of the transducer, the scattering model of the incident and reflected waves that hit the transducer from the external base station and the maximum number of bit that are important to transmit. In the hypothesis of a first scenario with a range of transmitted bits between 4 and 8, the frequency of the generated pulses is fixed around 1 MHz.
From these first consideration two elements are needed for sure into the communication circuit: a ring oscillator around 1 MHz and a Front-End monostable with the goal of recognize the rising edge of the incoming signal.
For what concern the word provided from the multiplexing layer (3 bits to discriminate the 5 different sensors mounted on the front-end layer), the simplest way to traduce it in a pulse series is to use a register, in particular a Parallel-Input-Serial-Output register (PISO). The register is triggered by the oscillator clock, while another circuit is needed. In this case, the PISO Input Conditioning is just a combinational circuit that triggers the writing and the shifting starting point of the register. This is fundamental since the serial word (output of the PISO) needs to be synchronized with the rising edge of the front-end signal.

At this point all the components of the circuit are presented as in Fig. 4.31 and now the generated signal (1 MHz data) need to modulate the impedance of the transducer in order to make the backscattering transmission method functioning.

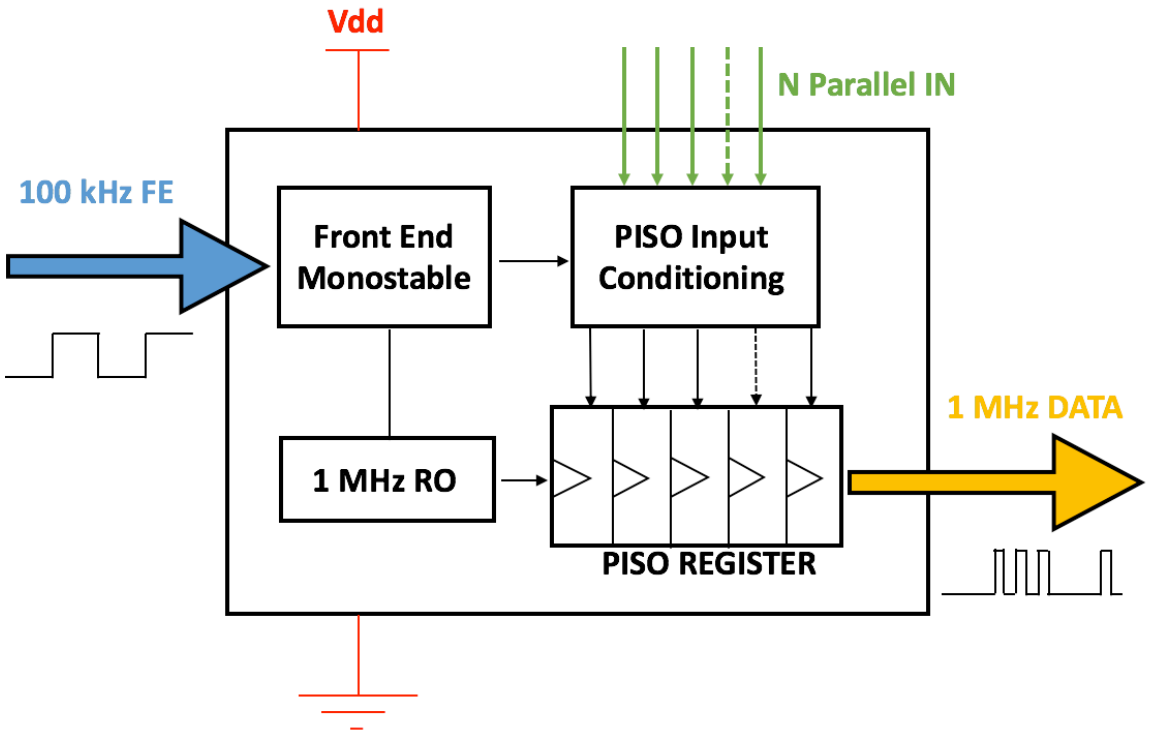


Fig. 4.31: Communication circuit main blocks.

I have already spoke about backscattering and wireless data transmission on Chapter 3 and, for here, the train of pulses generated by the proper circuit modulates the frequency of the opening and closing of a switch (simple transistor appropriately sized). The switch modulates the impedance of the sensor node (transducer), which ends with the variation of the reflected wave by the changing of the reflecting coefficient. In this way, an amplitude modulation ASK in performed (Fig. 4.32).

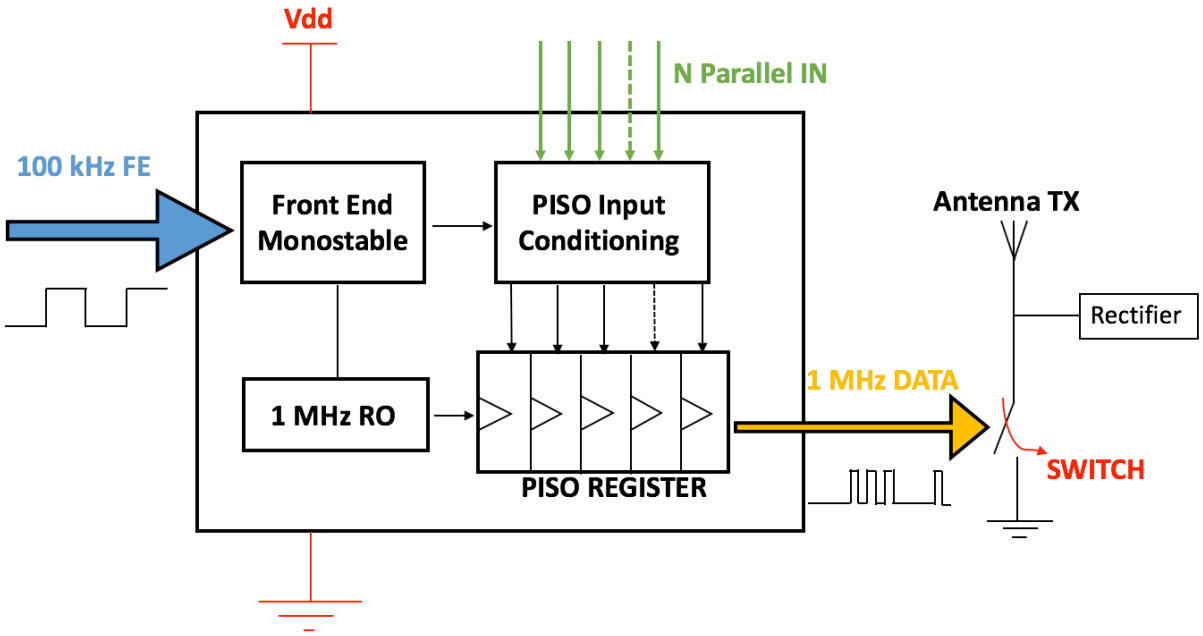


Fig. 4.32: Switch modulation of the communication circuit.

Summarizing:

- A train of pulses (at the RO frequency) is generated by the PISO register for each rising edge of the front-end signal.
- The pulses modulate the opening or closing of a switch that makes the final transducer in connection with the other parts of the circuit or short-cut it to ground.
- The switch modulates the impedance matching between the full-matched condition and the complete mismatched condition, enabling data transmission outside the body.
- The impedance modulation ends with the modification on the reflection coefficient of the system.
- The reflected wave is also modulated in amplitude.
- It is simple to translate this amplitude modulation in a bit address in the external base-station.
- Measuring the distance (in μs) between two equal digital words (silence time or "0 time") the frequency as emerging from the front-end signal is detected.
- Knowing the relationship between frequency and current (current to frequency converter is used in the extraction phase) and the sensitivity of the sensor, it is possible to calculate the concentration of the monitored molecules (glucose, lactate, glutamate, drugs, ...).

The following sections are made in order to describe in detail all the parts of the transmission circuit as per the block diagram in Fig. 4.32.

4.3.1 RING OSCILLATOR

In literature there are several models of RO (Ring Oscillator) for low frequencies oscillations, while for the specific applications discussed here I modeled a new type of oscillating-ring by merging different typologies since specific constrains on both power and size need to be considered. Fig. 4.33 presents the simplest possible three stages ring oscillator.

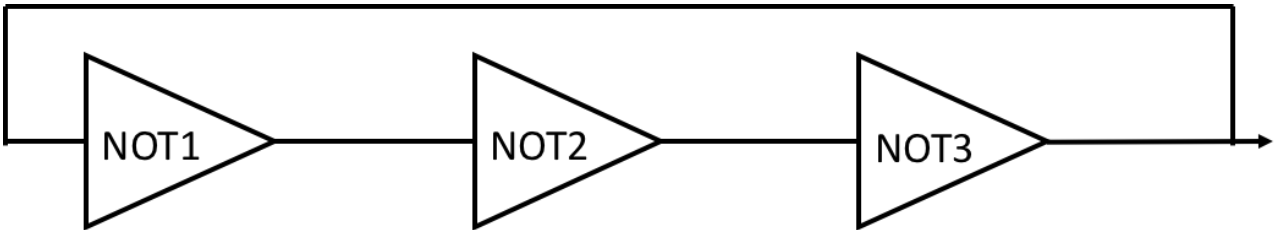


Fig. 4.33: Three stages ring oscillator.

The generated frequency can be approximated by the following equation 4.8:

$$f = \frac{I}{N * C_{tot} * V_{dd}} \tag{4.9}$$

where: N is the number of the ring stages, C_{tot} is the overall capacitance over every stage, V_{dd} is the voltage supply provided to the ring and I is the flowing current.
With this kind of ring the obtained oscillation frequency is the one simulated in the following Fig. 4.34.

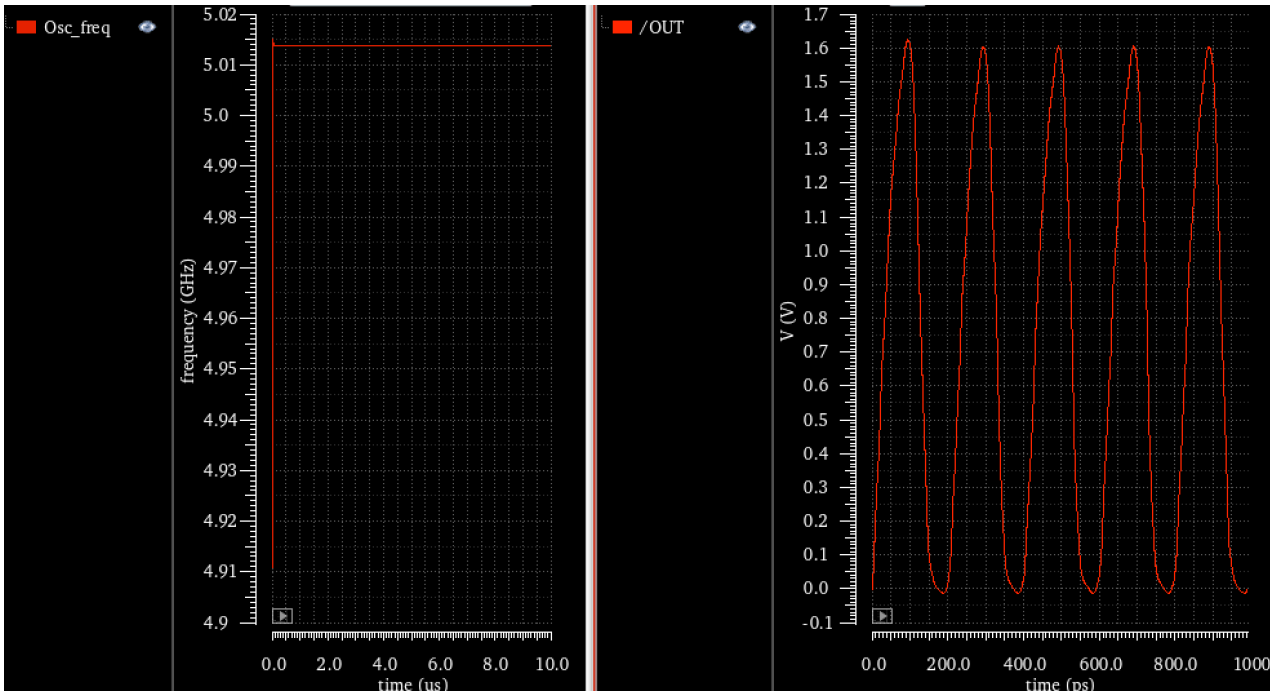


Fig. 4.34: Transient simulation with three stages simple ring oscillator at 5 GHz frequency.

Several strategies can be applied to decrease the oscillation frequency. In particular, there are four parameters in equation (4.8) on which can operate:

- V_{dd}: to increase the voltage supply is not a good idea, on the contrary there are several articles in which V_{dd} is deliberately decreased in order to reduce the power consumption [4.2]. Is important to remember that the power consumption is linear dependent with the voltage supply ($P = V * I$).
- N: is possible to decrease the frequency simply by increasing the number of stages. The question now is: how many stages are needed in order reach the volute oscillation? Too much.
- I: to limit the current flowing into the inverter is a valid solution. Also in literature, this idea is applied through different current limitation methods [4.3].
- C_{tot}: the simplest way is to increase the overall capacitance by adding capacitor at every output stage.

The configuration of a ring oscillator like the one in Fig. 4.33 may be implemented as shown in Fig. 4.35: three inverter stages with three capacitors C.

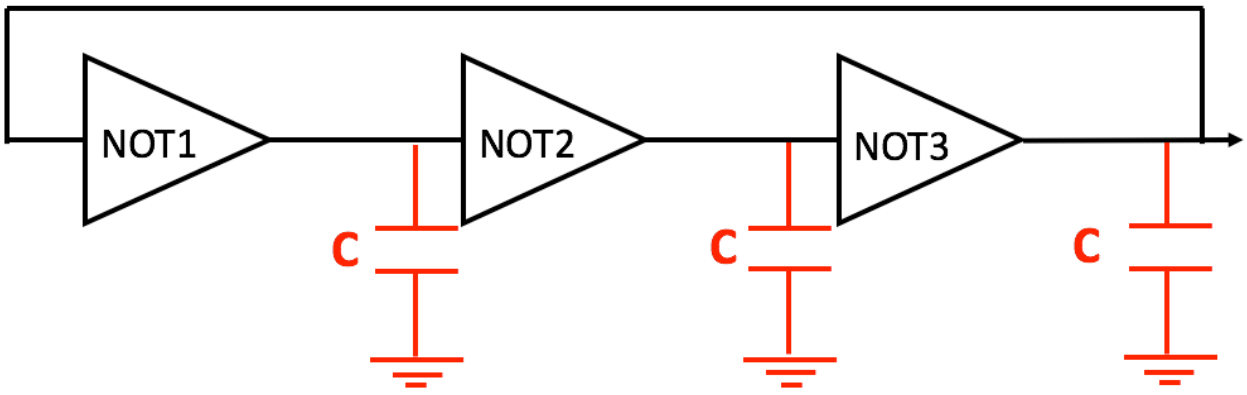


Fig. 4.35: Three stages RO with capacitors.

In order to understand the order of magnitude of the capacitance required to reduce the oscillation frequency, I have implemented sweep capacitances in the schematic in Fig. 4.36 by obtaining the result in Fig. 4.37.

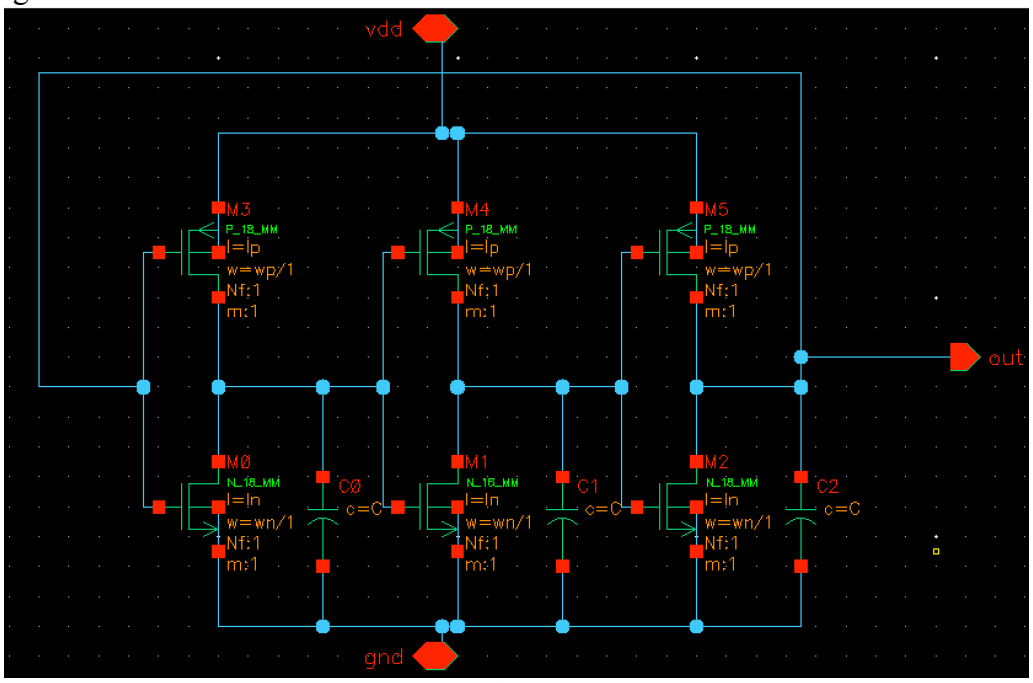


Fig. 4.36: Schematic RO view.

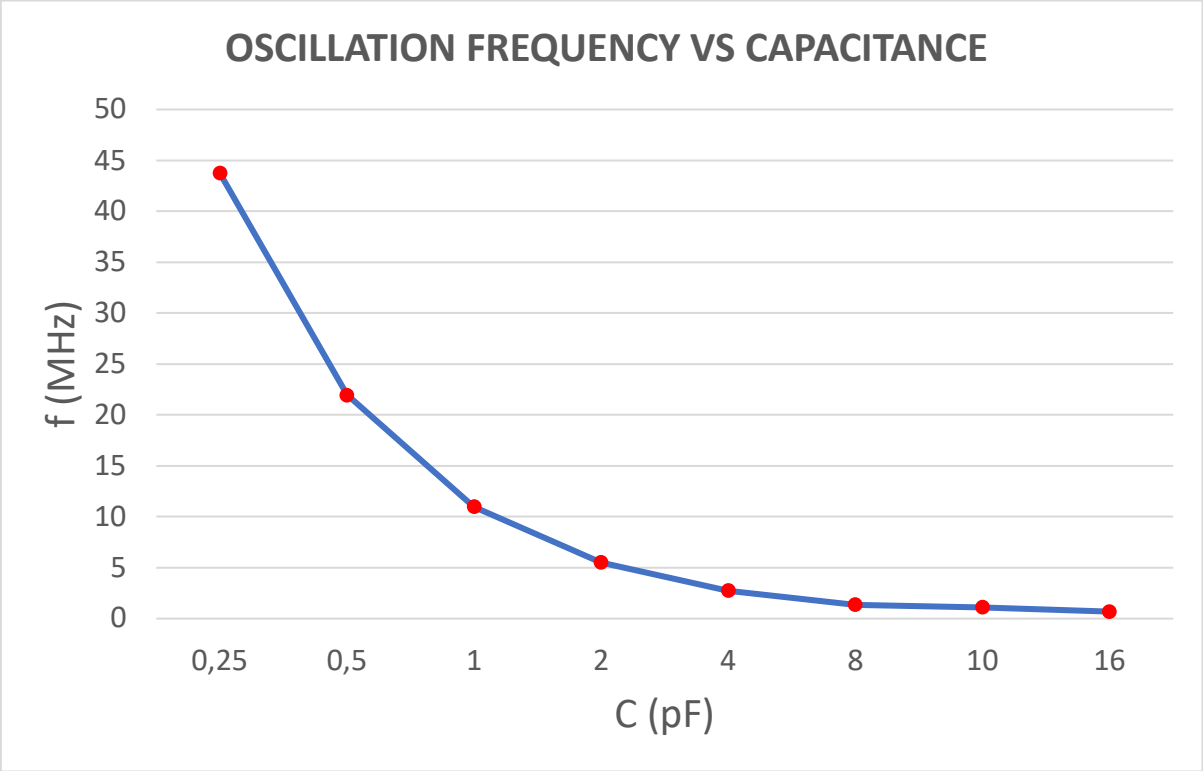


Fig. 4.37: Capacitance VS ring oscillation frequency.

As the graphic shows very well, a 10 pF capacitance is needed in order to generate a 1 MHz frequency. However, a capacitor of 10 pF takes up to 10 x1000 μm^2!
In reality there is another possibility: to combine the capacitive effect with a starved configuration [4.3] of other two transistors (gate connected with drain) used as a current limiter (Fig. 4.38).

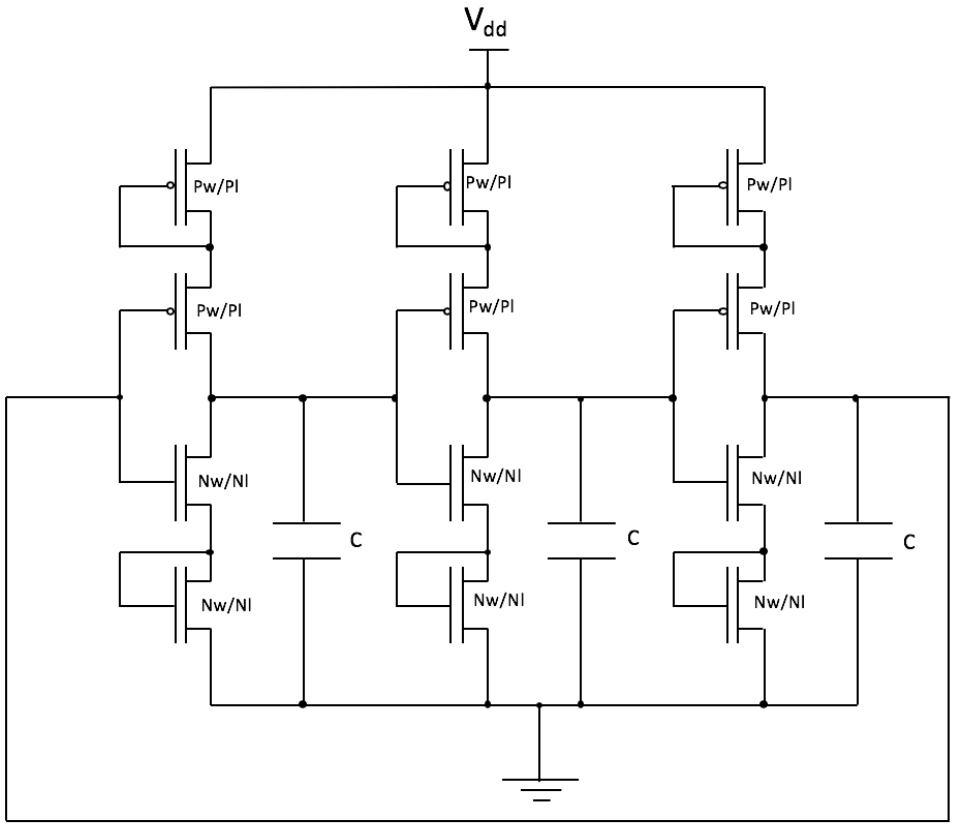


Fig. 4.38: Starved configuration of three stages ring oscillator.

Now, if I repeat the same simulation than before but using the above-reported configuration, with the minimum size transistors, the result is now as shown in Fig. 4.39.

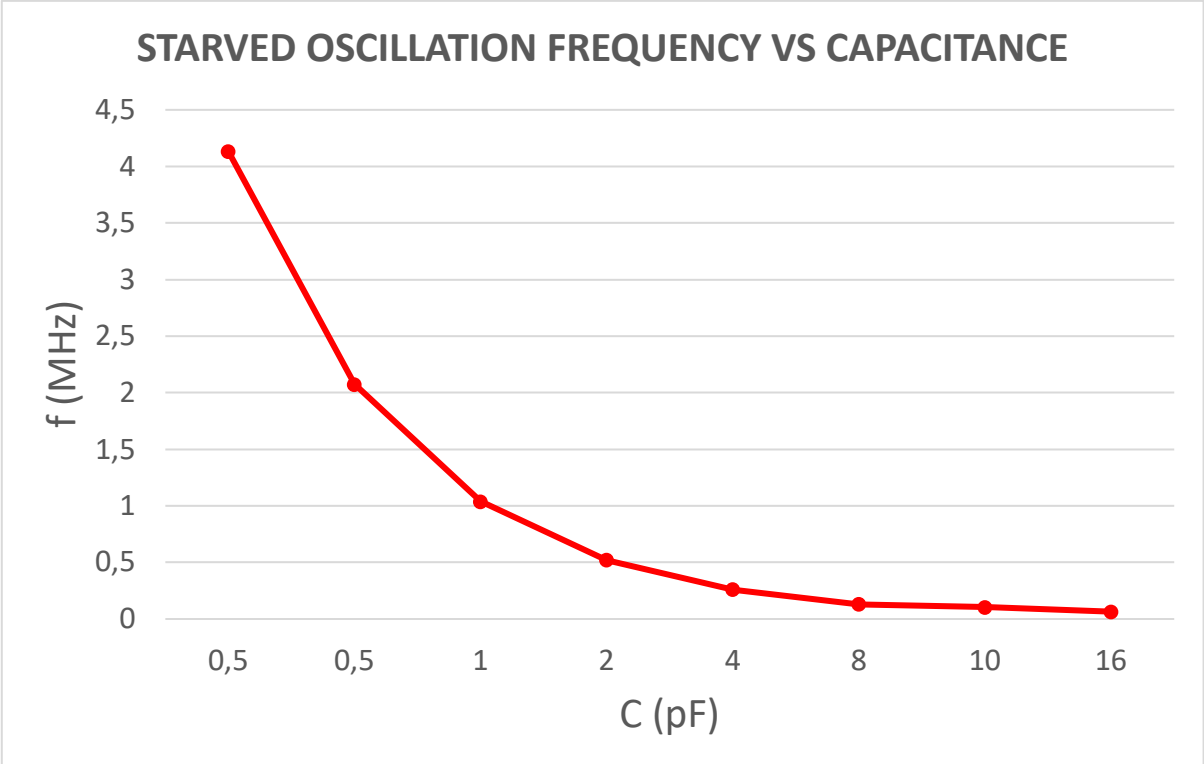


Fig. 4.39: Capacitance VS ring oscillation frequency in a starved configuration three stages ring.

Comparing the two graphs is simple to deduce that now the capacitance needed in order to have almost 1 MHz oscillation is decreased from 10 pF to 1pF and so the sizes of the capacitors are also reduced of a factor 10. This strategy is not sufficient because the occupied area is still too large: another well-known configuration to be considered is the one in which resistances are connected at every output stage in order to decrease the current and, thus, the oscillation frequency (Fig. 4.40).

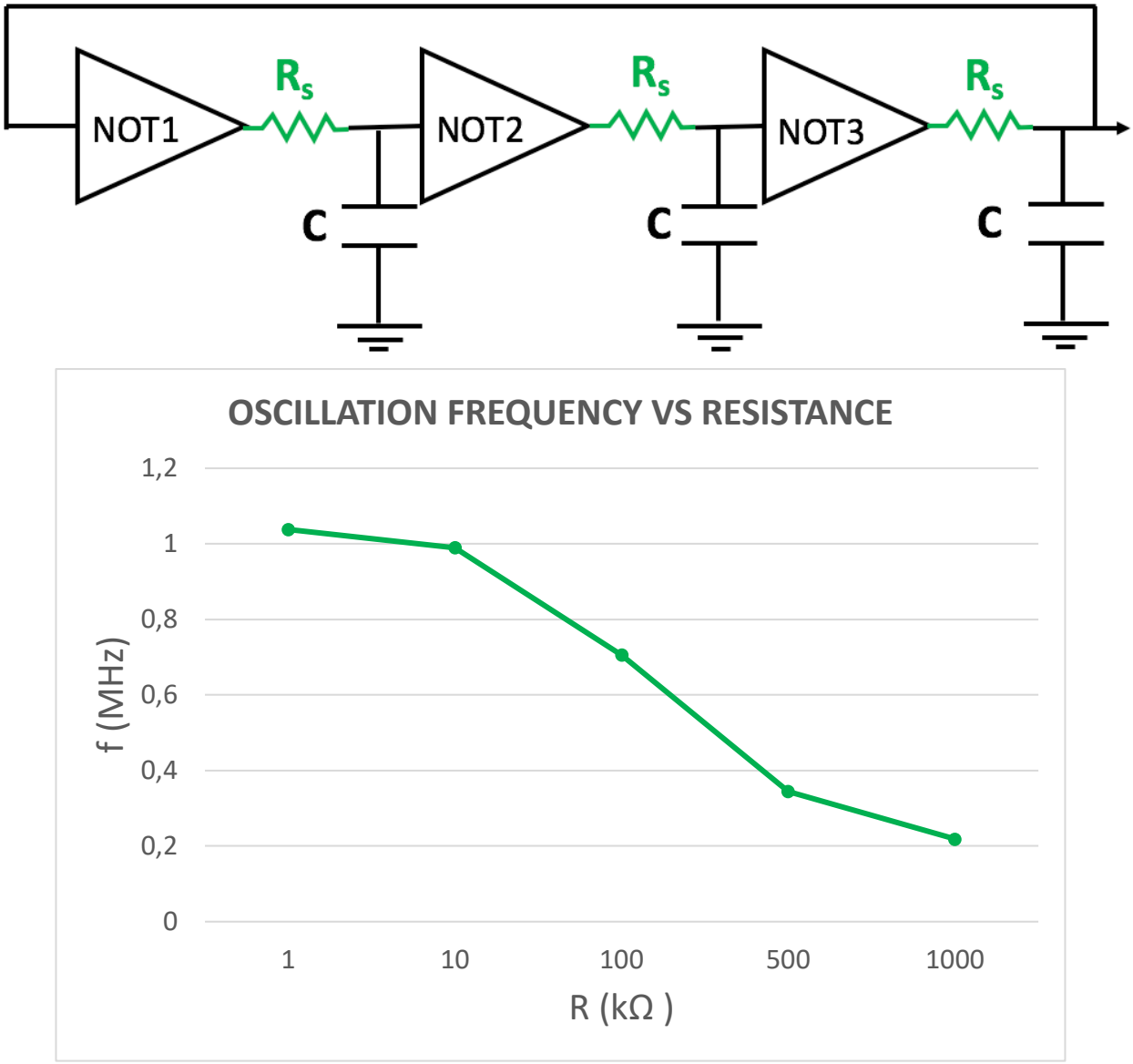
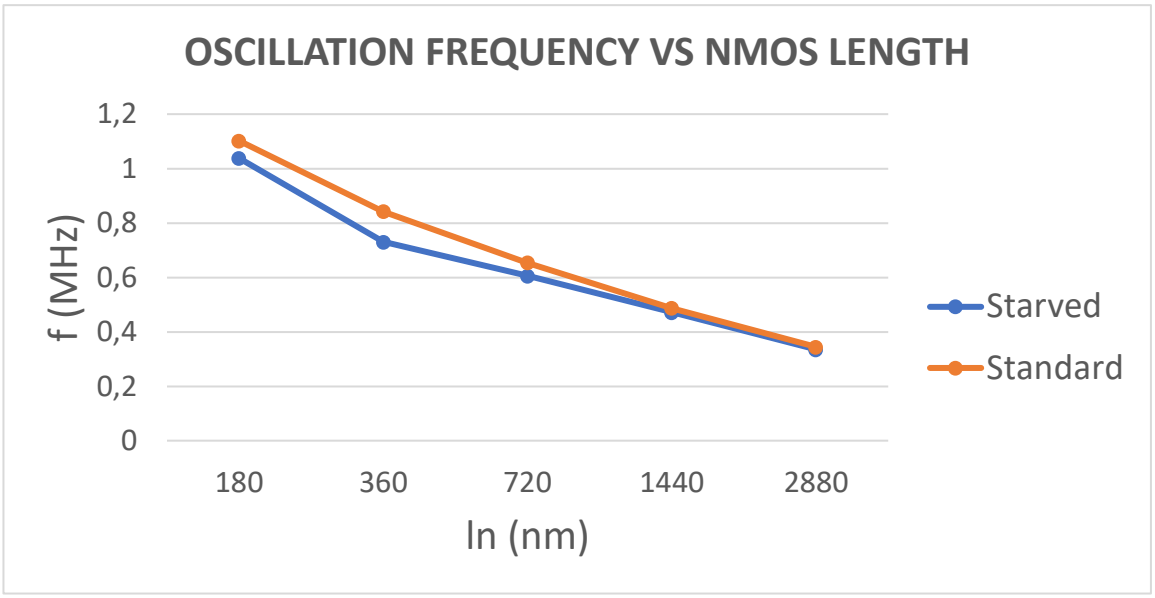


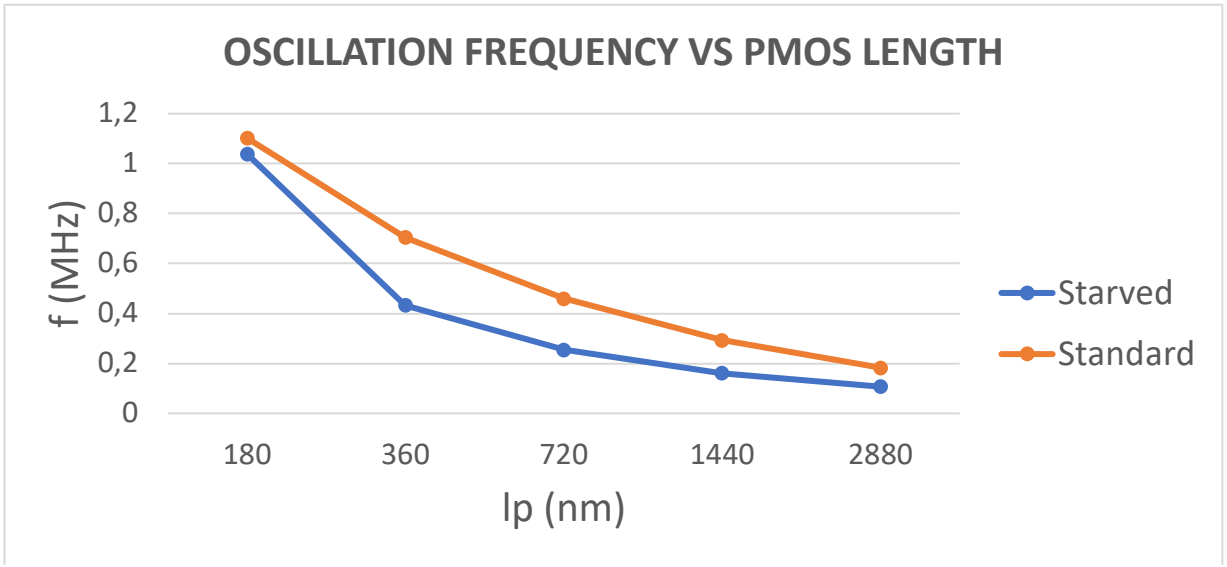
Fig. 4.40: Resistance VS ring oscillation frequency (bottom) in a simple three stages ring (top).

As the graphic shows, high resistance values are needed in order to decrease the frequency: again, the problem is on the sizes! I am trying to reduce the capacitance value in order to reduce the sizes: applying series resistors is not a good solution because the resistors now take the area spared by the smaller capacitance.

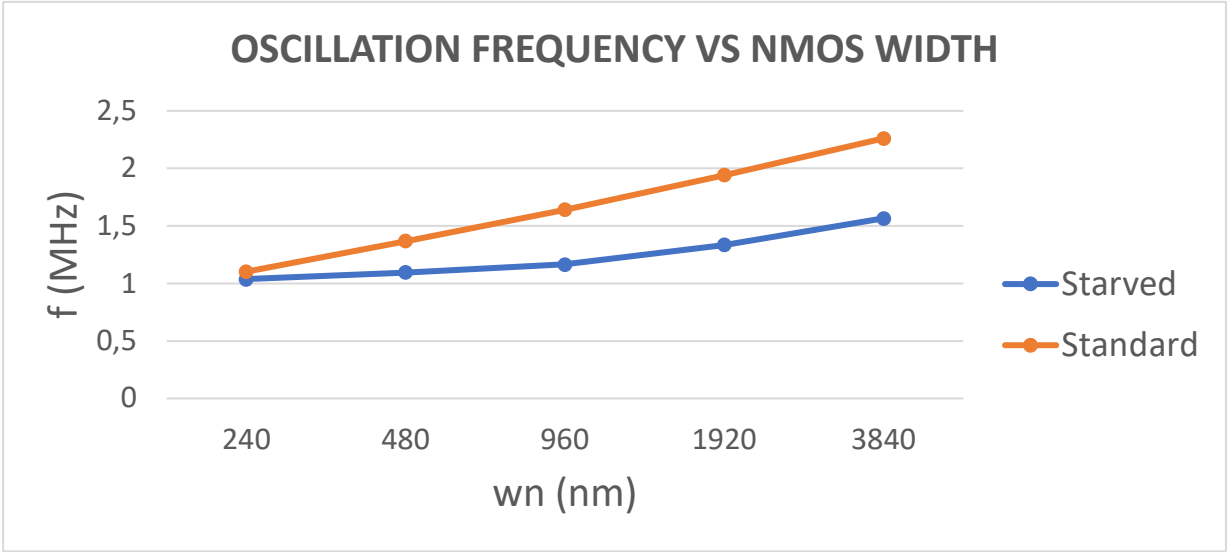
There is also another choice: to exploit the proper sizes of the transistors used in the starved configuration. In particular a long and thin transistor (pass transistor) behaves like a resistance. Under this hypothesis, the frequency is analyzed in the following graphs by sweeping the proper parameters in case of transistors (both PMOS and NMOS). In the Fig. 4.41 below the simple three stages configuration ring is compared with the starved one changing sizes of the transistors.


OSCILLATION FREQUENCY VS NMOS LENGTH
f (MHz)
1,2
1
0,8
0,6
0,4
0,2
0
180
360
720
1440
2880
ln (nm)
Starved
Standard

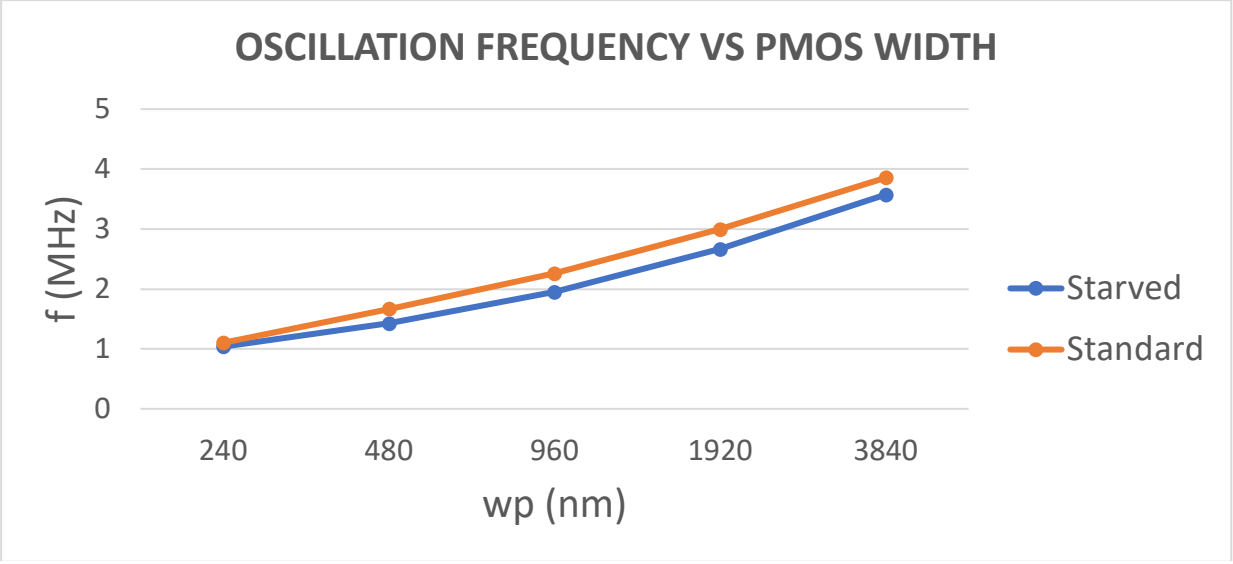
(A)


OSCILLATION FREQUENCY VS PMOS LENGTH
f (MHz)
1,2
1
0,8
0,6
0,4
0,2
0
180
360
720
1440
2880
lp (nm)
Starved
Standard

(B)


OSCILLATION FREQUENCY VS NMOS WIDTH
f (MHz)
2,5
2
1,5
1
0,5
0
240
480
960
1920
3840
wn (nm)
Starved
Standard

(C)



(D)

Fig. 4.41: Oscillation frequency of both simple (orange) and starved (blue) configurations VS transistors sizes: NMOS length (A), PMOS length (B), NMOS width (C) and PMOS width (D).

As expected, the best configuration to reduce the oscillation frequency is that with transistors used like resistances (current limitation with pass transistor) and so long and thin channels. In order to design the proper starved ring oscillator (SRO), the minimum width of both NMOS and PMOS transistors is chose (240 nm) and the other parameters are changed in order to find almost a 1 MHz oscillation without using big capacitors in terms of sizes. The final circuit is shown in Fig. 4.42 with both NMOS and PMOS being 360 nm in length and 240 nm in width while the three capacitors have a capacitance of only 200 fF.
By increasing the length of the transistors is possible to reduce the capacitance accordingly, but, as a matter of fact, the total area improvement is less than 10 %. Further, this would negatively affect the SRO performance reliability, in particular by making the oscillation frequency highly dependent on parasitic capacitance. After simulating different trade-off in this regard, I deemed the proposed design a safe and good solution.

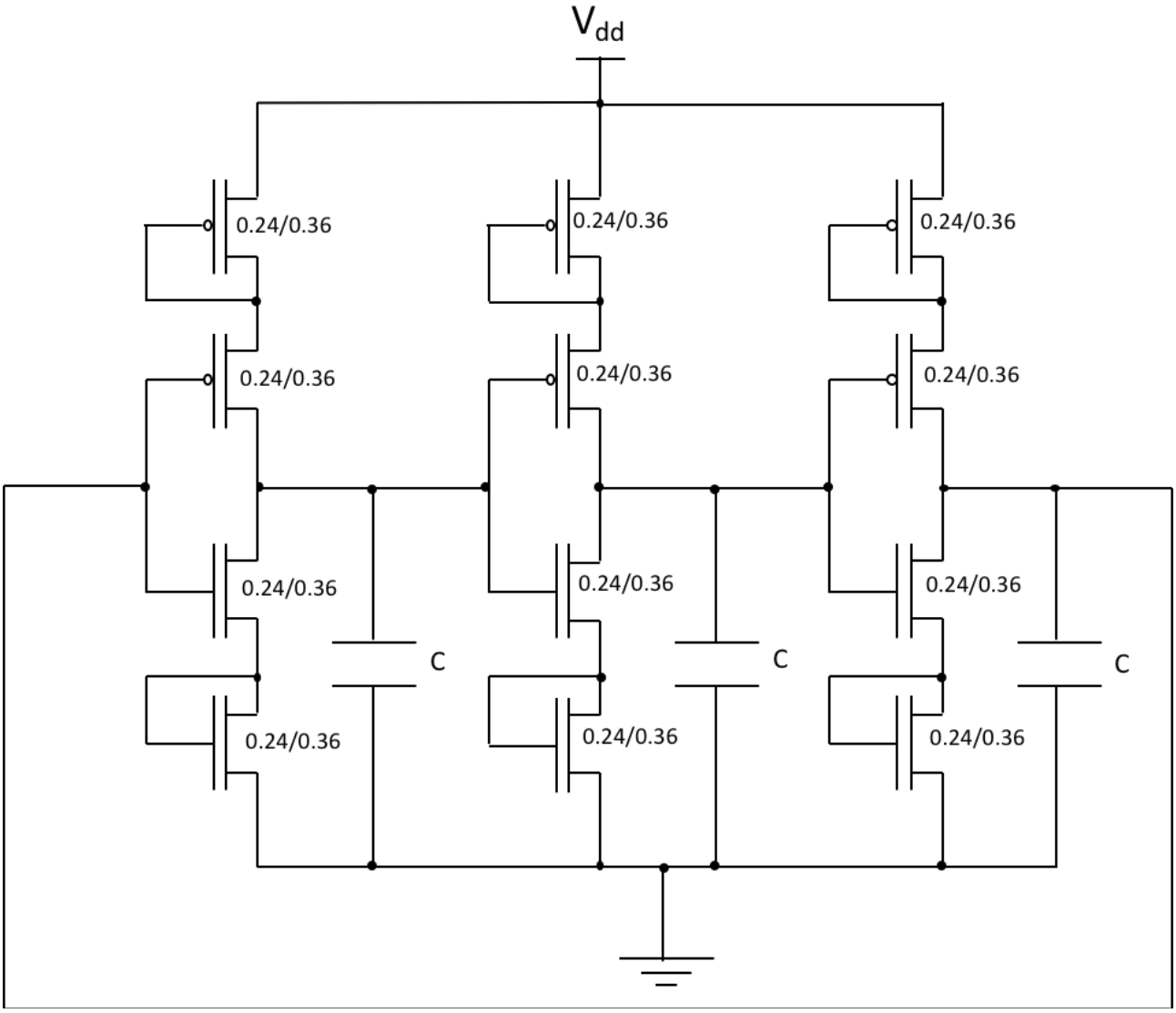


Fig. 4.42: Final configuration of 1 MHz starved ring oscillator.

Finally, Fig. 4.43 presents the outputs in testing the above configuration for the ring oscillator.

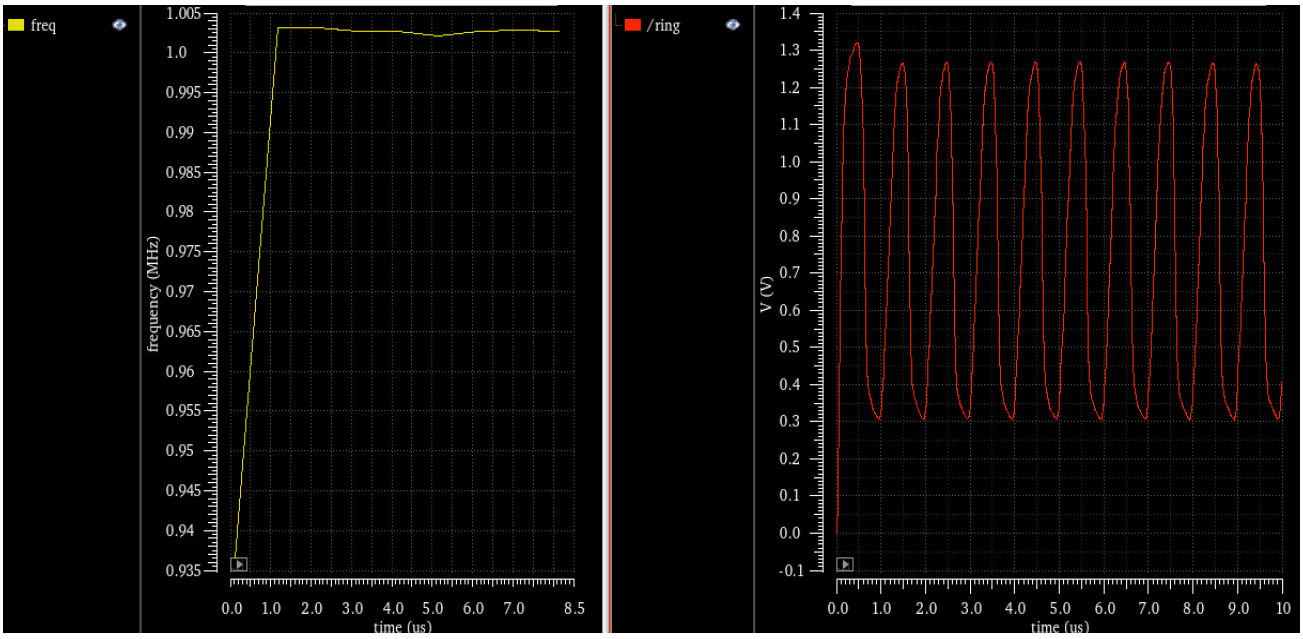


Fig. 4.43: Transient simulation with three stages starved ring oscillator at almost 1 MHz frequency.

Comparing this simulation with that obtained with the simple three-stage ring oscillator (Fig. 4.34), it worth to note that, even though both the rings are powered with 1.8V as a voltage supply, the last simulation does not provide neither an upper nor a lower limits in the oscillations close to 1.8V or 0V, while the previous does. Here, the limits are instead 1.25 V (higher) and 300 mV (lower). This output is undesirable but necessary because, as I am using pass transistor as resistance, the core of the ring does not have all the current available before (I limit its flowing by starving) and so the amplitude of the oscillation results reduced. This is not a big problem, but it is important to take it into consideration for the designing of the next components and, in particular, because the output of the ring oscillator is used as a clock for the PISO register.
Other issues arise about the post-layout simulations since the presence of three capacitors, considering that the parasitic components are not negligible. It is simple to imagine that most of the parasitic capacitances are located, in the ring, between the connection by the output of one stage to the input of the following one (Fig. 4.44).

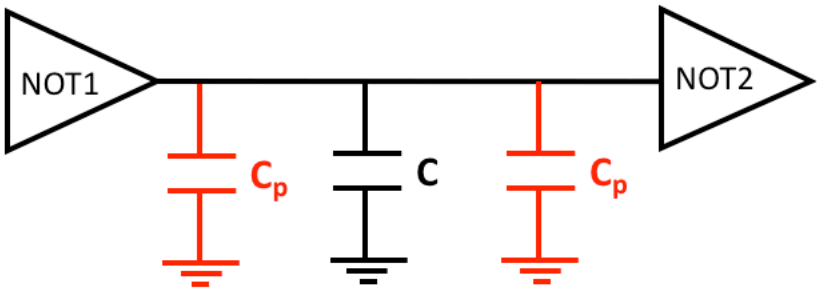


Fig. 4.44: First stage model of parasitic capacitance in ring oscillator.

Following the equation 4.9 below, it is possible to estimate the C_p values and to make some consideration about the post-layout simulation circuit.

$$C_{p_{tot}} = 2 * C_p = 2 * \frac{2}{3} C_{ox} WL \tag{4.10}$$

In which C_{ox} is the capacitance per area provided by the used CMOS technology, usually equal to $8 \frac{fF}{\mu m^2}$. Imaging now an area (WL) of 1 μm^2 for the total parasitic capacitance, we have about 11fF.

This capacitance is in parallel with the real capacitance C (200fF) and so, what is expected from the post-layout simulations is that the parasitic capacitance influences the oscillation of the ring for a 5.5%. Fig. 4.45 below presents the final layout of the starved ring.

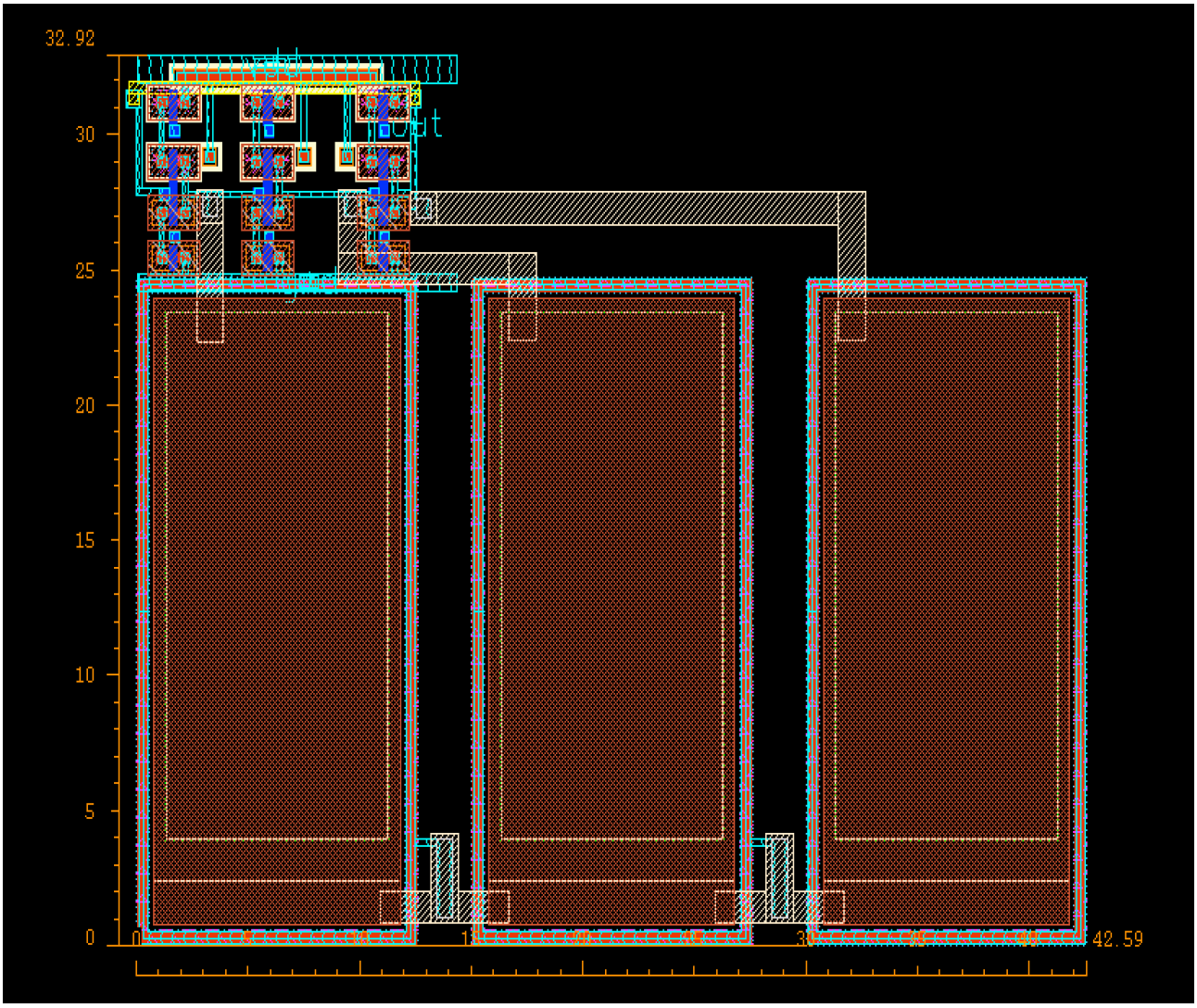


Fig. 4.45: Starved ring oscillator layout.

As evident, the large majority of the design area is occupied by the three capacitors (40x25 μm^2).

As expected, post-layout simulations, as compared with the original design (cfr. Fig. 4.46) shows a reduction of the oscillation frequency, as per the consideration made above about parasitic capacitances in between the ring' stages.

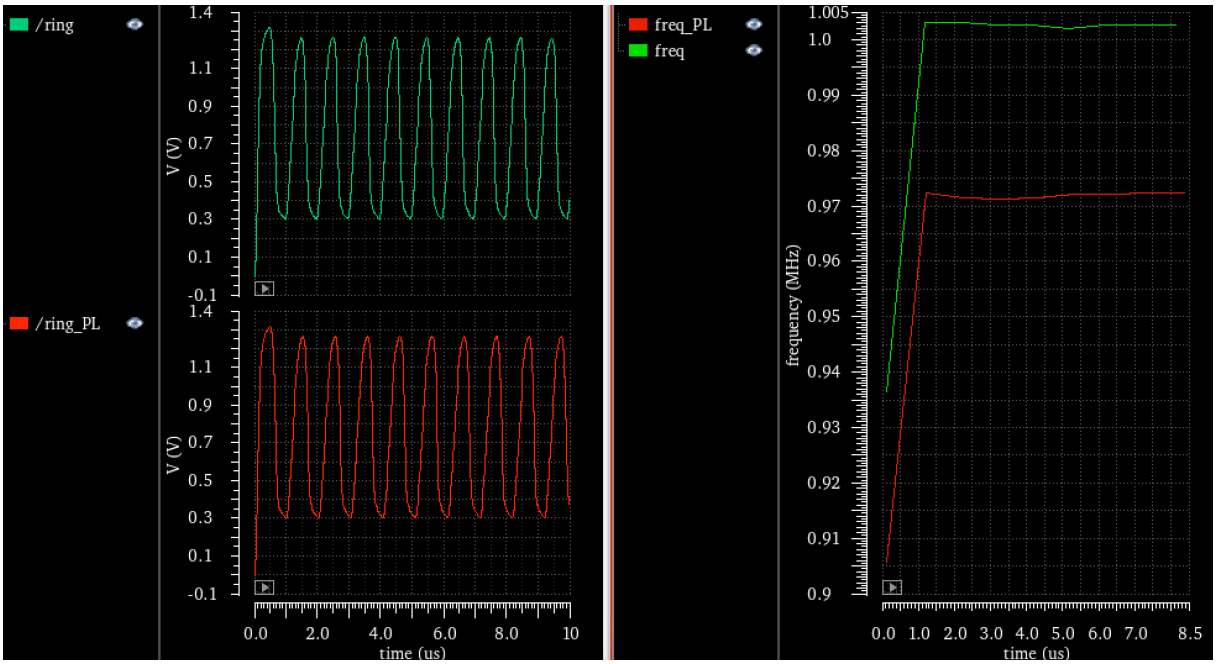


Fig. 4.46: Transient simulation comparing schematic (green) and post-layout (red) starved ring oscillator.

Post-layout simulations show here a reduction of the frequency in the order of 3.2%. The percentage of decreasing is smaller than the calculated one because, obviously, the area is not exactly 1 μm^2. This post-layout oscillation frequency is acceptable, even if slightly reduced, since the result is good any way for the aim of the work.

Finally, the power consumption of the entire ring is another critical since it is supposed to operate under power transfer condition by exploiting collection of energy by a micro-coil. A simple operation is then performed in order to estimate the average of the dynamic power among the duration of the simulation. The value obtained by the simulations is around 9.5 μW.

Targeting in-body applications, another important parameter is the sweeping of temperature. All the simulations done are made at 47°C as a reference temperature while the chip will operate indeed into the body at a temperature oscillating between 35°C and 40°C. In the following Fig. 4.47 the temperature sweep is simulated testing the ring from 27°C to 47°C .

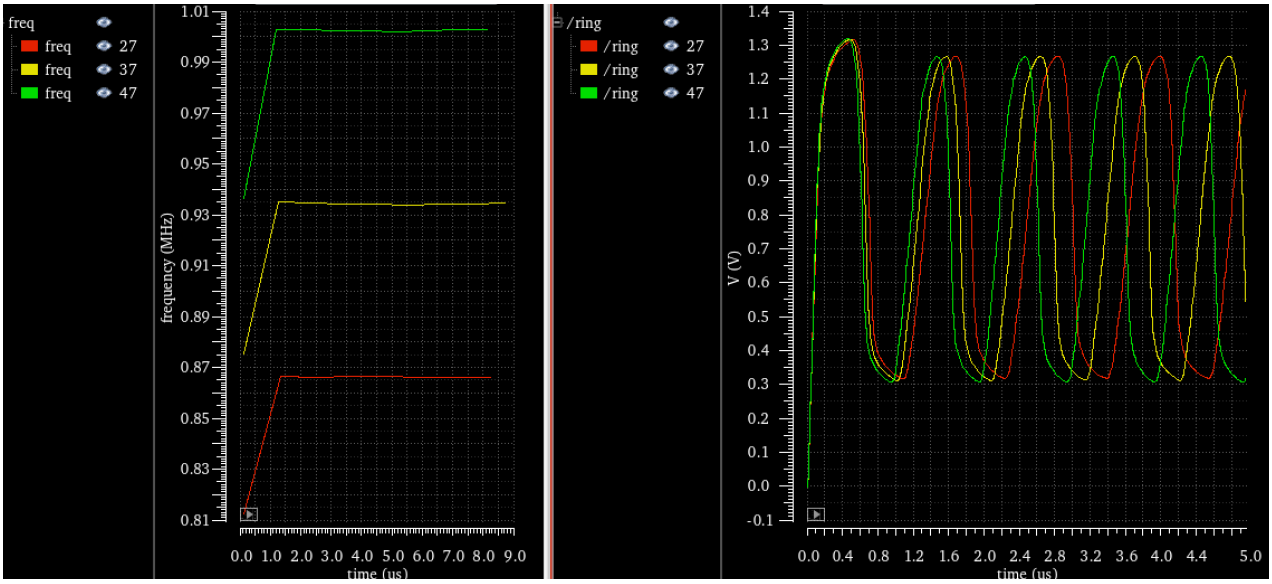


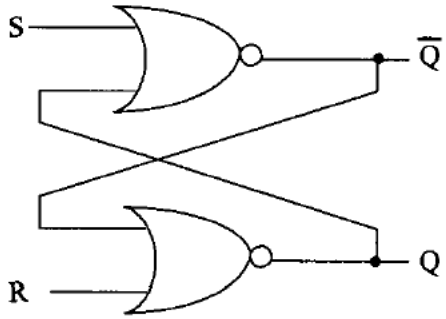
Fig. 4.47: Frequency shifts of the ring VS temperature sweeping between 27°C and 47°C.

4.3.2 PISO REGISTER

As the literature suggests [4.4], the simplest way to design a register is to use flip-flop (FF). The idea is to connect subsequently N flip-flops in order to be able to shift the digital word every rising edge of the clock. Flip-flop is a bi-stable memory element and it is the starting point for every circuit that need to dynamically store data with low space and ultra-low power consumption [4.1].
Before going in details on the PISO register, the typical flip-flop needs to be introduced first.

4.3.2.1 FLIP-FLOP SET RESET

A simple memory element is the two inputs SET-RESET flip-flop. It is simply made through two NOR gate, it has two outputs (in which one is the inverted of the other) and the truth table is the one described in the following Fig. 4.48.



Truth table

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

Fig. 4.48: Set-reset latch made using NOR gates (left) and truth table (right). [4.1]

The first condition of the truth table is the memory one: when both inputs are set to 0 the outputs maintain their logical states. The last condition is forbidden while the other two are commands conditions. Schematic and symbol views of this simple FF are shown in the next Fig. 4.49.

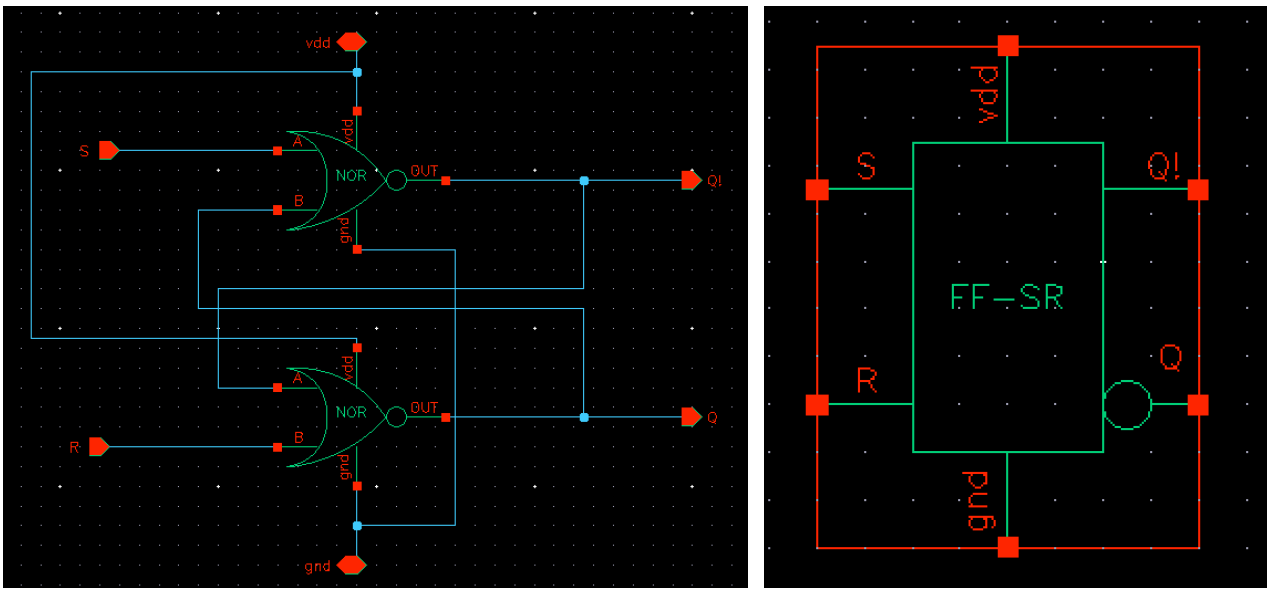


Fig. 4.49: Set-reset latch schematic (left) and symbol (right) views.

The functioning of the circuit above is simulated through a transient analysis and the result is shown in Fig. 4.50.

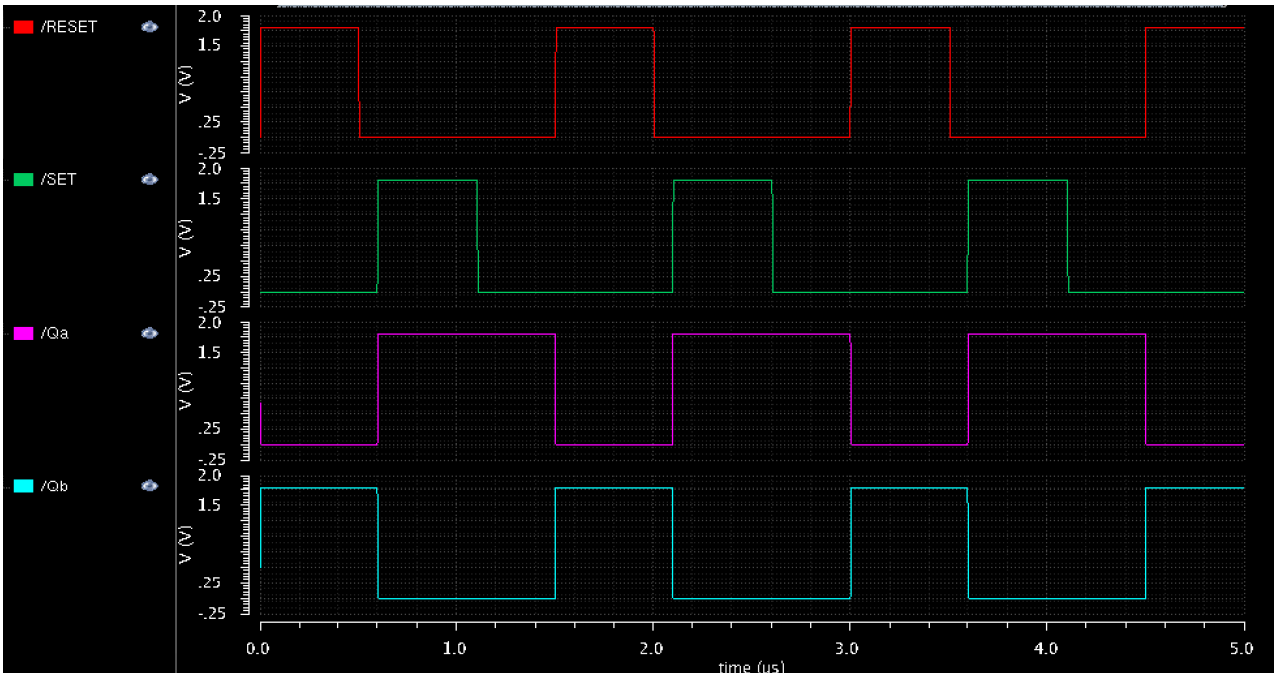


Fig. 4.50: Transient analysis of a set-reset latch.

4.3.2.2 FLIP-FLOP LATCH ENABLE

This FF has the same two inputs of the previous set-reset latch, but it has a third one (Latch Enable or LE input) that forces different conditions on the proper FF (Fig. 4.51).

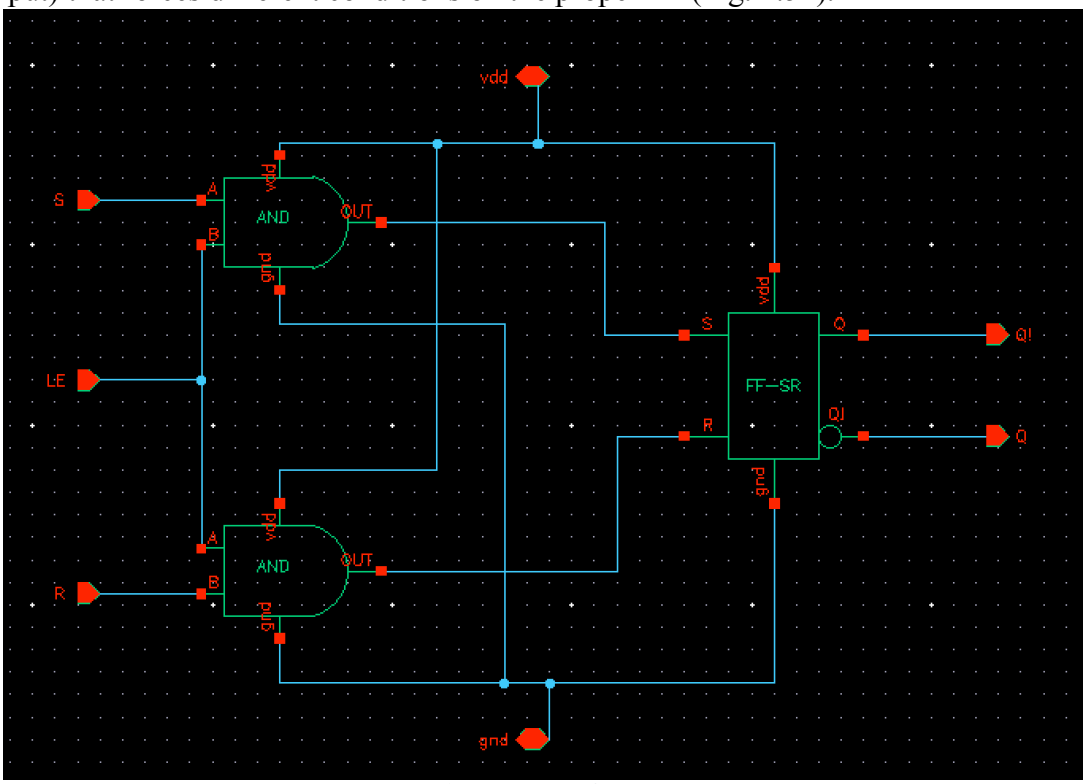


Fig. 4.51: Schematic view of a LE set-reset FF.

In details: when the LE is on the logical 0 state the memory condition is forced by the combinational circuit made before the proper set-reset FF while, on the contrary, when the LE is on the logical 1 state the flip-flop works as simple set-reset latch. The difference seems to be negligible but, in reality, the LE input is important if the flip-flop needs to be synchronized with another signal that could be exactly the LE. The functioning of the LE-FF is shown in the following Fig. 4.52.

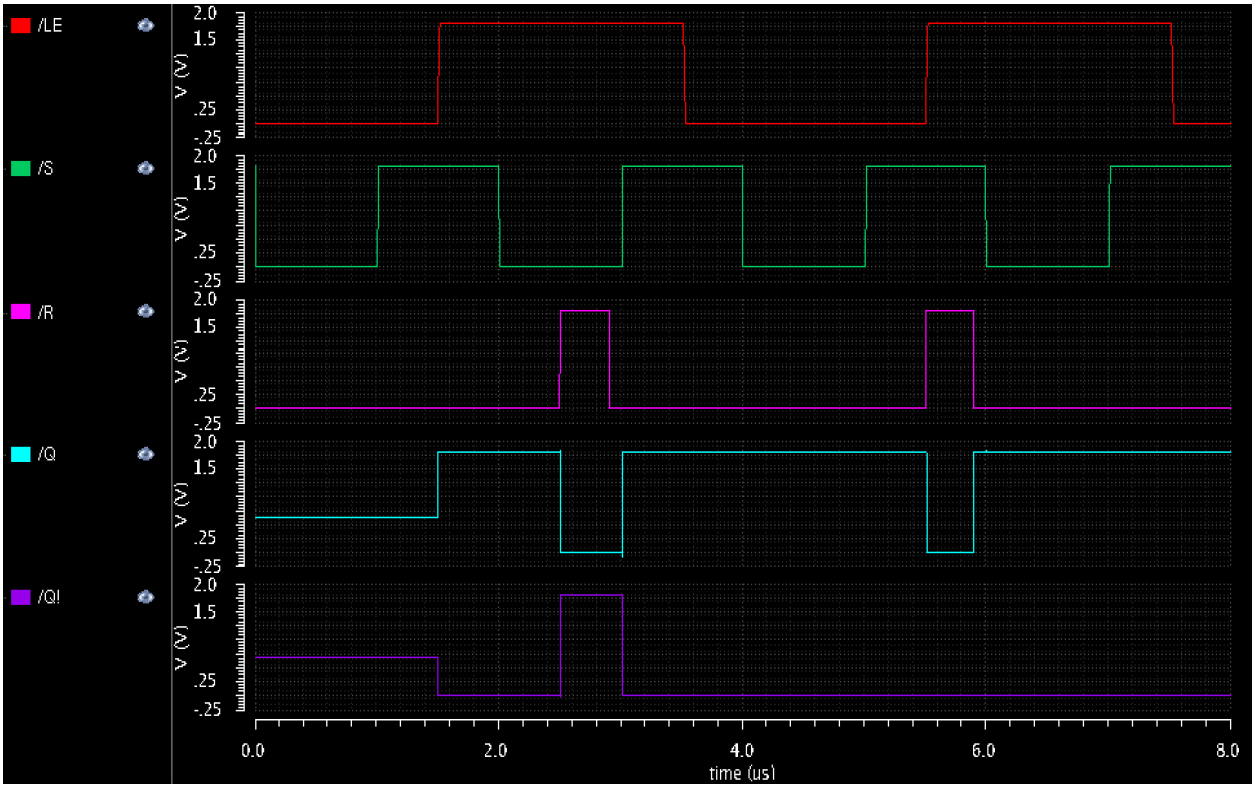


Fig. 4.52: Transient analysis of LE flip-flop.

The output maintains its previous logical state until the LE goes to logical 1 state (1.8V): all the variations on the set or reset inputs are transparent if the LE is in the 0 state.

4.3.2.3 LATCH D

This is the flip-flop that is needed for the communication circuit and, in particular, to design the register. Approximately, it is similar to the previous one while the two inputs (set and reset) are reduced to one (D input), the other is simply the inverted of D (Fig. 4.53). The working principle is very simple: when LE is 0 the flip-flop is in memory condition while when it is at logical 1 state the output is exactly the reproduction (Q) or the complementary (notQ) of the D input. In the Fig. 4.54 a transient analysis is performed in order to show precisely the functioning of latch-D flip-flop.

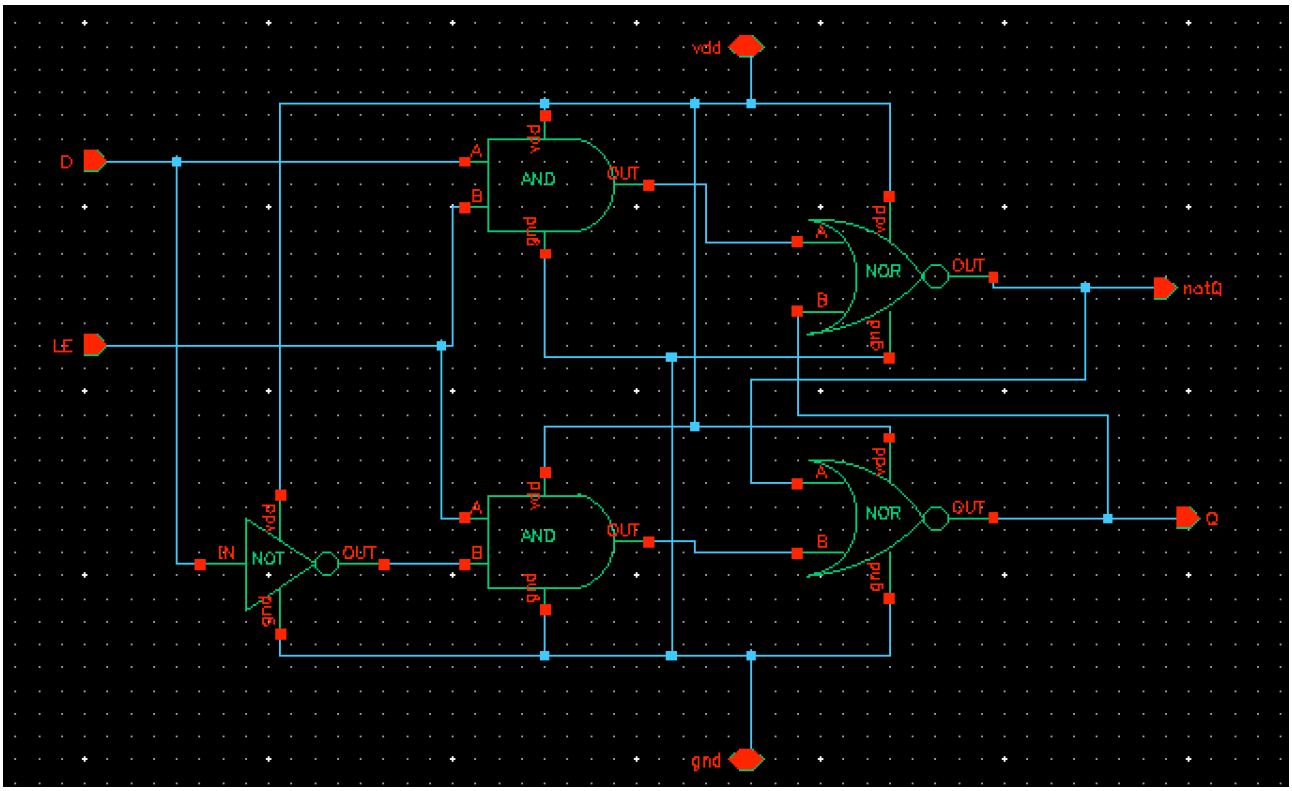


Fig. 4.53: Schematic view of a latch-D FF.

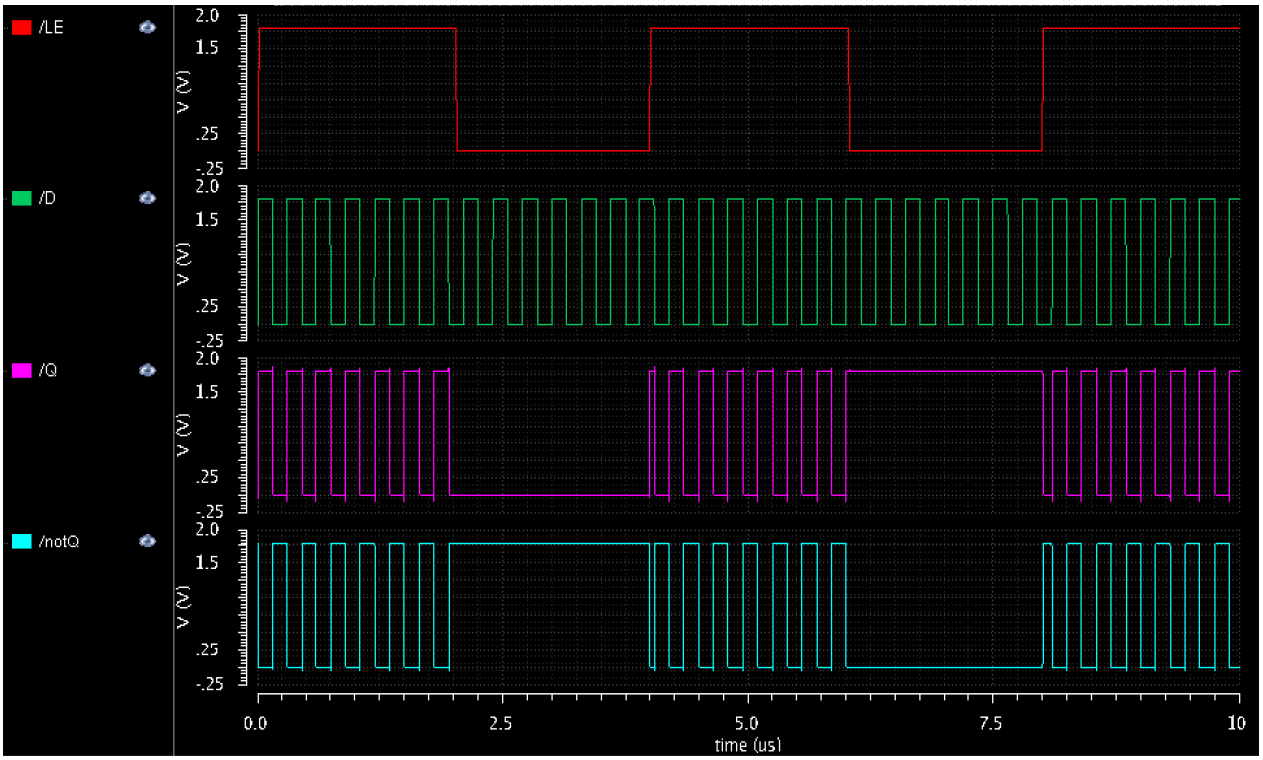


Fig. 4.54: Transient analysis of latch-D flip-flop.

4.3.2.4 PET-D

The ring oscillator triggers the latch-D while the flip-flop needs to freeze, almost instantly, the condition on the D input. At the moment, the latch is sensible on a changing that has a certain temporal duration (LE) and now a simple monostable, like the one in Fig. 4.55, is used to modify this situation.

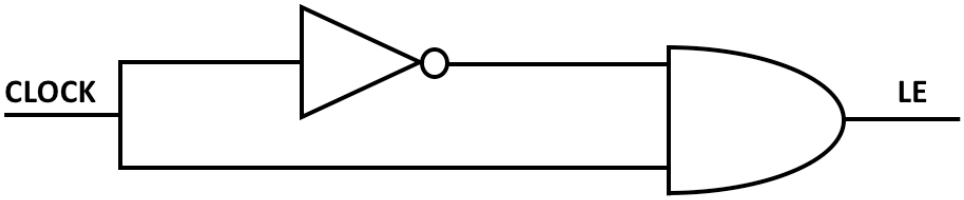


Fig. 4.55: Simple monostable with inverter as a retarder.

If this monostable is inserted before the flip-flop, the rising edge of the clock will be recognized and so the latch looks at the D input every clock-shot. This is the simplest way to realize a PET-D (Positive Edge Triggered latch-D). In the following Fig. 4.56, the schematic and symbol views are presented, and in the Fig. 4.57 the system is analyzed through a transient simulation.

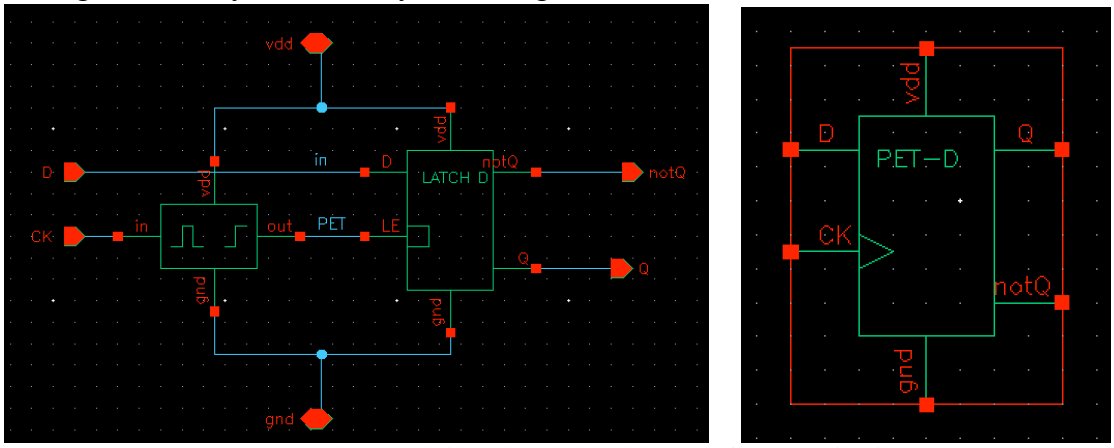


Fig. 4.56: Schematic (left) and symbol (right) views of a PET-D flip-flop.

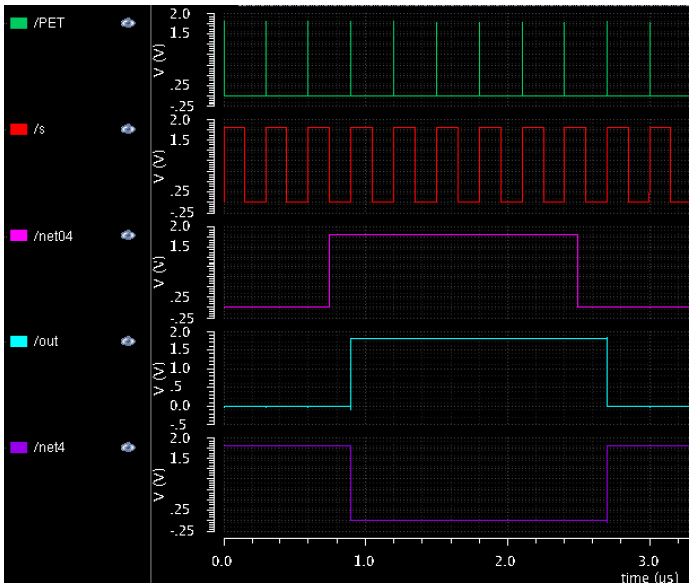


Fig. 4.57: Transient analysis of a PET-D flip-flop. Pink wave is the D input while light blue and purple ones are the Q and not(Q) outputs.

PET-D flip-flops are properly used to realize frequency divisor or shifting registers. For the first application the negate not(Q) output of the flip-flop is directly retro-connected with the D input of the same flip-flop while the Q output is connected with the CLK input of the following flip-flop as a

new clock. M flip-flops connected in this way can realize a 2^M frequency divisor: in the next Fig. 4.58 a four stages frequency divisor is implemented.

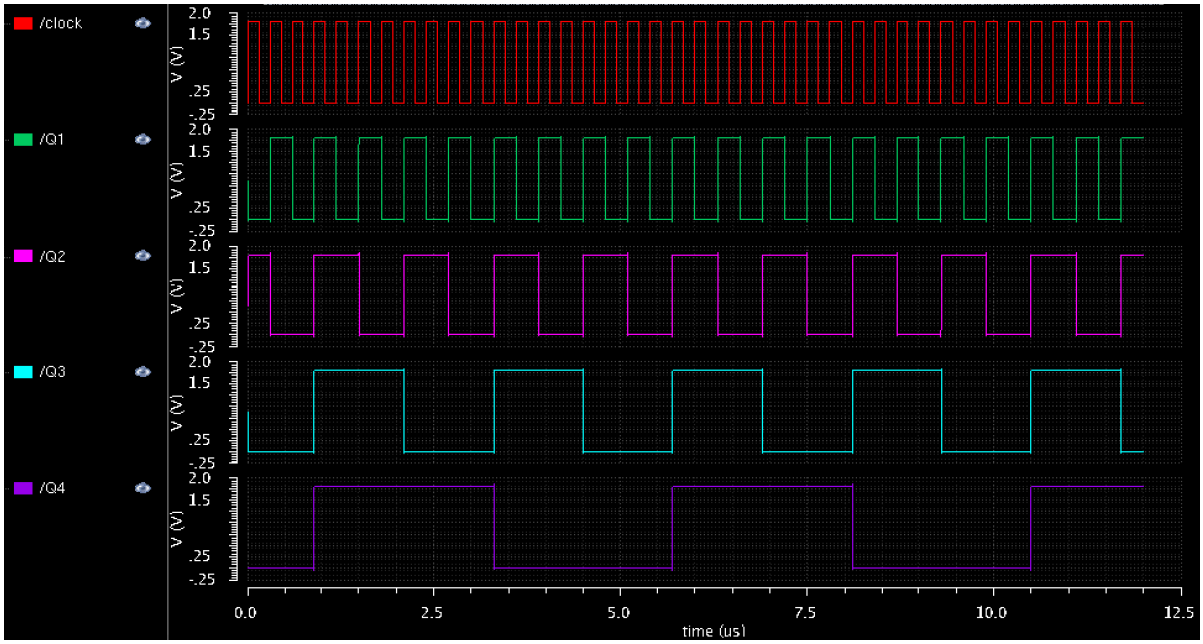


Fig. 4.58: Four stages frequency divisor made using PET-D flip-flop.

The second application is the one that is needed in order to realize the PISO register. In this case the output of every latch is directly connected with the D input of the following flip-flop. And so, with N latch, if the first FF input is a digital signal, at the final stage, the output of the N° FF will be the same wave as the D input but shifted by N clock shots (Fig. 4.59).

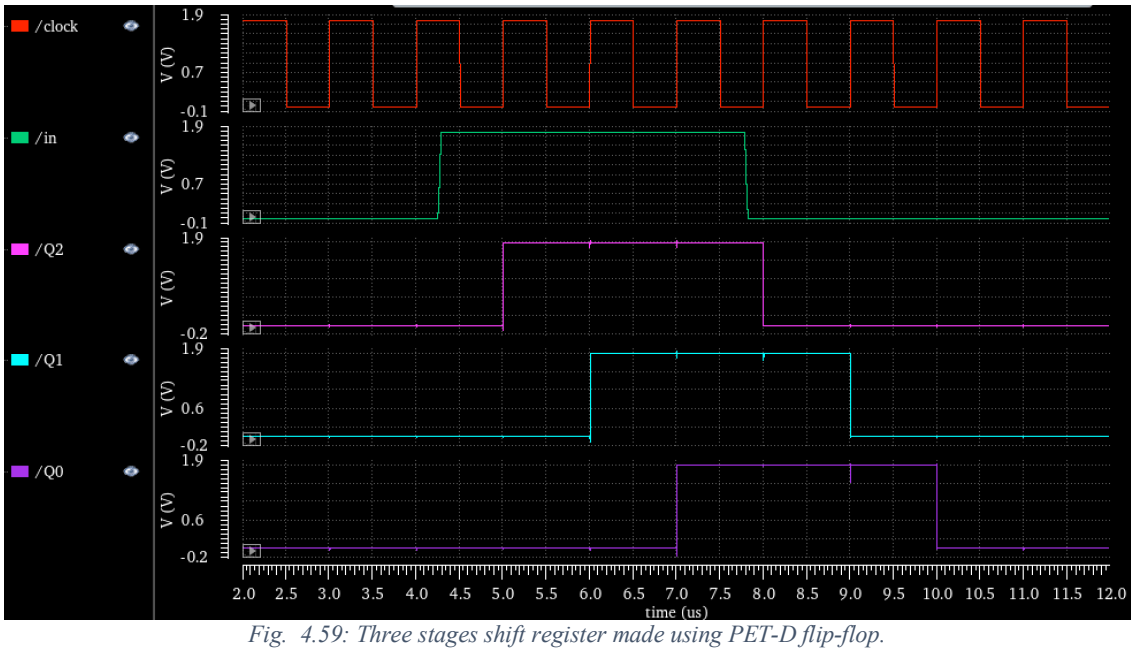


Fig. 4.59: Three stages shift register made using PET-D flip-flop.

The shifting register is now designed and, then, I need to define the connection between the digital word provided by the multiplexing layer and the flip-flop. The PISO Input Conditioning circuit of the Fig. 4.32 proves this connection.

4.3.2.5 PISO INPUT CONDITIONING

The circuit needs to have N inputs (the N parallel bits) and N outputs that will be connected as D input of the N latches. In particular, the designed circuit of the Fig. 4.60 has another input called LOAD that is a sort of flag: if LOAD is in the logical 1 state the parallel inputs flows into the flip-flop parallel D inputs as a static inputs, but when LOAD goes to logical 0 state the flip-flop starts shifting their inputs from left to right and after N clock shots all the parallel inputs will be translated into a serial output (SO) that will be exactly the modulation signal for the final switch.

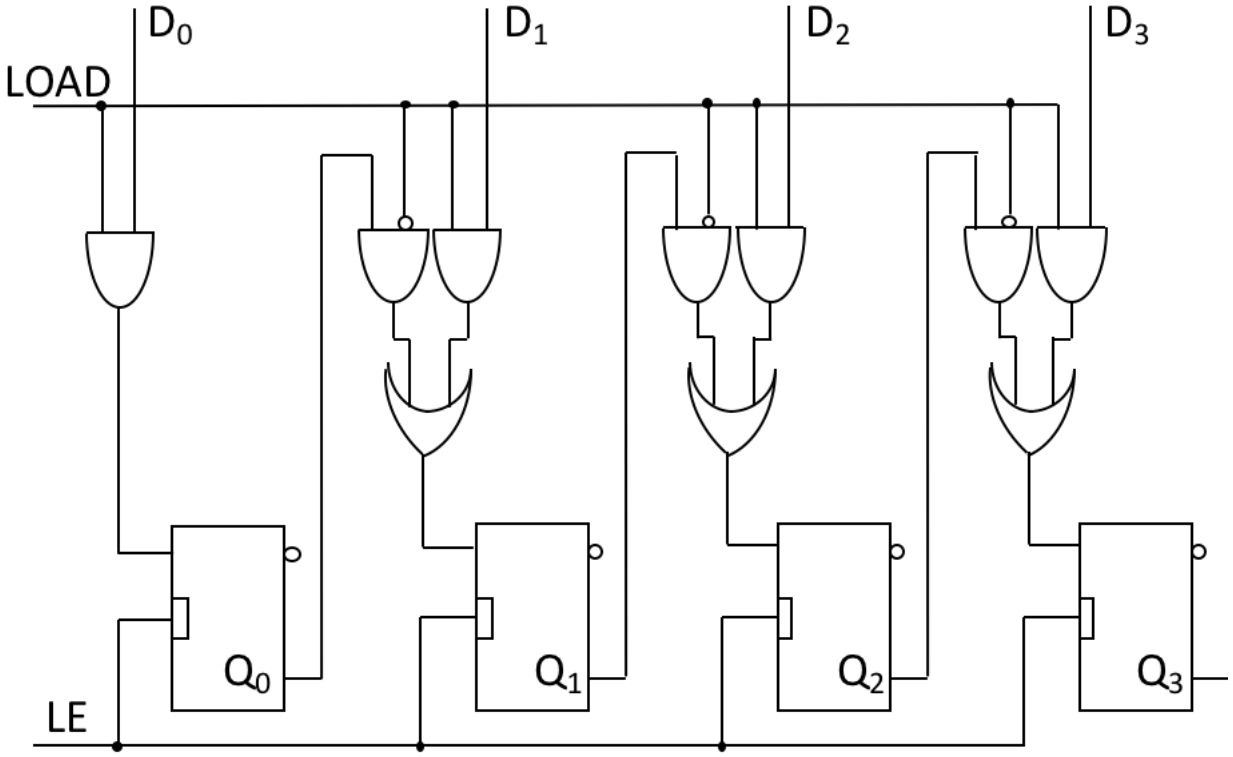


Fig. 4.60: 4-bit PISO register.

There are other methods in literature to realize a PISO register, like the one showed in Fig. 4.61, but requires different types of flip-flop, in particular preset and clear inputs are needed. I choose the configuration above since its simplicity and minor number of components.

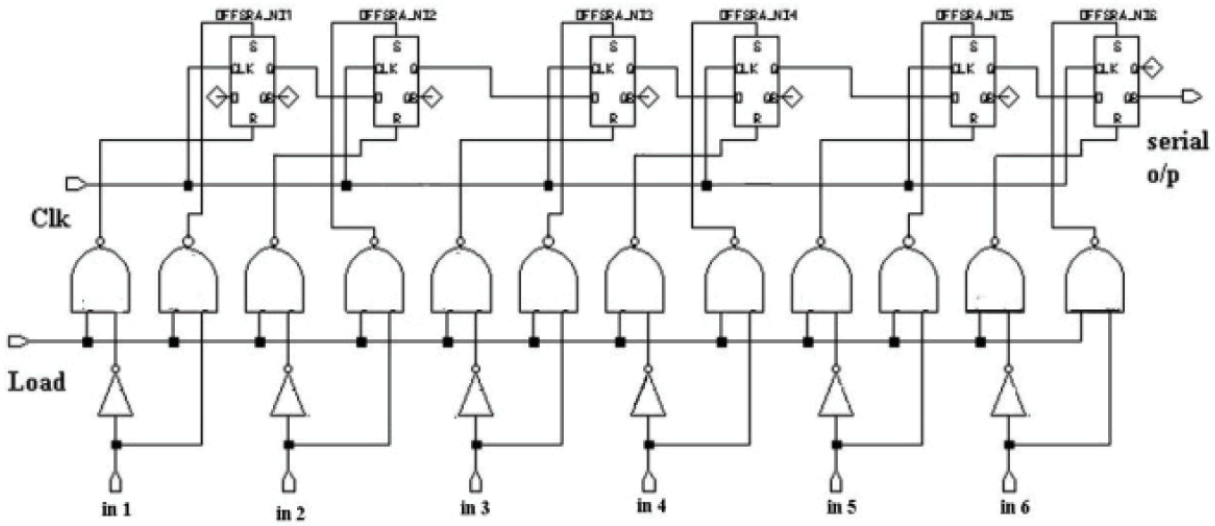
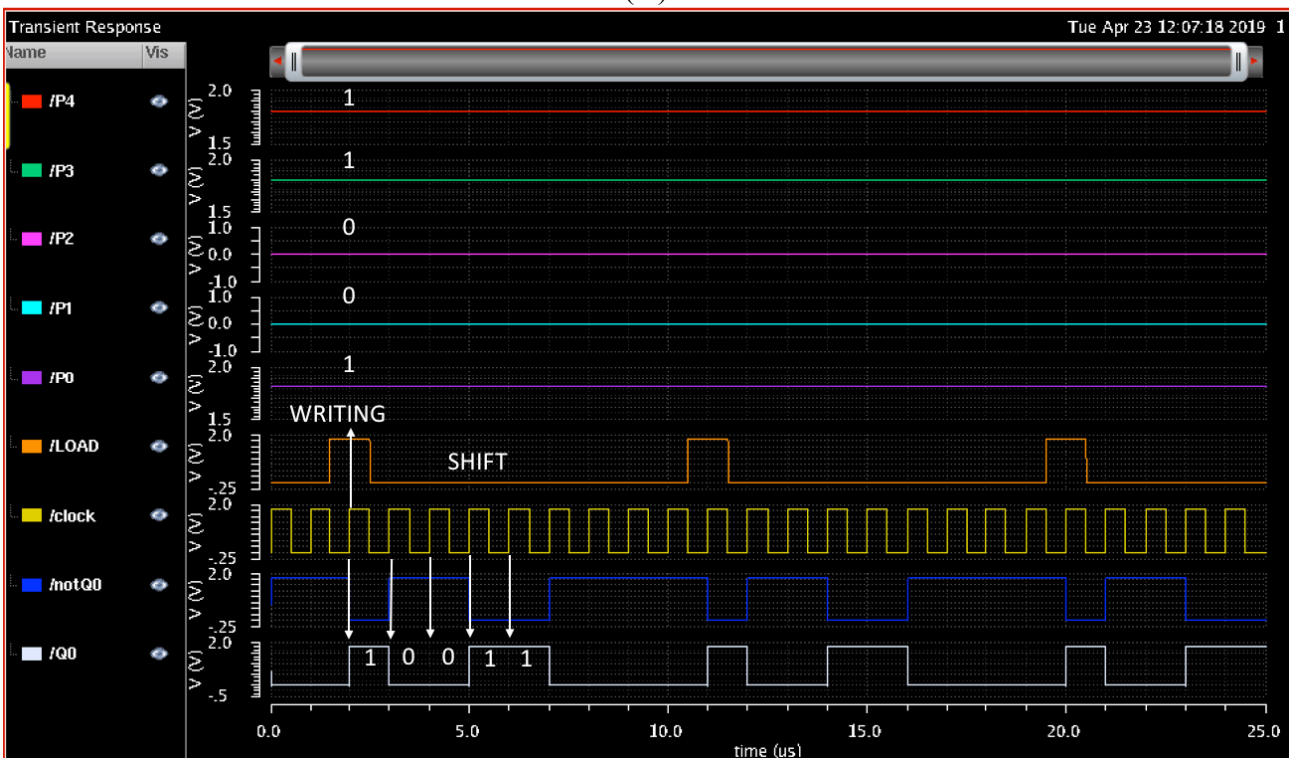


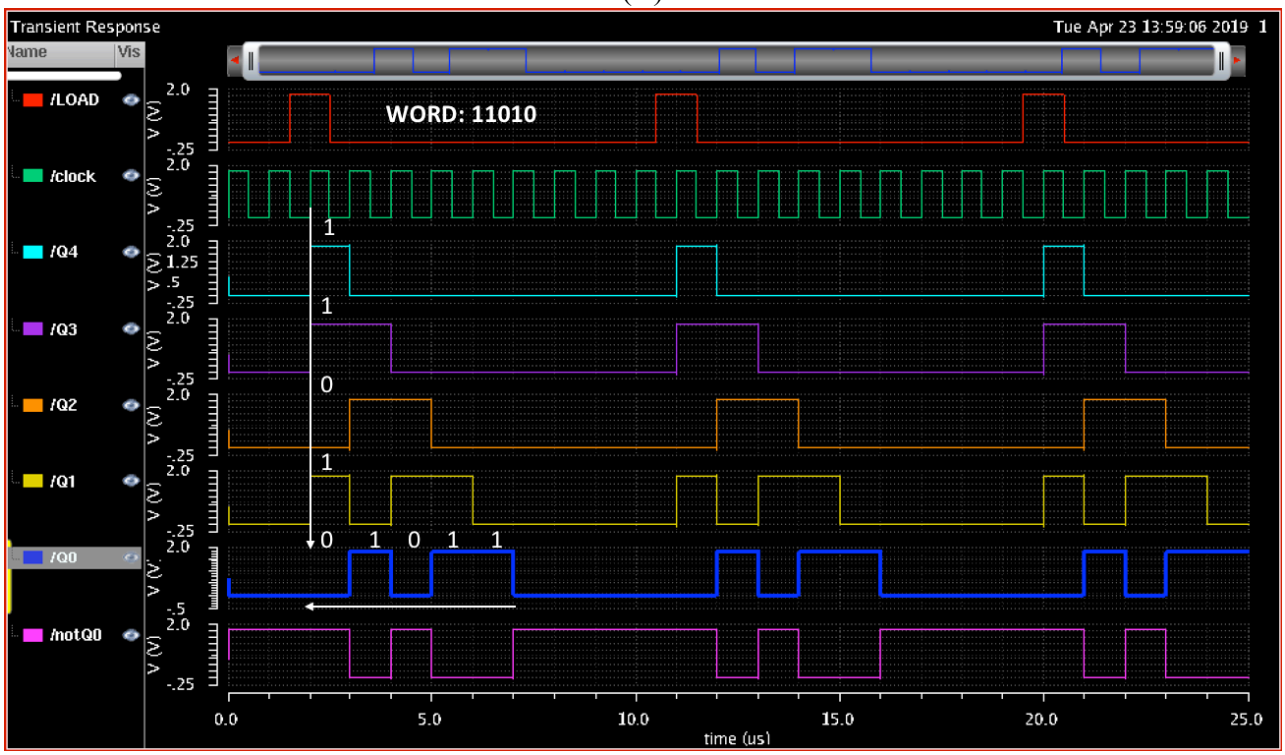
Fig. 4.61: 6-bit PISO Register. [4.4]

A 5-bit PISO register is tested in the next three simulations (grouped in Fig. 4.62).

(A)



(B)



(C)

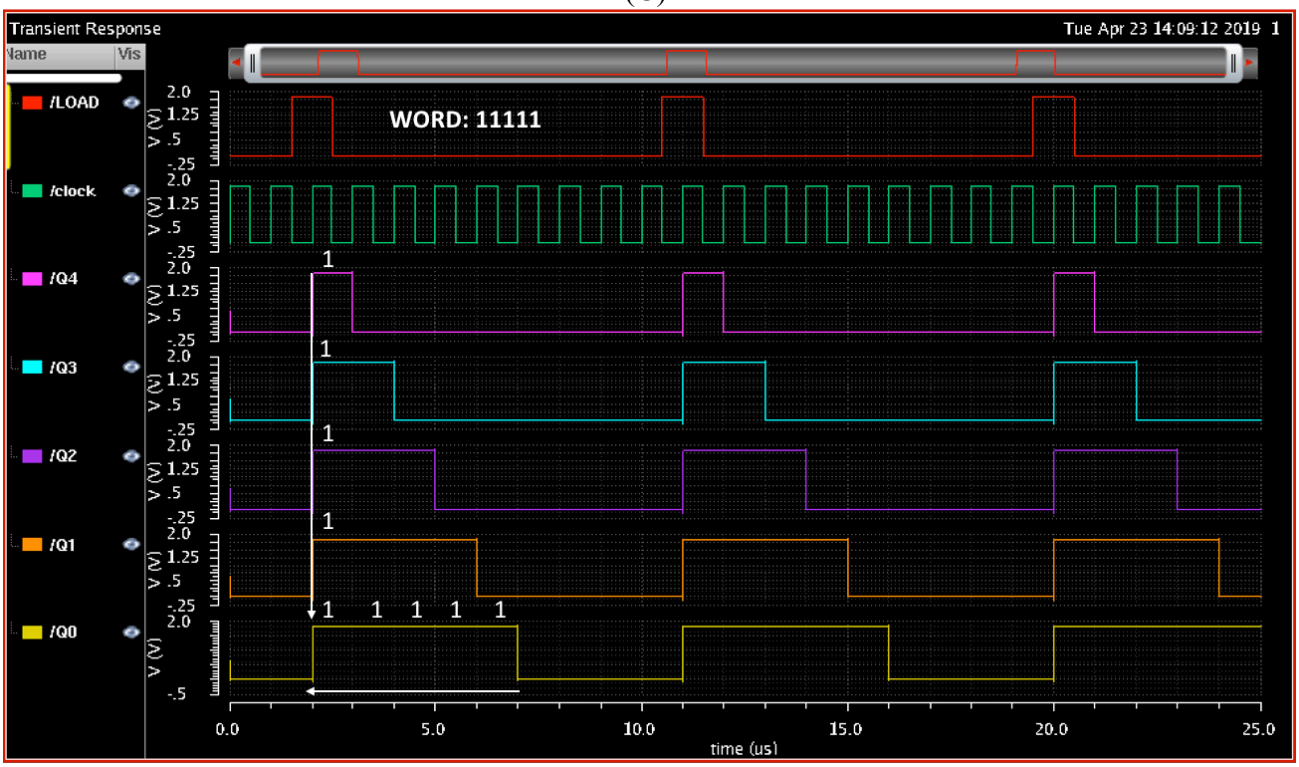


Fig. 4.62: Transient analysis for 5-bit PISO register. (A) Detail of parallel inputs P4→P0 (11001) and Q0 output. (B) and (C) writing and shifting details of the two words (11010 for B and 11111 for C) through the 5 FF (Q4 →Q0).

At this point the number of the flip-flop need to be chosen and the format of the data packet need to be declared. Inspired by a work done for a wireless multi-channel tactile sensing glove [4.5], the data packet will be defined as follows (Fig. 4.63).

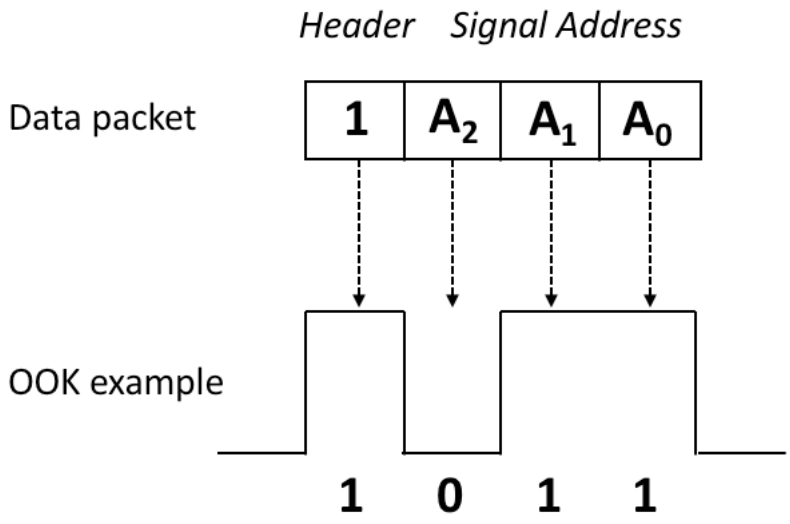


Fig. 4.63: Packet template and binary example of OOK modulation.

The header is needed because the receiver cannot understand otherwise when the communication starts (imagine the case in which the signal has the ID equal to 001). 3 bits for the address (A_2, A_1, A_0) are the minimum possible in order to distinguish the 5 signals treated by the multiplexing layer. Once chosen the number of bits, it is then possible to realize the proper PISO register with four stages (4 parallel inputs).

In order to reduce the sizes of this block, I decide to extract the recognizer part from every latch and use a single monostable that triggers every flip-flop. So, the PET-D turns to be a latch-D flip-flop and the monostable in Fig. 4.55 is designed separately as a simple block of the complete communication circuit. Finally, the complete full circuit will be composed by five main blocks: Front-End monostable, starved ring oscillator (SRO), monostable synchronizer, 4-IN-PISO register and 4-IN-PISO Input Conditioning circuit as in Fig. 4.64.

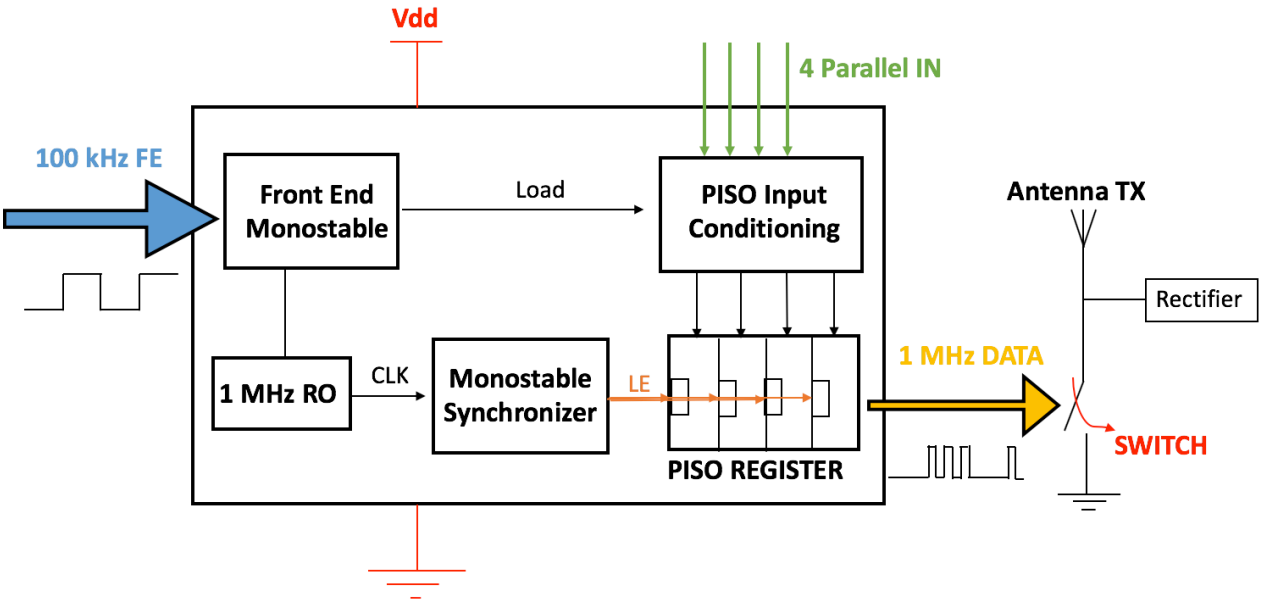
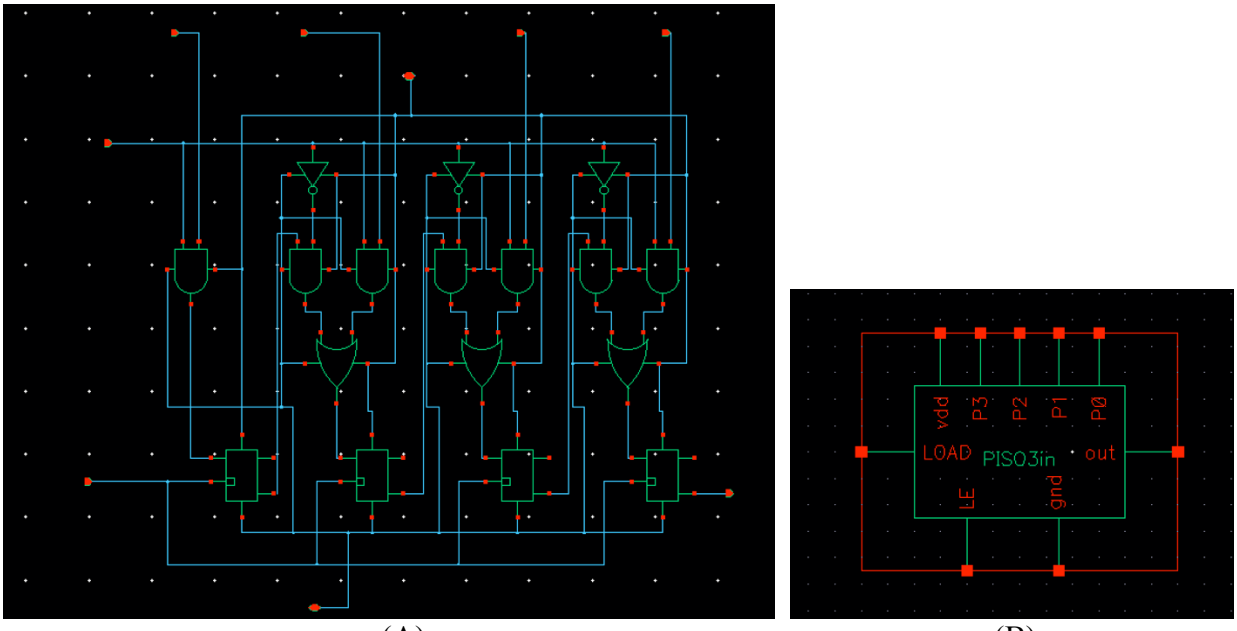


Fig. 4.64: Communication full circuit main blocks.

Fig. 4.65 shows the schematic, symbol view and the layout of both the PISO register and its input conditioning circuit.



(A) (B)

(C)

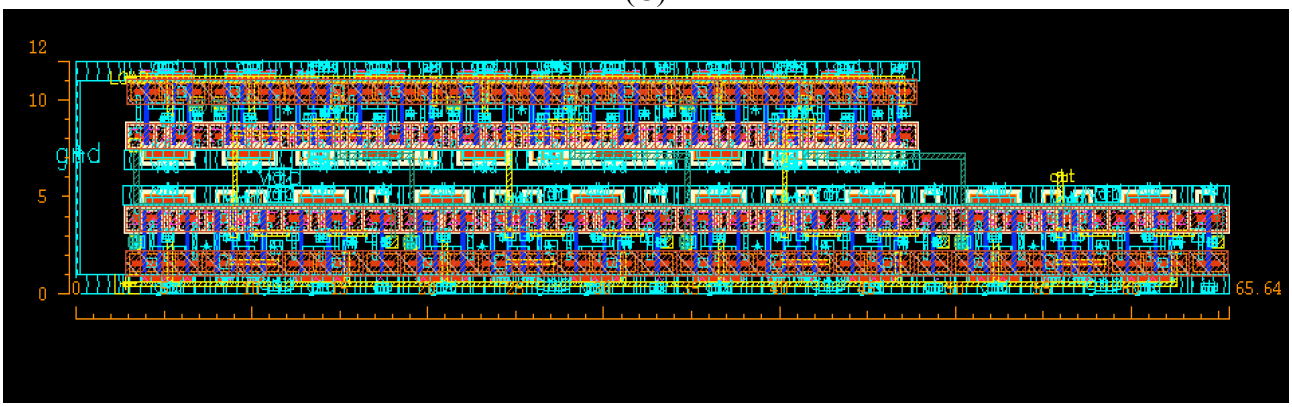


Fig. 4.65: Schematic (A), symbol (B) and layout (C) views of 4-bit PISO register and input conditioning circuit.

In details, two parts compose here the layout: the bottom one (bigger) is the part that includes the latches, while on the top is the PISO input conditioning circuit. Also this block is tested with a transient post-layout simulations, which have shown that no changes in the design are necessary.

4.3.3 FRONT-END MONOSTABLE

The Front-End monostable is really a quite important part of the entire communication circuit because it is the only one that receives the signal acquired by the sensors. It is a simple monostable, but quite different with respect to that introduce in the previous section. Here, instead of a simple inverter, a latch-D is used as a retarder because I need to control different things. In particular, I don't know a priori the exact waveform of the incoming signal. Therefore, I can work here with a digital waveform between 0 and 1.8V, with a 10 μs of period and 50% of duty-cycle. This is the first reason for which I chose another element with respect to the inverter that, as I have already mentioned, is really sensitive to the edges and, moreover, its proper working depends on the sharping of the rise and fall edges.
Furthermore, the output of the monostable has to trigger the LOAD signal, which is another good reason for which latch-D is a good choice indeed. The output of the monostable has to be a digital wave large enough to permit the correct writing on the flip-flop. I design it large enough to permit also the detection of changes in the digital word provided as a parallel input (signal address) in order to make the design more versatile and to be sure that almost one edge of the clock is included in that interval of high time. The schematic and symbol views of the monostable are shown in the following Fig. 4.66.

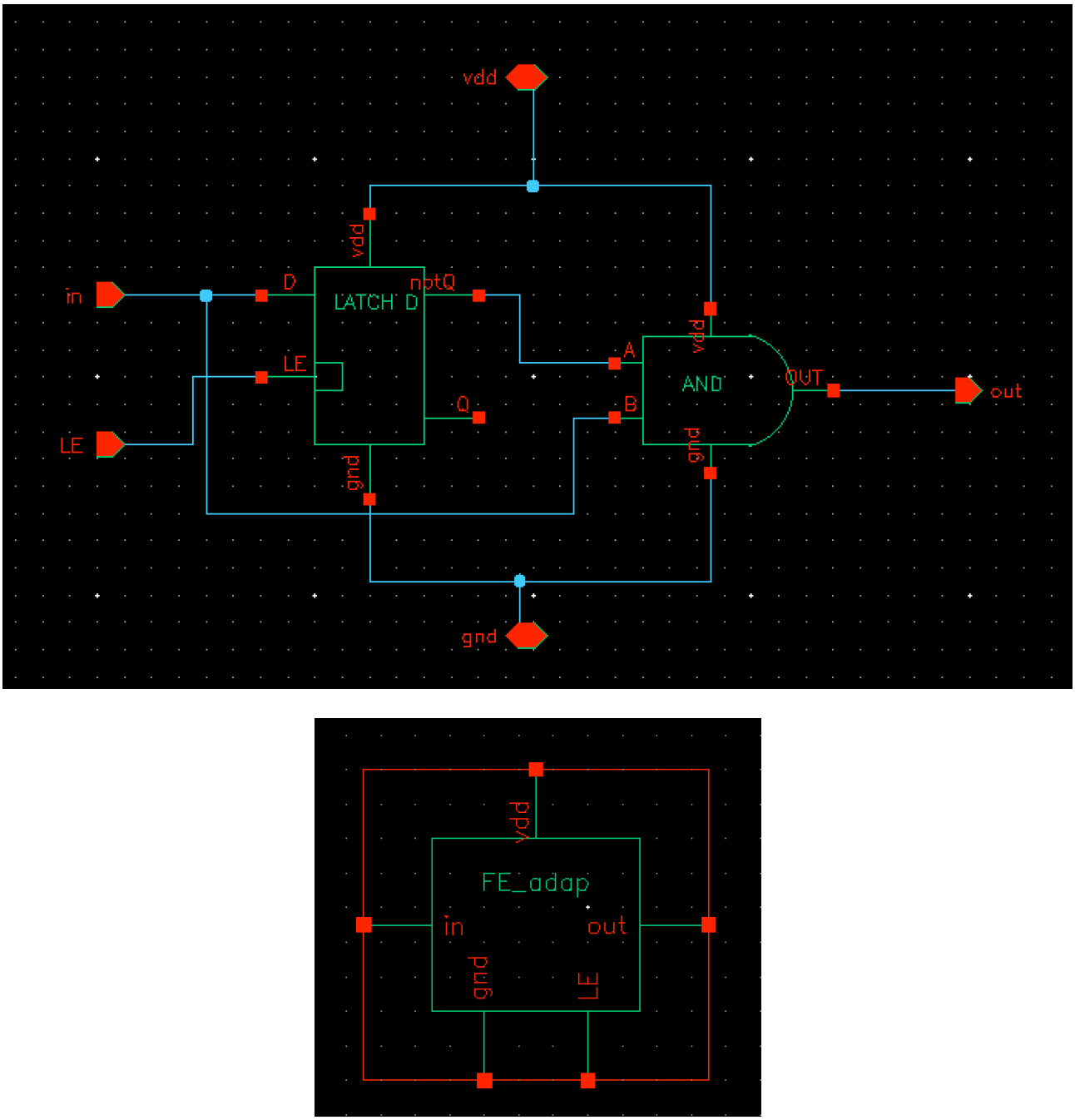


Fig. 4.66: Schematic (top) and symbol (bottom) views of Front-End monostable.

The monostable synchronizer of the Fig. 4.64 also triggers the D-latch of the Front End monostable. So, the working principle is simple: whenever a rising edge of the incoming signal is detected, then a digital wave is generated by the Front-End monostable, which is the LOAD signal that will trigger the PISO Input Conditioning circuit the writing or shifting operations. In the following Fig. 4.67, a simple transient simulation is performed in order to verify the concept idea.

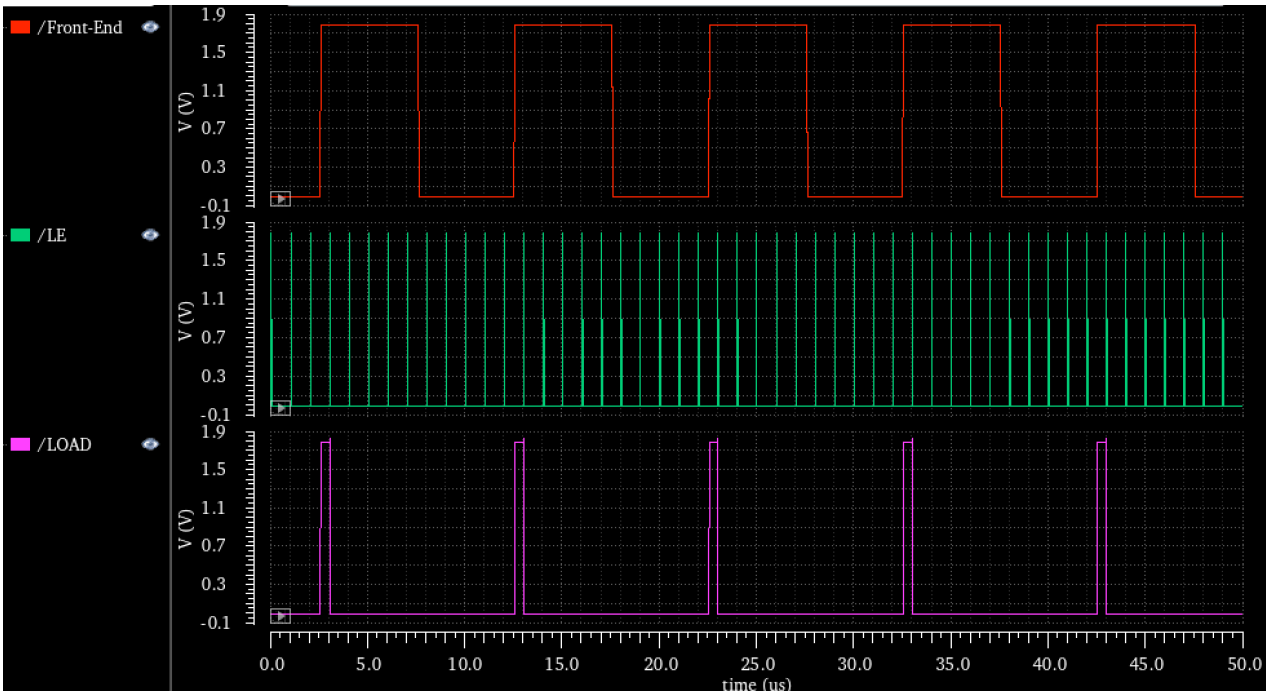


Fig. 4.67: Transient analysis of Front-End monostable.

The last Fig. 4.68 shows the layout of the monostable with labels in order to have idea of the occupied area.

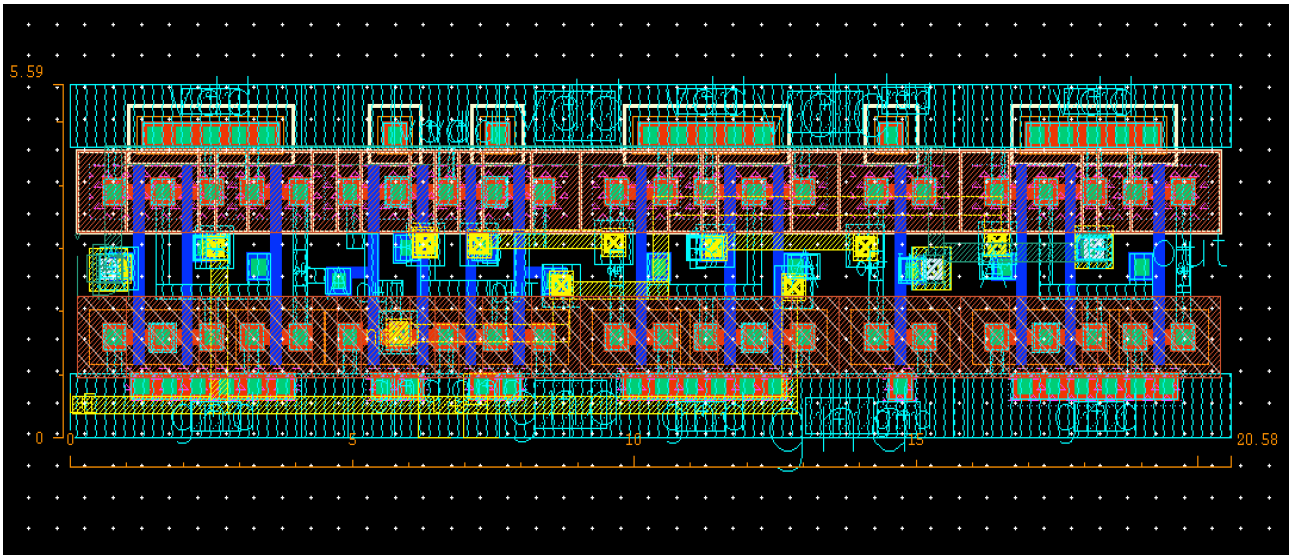


Fig. 4.68: Layout view of Front-End monostable.

4.3.4 MONOSTABLE SYNCHRONIZER

As I have already explained, I decide to use an external monostable to synchronize all the four latches present in the register. The configuration of the block is the same described in Fig. 4.55, but now I need to go down in details, in particular I am going to explain the connection made between the output of the starved ring and the four latch inputs.
I have already mentioned the problem on the amplitude of the ring-oscillator output caused by the pass transistors but there is also another problem that I did not anticipated before: the rise and fall timing are very large if compared to the typical edges of a simple inverter. This condition could be

simply solved by applying, downstream the ring, two stages of inverters that should re-establish the correct dynamic amplitude of the clock and, therefore, the acceptable rise/fall timing [4.6].
In particular, the monostable need to trigger the four latches of the register and the latch created into the Front-End monostable block.
In the Fig. 4.69 below, the differences between the output of the ring and the signal after this simple logical operation is presented through a time varying simulation.

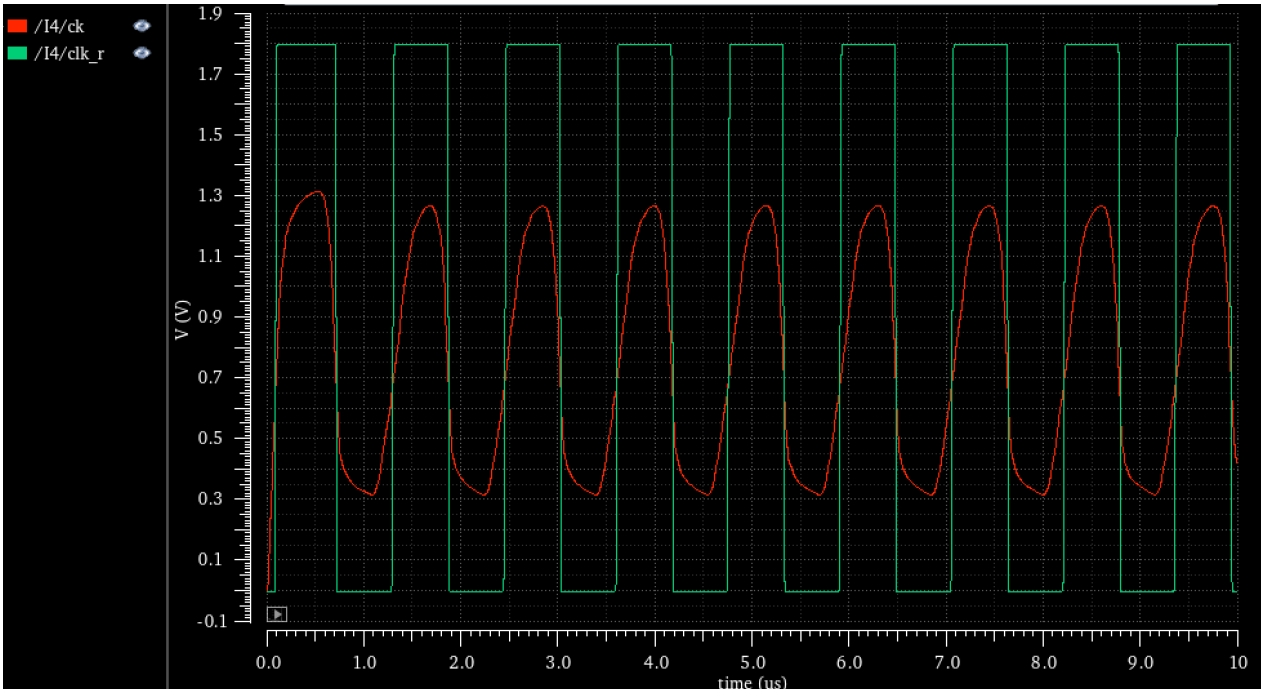


Fig. 4.69: Transient analysis simulating differences between the output of the ring oscillator (red) with the digital wave created by the two inverters applied in series (green).

The proper monostable need now to be designed. In particular, the sizes of the inverter, used in this case as a retarder, need to be accurately designed. In the following Fig. 4.70, the monostable working principle is shown in order to make the discussion clearer.

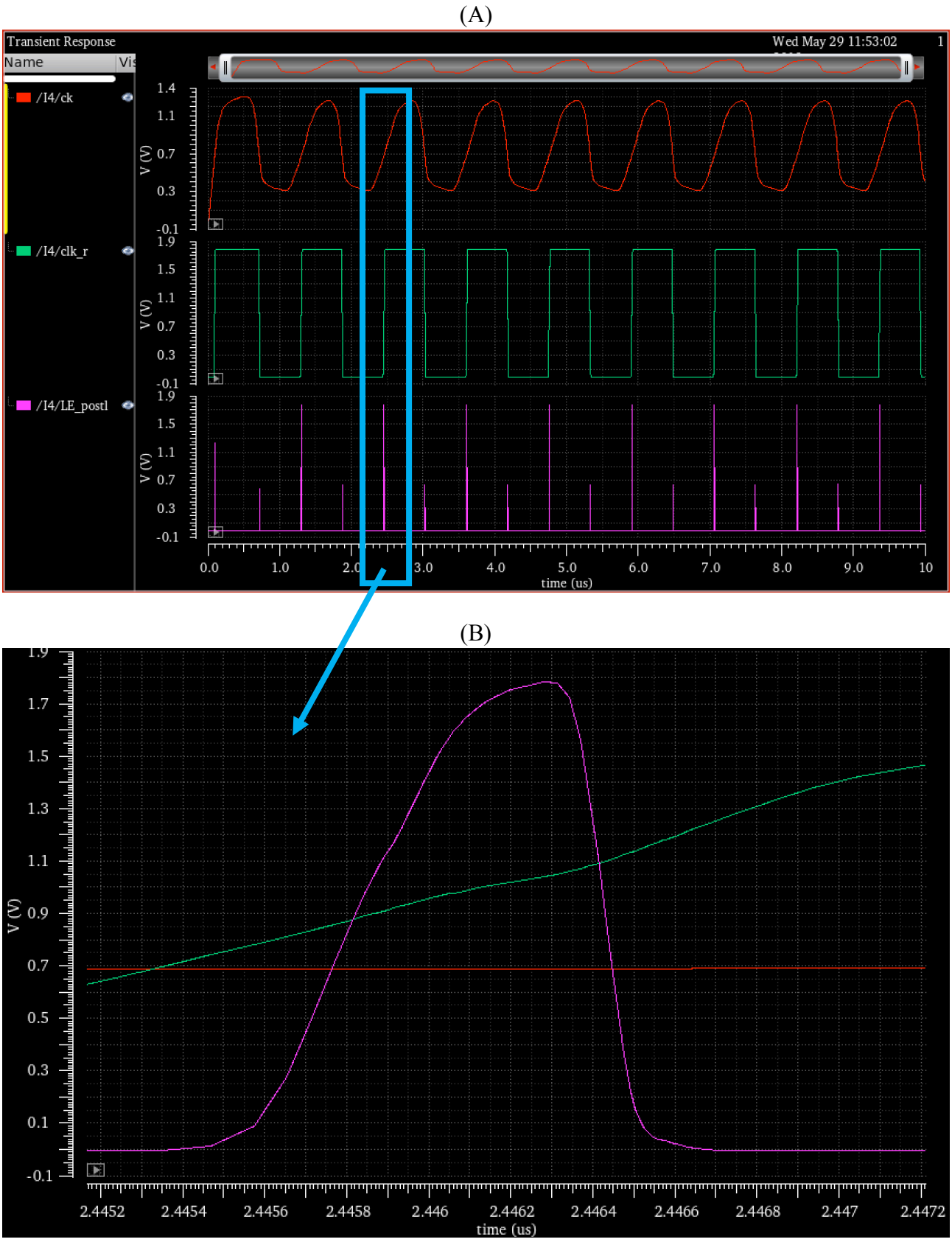


Fig. 4.70: Transient analysis to show the generated LE signal (A) and detail on the waveform of the command signal (B).

The generated signal has to trigger all the latches and so another important consideration needs to be done: in this case the layout influences a lot the functionality of the monostable since the connections between it and the FF will be long enough to cannot exclude the influence of the parasitic capacitance. The command signal decrease in amplitude and the transitions between high and low state by inserting a capacitance after the monostable, and vice versa, became less sharp. In that way, the signal cannot properly command the flip-flop! In the following Fig. 4.71, the layout of the monostable is shown.

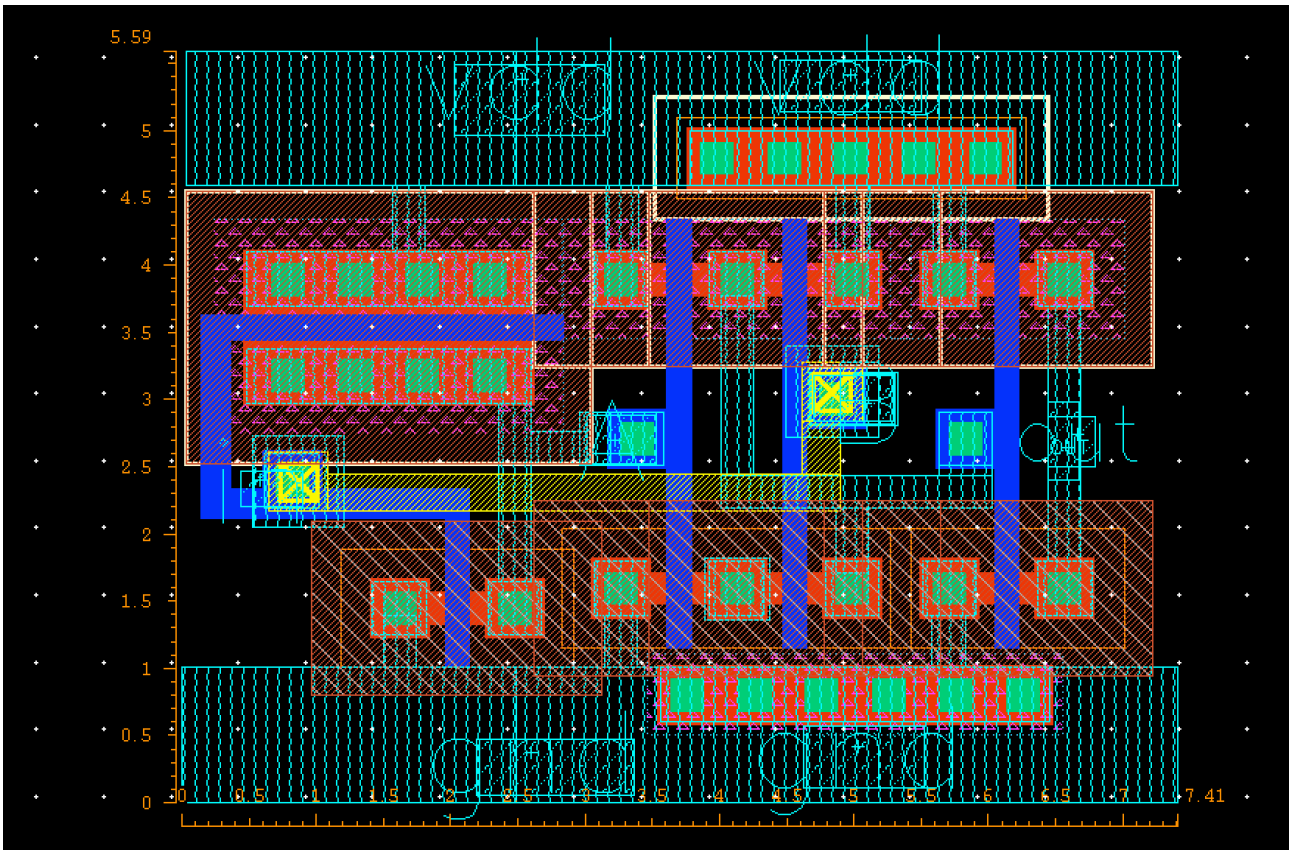


Fig. 4.71: Layout view of the monostable synchronizer.

After all the post-layout simulation the final sizes of the retarder NOT is chosen in this way:

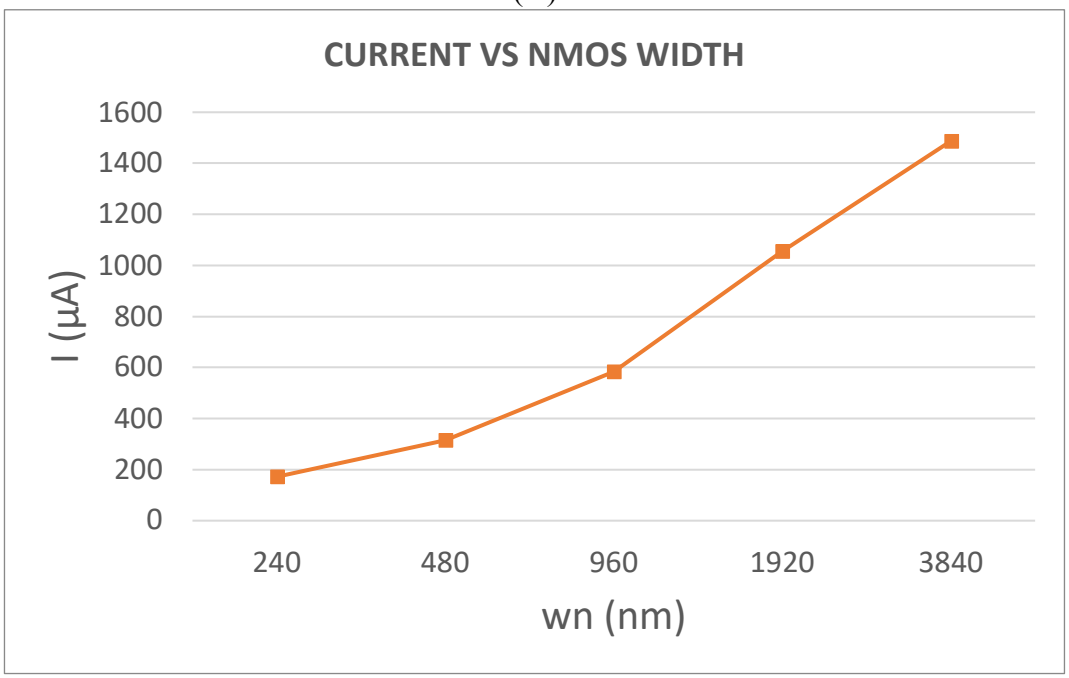
- NMOS: minim sizes 180x240 nm.
- PMOS: minim length 180 nm and 9 times the minim width (2160 nm).

What is important to notice is that if the number of flip-flop increases, the size of the inverter need to be increased too, in order to maintain the circuit functioning correctly.

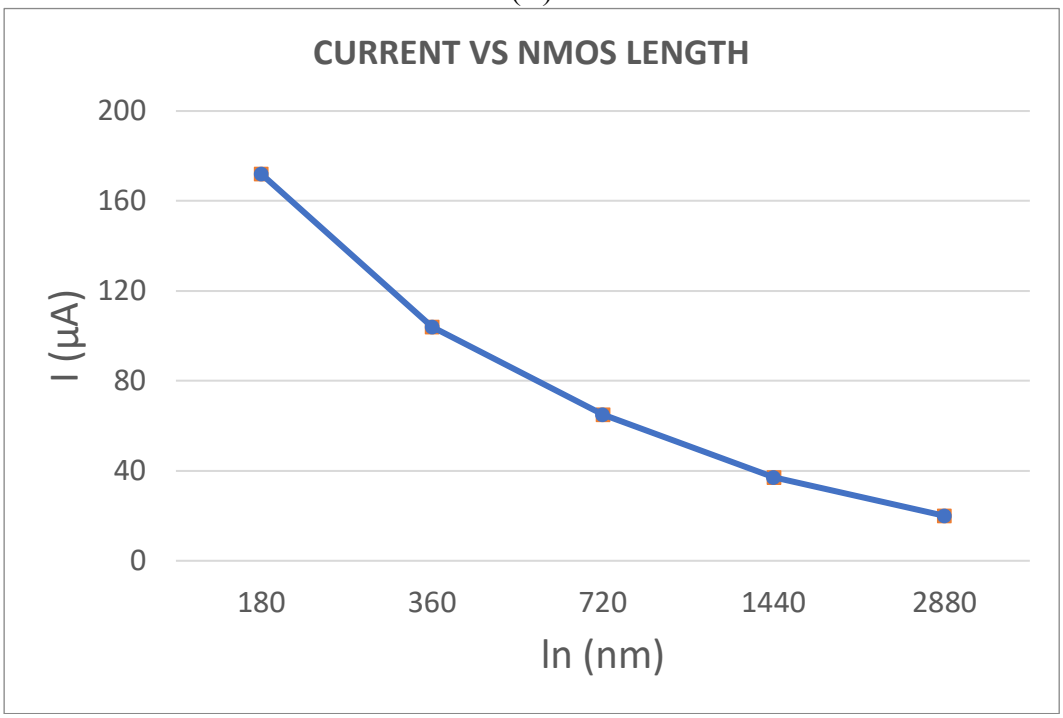
4.3.5 SWITCH

The final switch of the designed circuit is the one that provides the proper On-Off-Keying (OOK) communication with amplitude modulation of the scattered wave. In the Chapter 3, I spoke about wireless data transmission mentioning some possibilities for the transducer and for the incidence of the incoming waveform from the external base station.
First of all, the switch is tested applying a simple resistance as electrical equivalent impedance model of load in order to investigate the properties that the chosen NMOS need to have in order to modulate the signal. Remember that the important parameter here is the drain current: if the passed current is too low anything will happen on the impedance of the modulator. In particular, in the next Fig. 4.72, the result of a simple starting simulation is shown inserting the current on the y-axis and the proper parameters on the x-axis.

(A)



(B)



(C)

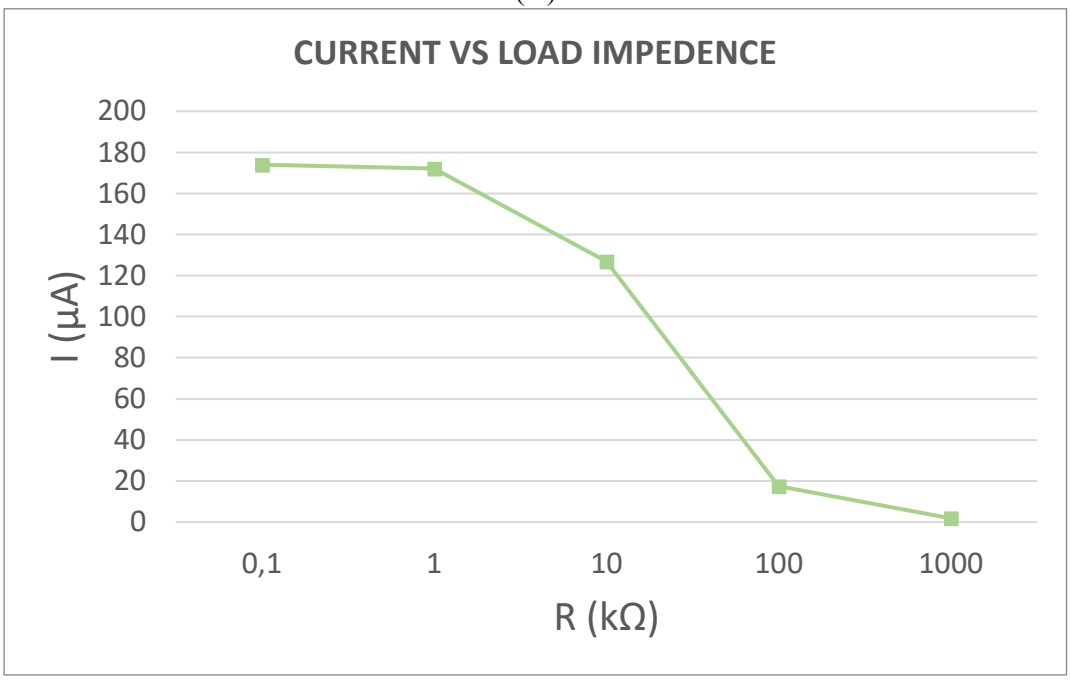


Fig. 4.72: Drain current variation of the switch compared with the sweeping of NMOS width (A), length (B) and total load impendence (C).

As expected, the NMOS needs to be designed with a short channel in order to increase the current and to limit the passive resistance with a width large enough to modulate the impedance. This last parameter plays in important role on the design decision for the switch sizes: as the impedance increase the current decrease exponentially and so the electrical model of the piezo need to be properly defined in order to choose the correct sizes for the NMOS.
I briefly introduce now the electrical model for the transducer (simple RC circuit) and the incident wave (simple alternate current generator). The tested circuit is shown in Fig. 4.73.

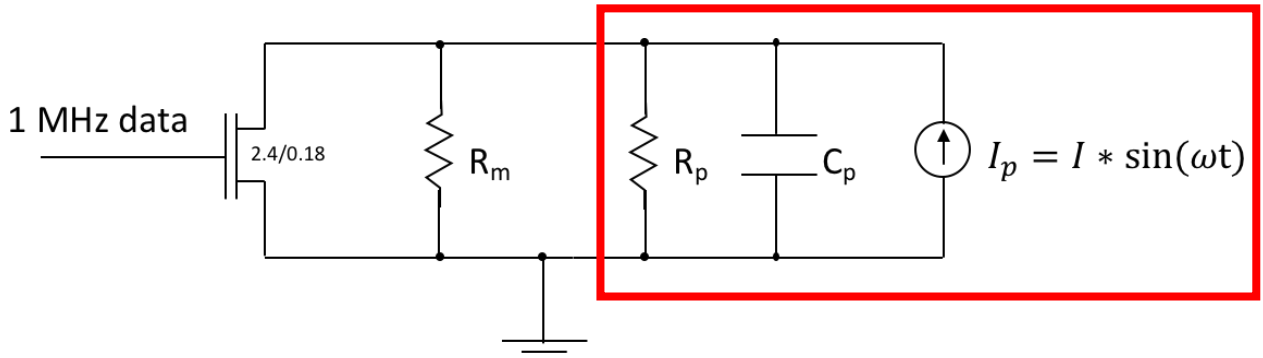


Fig. 4.73: Electrical model of the piezo and incidence (red box), modulator and switch.

The electrical model of the transducer is taken from literature [4.7] [4.8] [4.9]. The switch sizes are properly chosen in order to have modulation on the R_m resistance. It worth to notice here that the R_m (modulator) is set exactly equal (in value) to the resistance of the electrical model of the piezo in order to have the better result in modulation.

- When the switch is in opened condition $R_M = R_P$ and so the full matched condition is achieved.
- On the contrary when the switch is closed the modulator is in parallel with a short circuit and so $R_M = 0$ and the mismatched condition is achieved.

This is the base principle for the backscattering communication and the result of a simple transient analysis is shown in the next Fig. 4.74 by reporting the amplitude of the modulation of the current

flowing into the modulator R_M and, so, the variation on the impedance of the sensor node. A simple random bit sequence is set between 0 and 1, which correspond to the well note 0V and 1.8V.

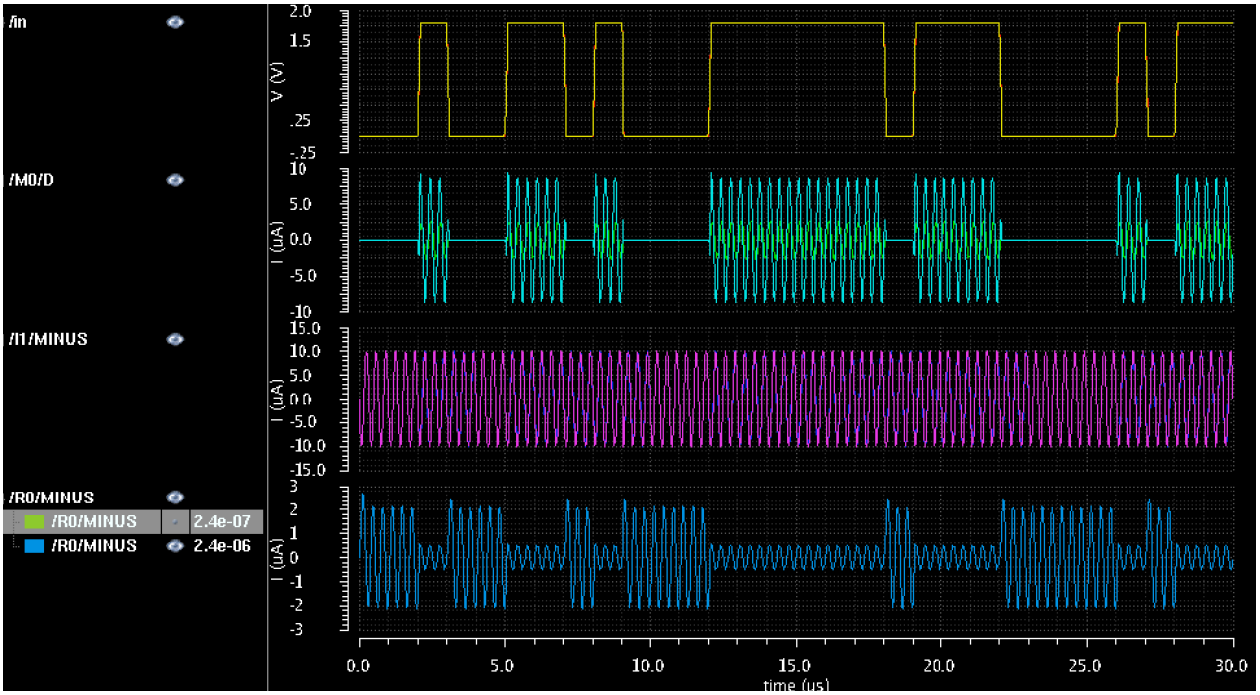


Fig. 4.74: ASK modulation by the switch element.

The switch is the most common element used to provide S-OOK modulation for backscattering communication and it is also used in [4.10] in neural dust work to provide wireless data transmission.

CHAPTER 5

FULL CIRCUIT SIMULATIONS

All the blocks of the circuit are well explained in detail in the previous Chapter 4 while here, in this section, the schematic of the full circuit is presented (Fig. 5.1).

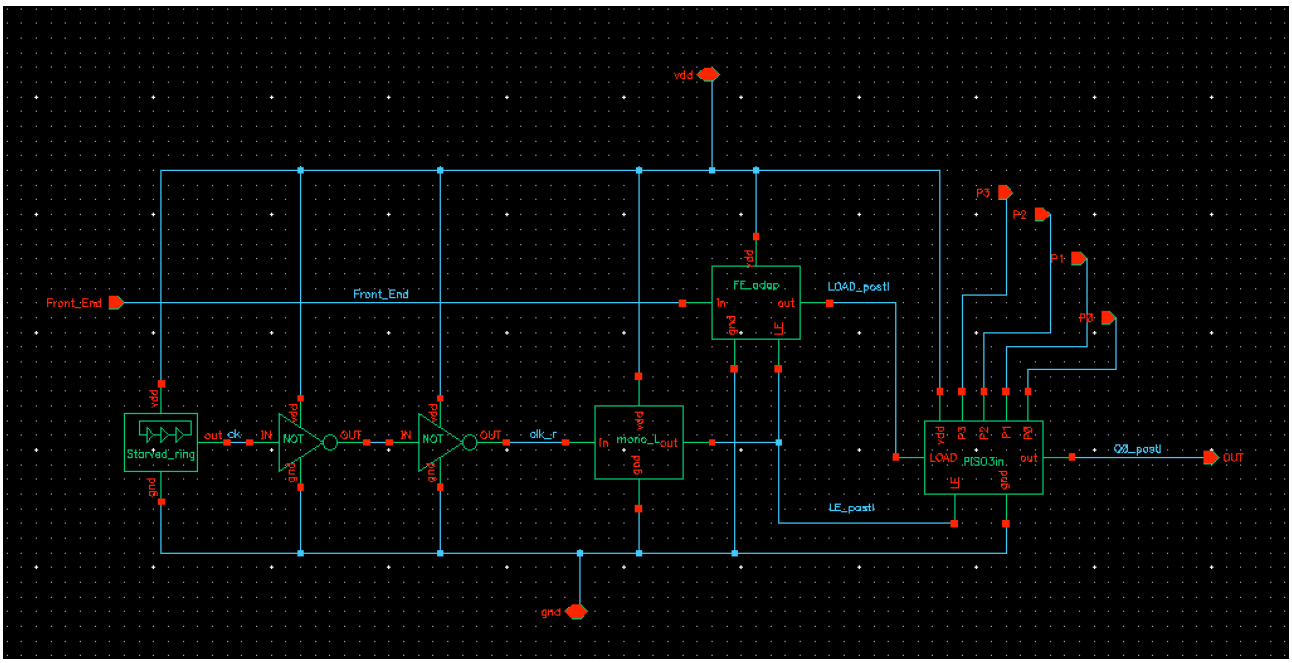


Fig. 5.1: Full-circuit schematic view.

All the simulations are performed with post-layout parasitic capacitances and, so, the next Fig. 5.2 presents the layout of the full circuit while Fig. 5.3 shows the complete extracted view.

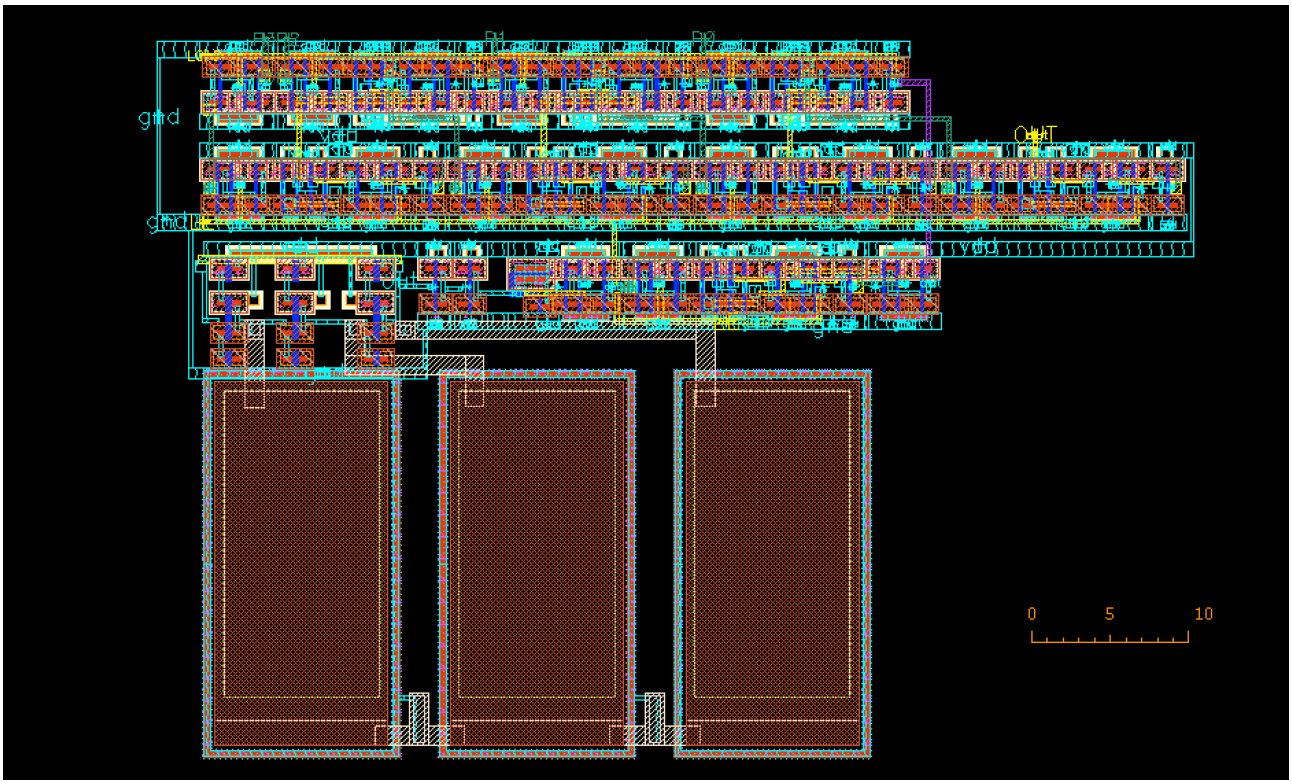


Fig. 5.2: Layout of the full-circuit.

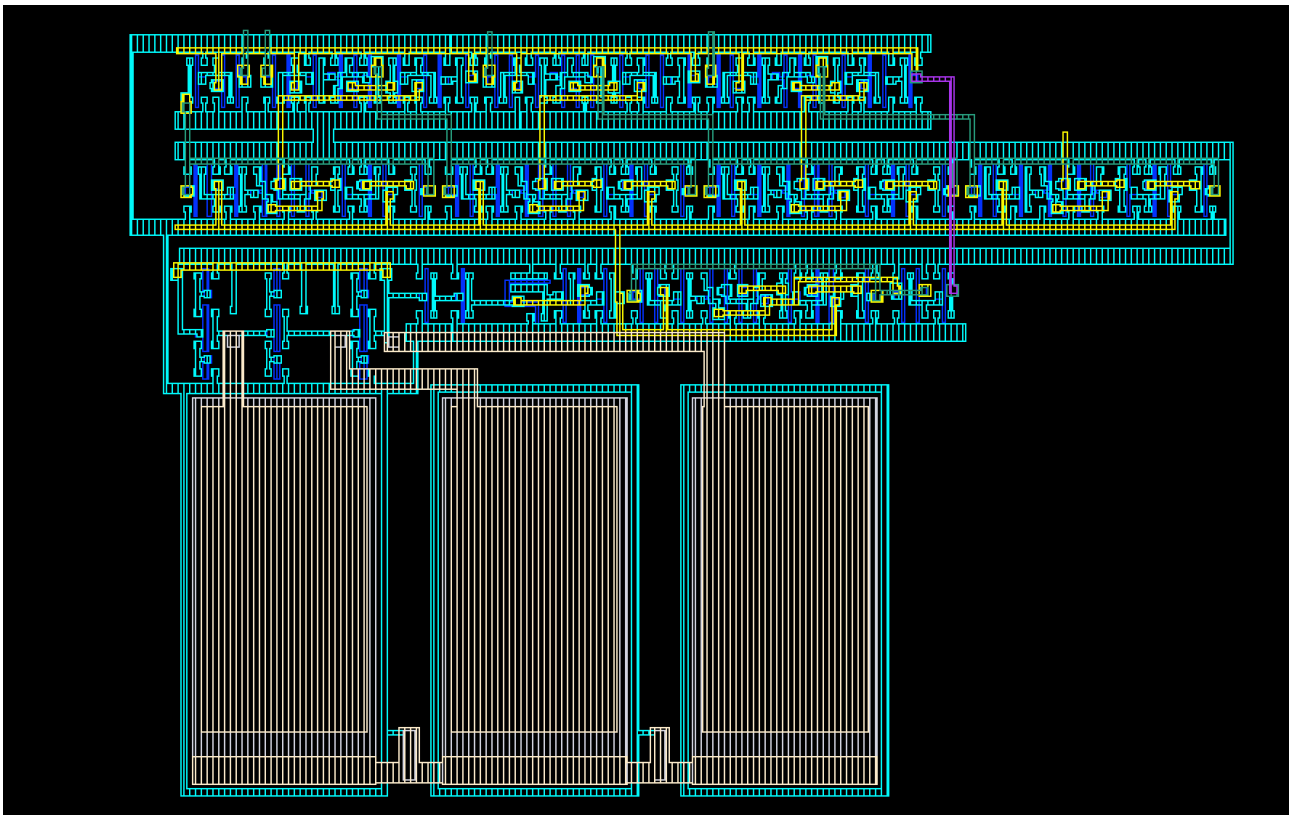
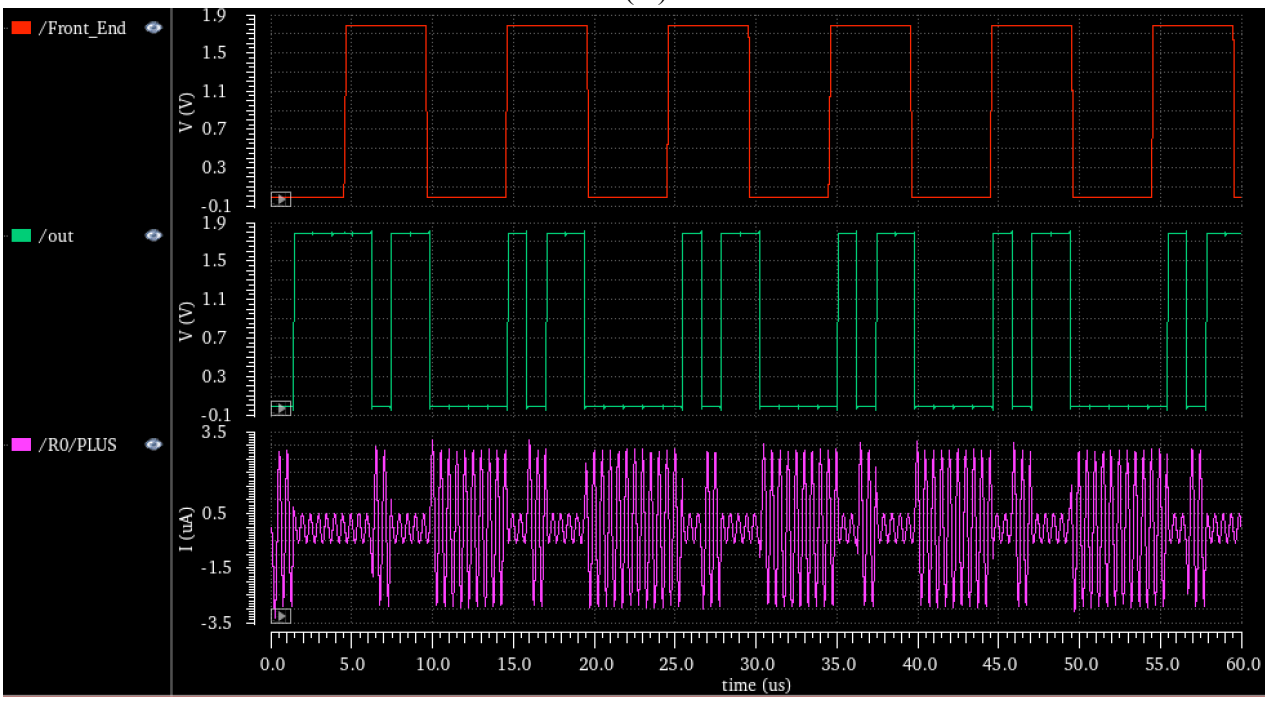


Fig. 5.3: Extracted view of the full-circuit.

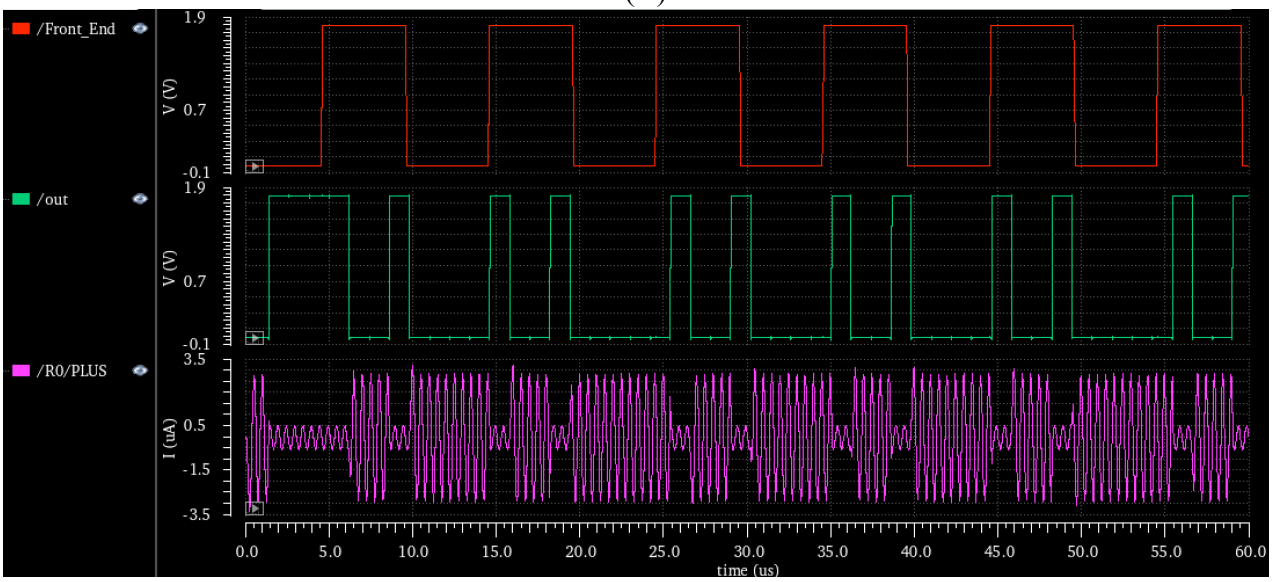
5.1 POST-LAYOUT SIMULATIONS

At this point three transient simulations are shown in the following Fig. 5.4, as examples of the functioning of the chip. Three different chip addresses are set for the parallel inputs (i.e. 1011, 1001, 1111) in order to test the circuit by different inputs.

(A)



(B)



(C)

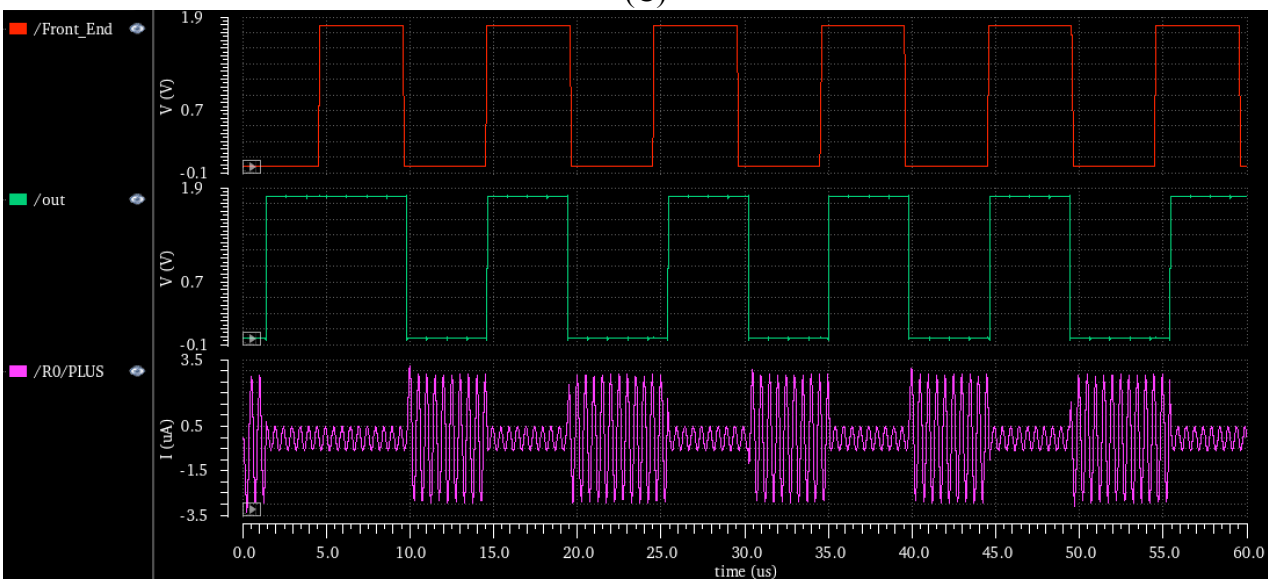


Fig. 5.4: Three simulation of the full-circuit with three different packet templates: 1011 (A), 1001 (B) and 1111 (C).

In each simulation, the pink wave is the one that perform the proper ASK modulation and, so, in an ideal case, without losing medium, is the one received as scattered wave by the external base station. With a simple analysis of the pink signal, it is easy to extract the packet template while it is possible to obtain the frequency (the real important information to achieve) by measuring the distance between two identical packet templates.

5.2 CURRENT EXTRACTION EXAMPLE

At this point I want to simulate a bi-acquisition of two different signal from two different biosensors, glucose and lactate in particular. The aim of the simulation is to imagine that the two signals have been treated through the multiplexing layer and so two different signal address are provided at the register inputs.
The next Fig. 5.5 presents exactly this situation with two different packet templates (1101 and 1001) inserted into the PISO Input signal conditioning.

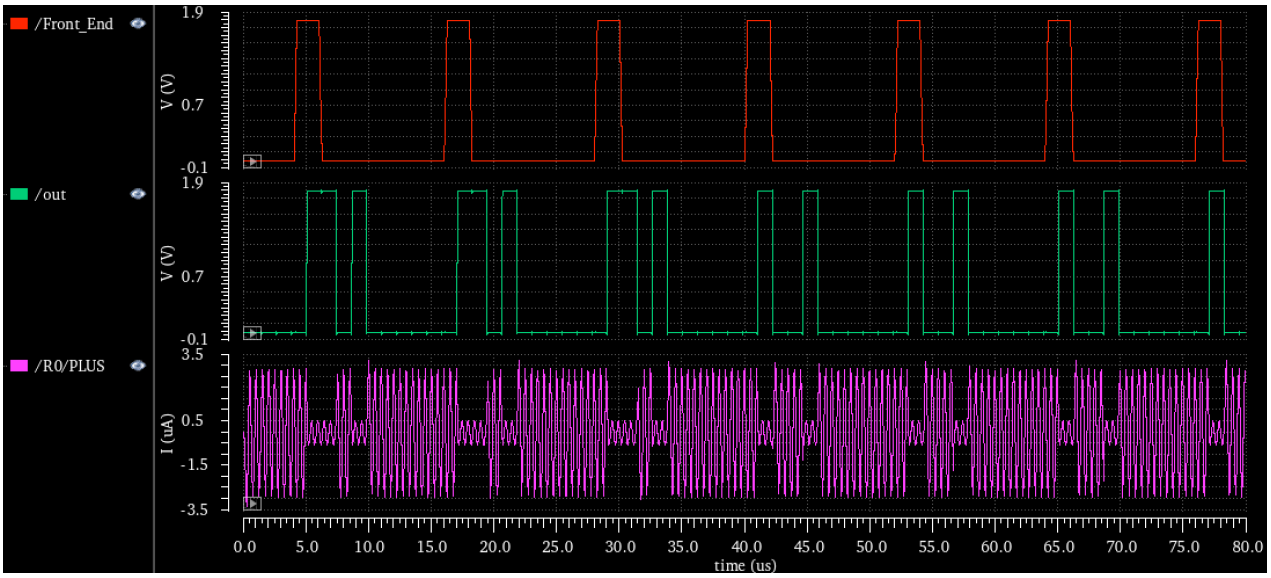


Fig. 5.5: Full-circuit transient analysis with two different packet templates (1101 and 1001).

By analyzing the pink wave (Fig. 5.6) is so possible to extract the desirable informations.

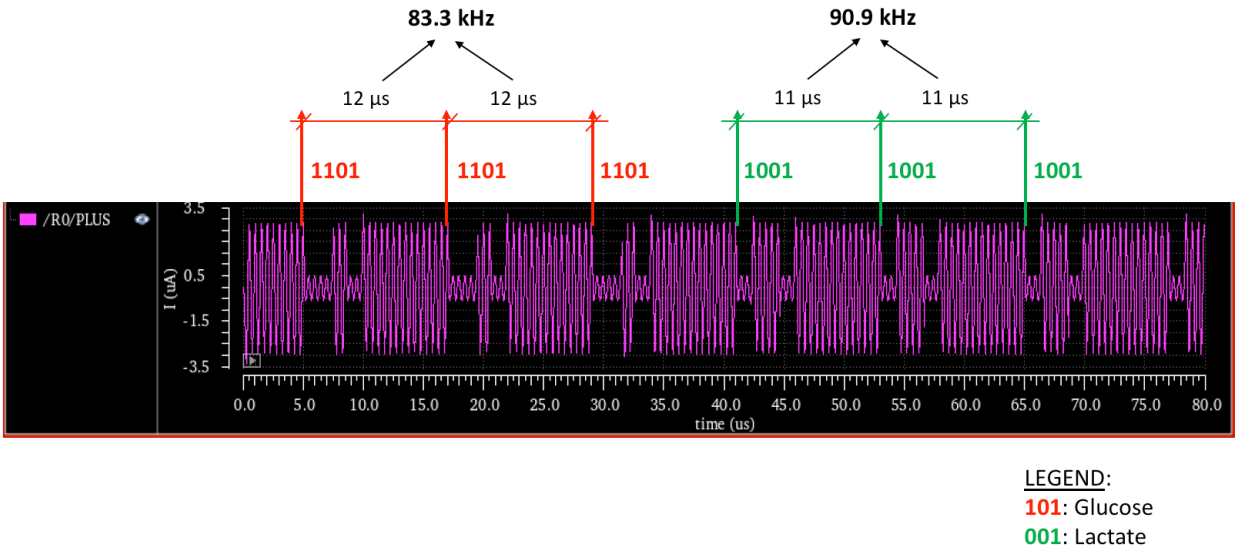


Fig. 5.6: Different frequency for two different signals extracted and modulated.

Glucose signal oscillates at 83.3 kHz while lactate one at 90.9 kHz. Assuming, as the previous article [2.17] asserts, that the sensibility of the current to frequency converter is something like 7 kHz/nA:

- Glucose: 11.90 nA measured by the glucose sensor.
- Lactate: 12.99 nA measured by the lactate sensor.

At this point, knowing the relationship between the current and the concentration of the molecules (that is known by the proper sensors) is possible to calculate the real concentration of them during time (Table 5.1).

Sensors sensitivity: 1.8 $* 10^{-7}$ $A/mmol * mm$

VCO sensitivity: 7 kHz/nA

Address	Signal	Measured Freq.	Current	Concentration
1+101	GLUCOSE	83.3 kHz	11.90 nA	0.066 mmol * mm
1+001	LACTATE	90.9 kHz	12.99 nA	0.072 mmol * mm

Table 5.1: Reconstruction of molecules concentration example.

As already wrote, it is possible to put the modulator in series with the transducer and then obtain the dual situation with respect to that described in Fig. 5.6: the amplitude modulation is achieved during the transmission of the bit 0 and fully matched condition during the transmission of the bit 1.

5.3 TEMPERATURE SWEEPING

Because of the ring oscillator is temperature dependent, also the full-circuit will be influenced by temperature as well. What is important to test now is that all works by sweeping the temperature with the previous tested range, between 27°C and 47°C (Fig. 5.7).

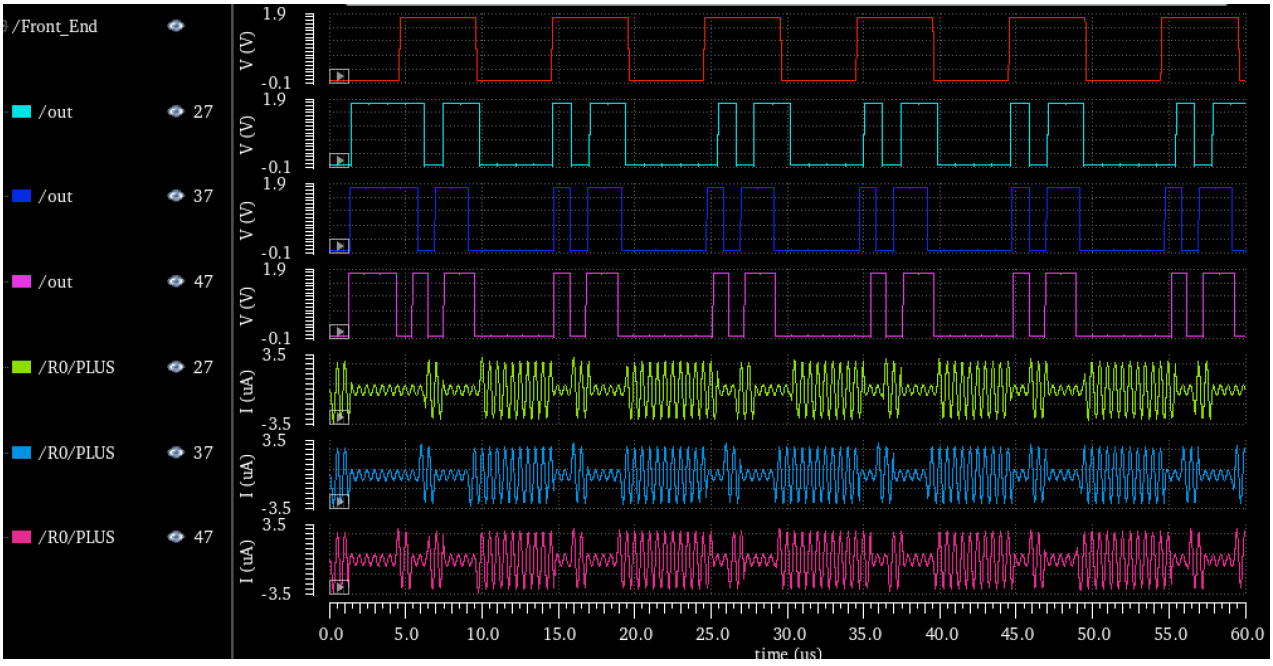


Fig. 5.7: Full-circuit working with temperature sweeping between 27°C and 47°C.

The circuit works correctly despite the little variations of the center frequency by the ring oscillator caused by temperature increment.

5.4 POWER CONSUMPTION

First of all, in the following Fig. 5.8, the total power consumption of the full circuit is compared with the temperature sweeping.

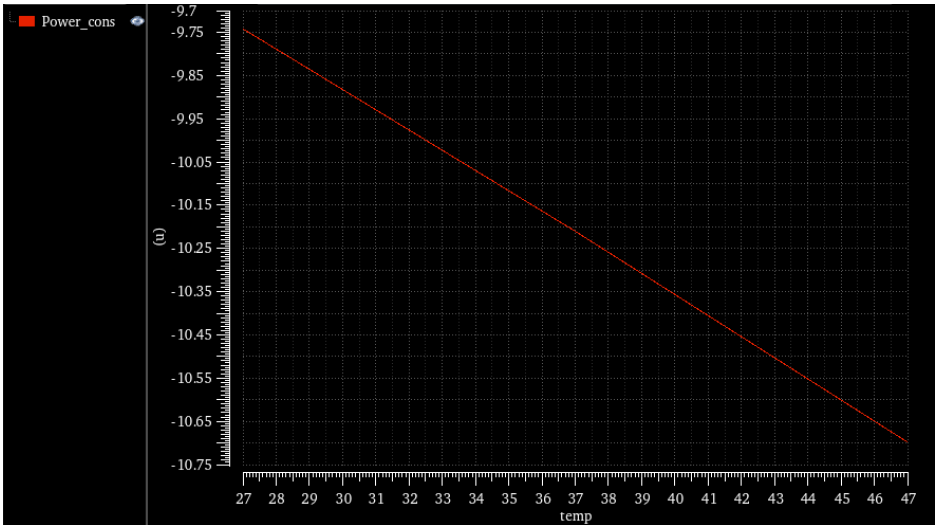


Fig. 5.8: Full-circuit power consumption VS temperature sweeping.

As the previous graph highlights, the total average power consumption is slightly higher than the power that is required by the ring. This is an expected result since all the circuit is off (transistors turned off) except when a rising edge of the front-end occurs, while the ring oscillates continuously during time. The next pie chart (Fig. 5.9) shows the power consumption related to all the circuit blocks and shows that the starved ring oscillator requires 98 % of the total power consumption.

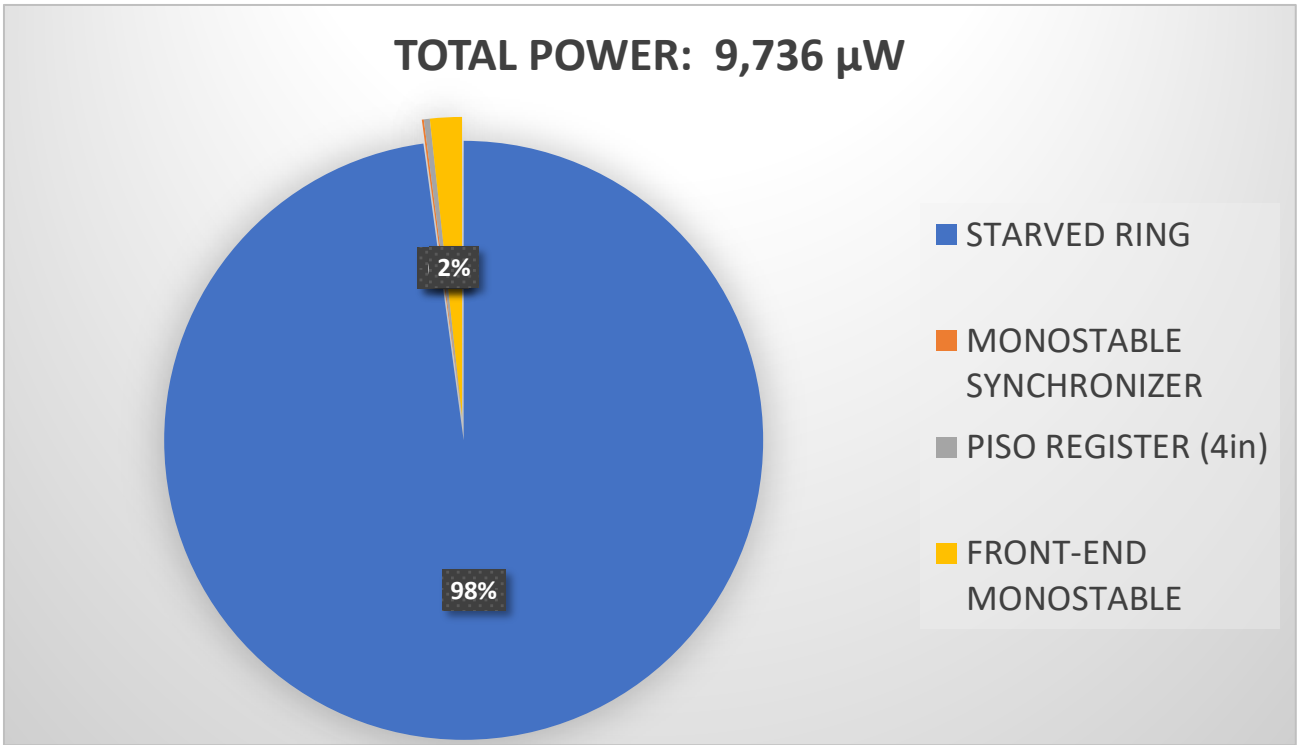


Fig. 5.9: Pie chart for power consumption.

The power figure (9.7 µW) is extreme positive and it can goes down at least of one order of magnitude by redesigning the oscillator only.
In reality, another important consideration needs to be done in this case: the averaged power consumption in "sleep mode" is not so important since the chip does not have any battery (it is supplied wirelessly), while what is key to be analyzed is the instantaneous power consumption for every oscillation.

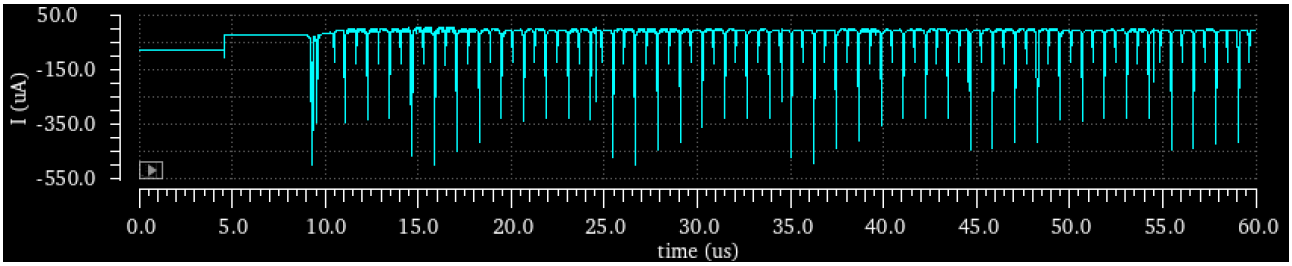


Fig. 5.10: Instantaneous power consumption of the full-circuit.

As is shown in the Fig. 5.10, the instantaneously power required to transmit is very high, and also the power needed to supply the oscillator is high: more precisely 450 µA/pulse are needed to transmit every bit and 350 µA/pulse are needed to grant the oscillation. The provided voltage supply is 1.8 V and, therefore, these values become almost 810 µW/pulse for the transmission, of which 630 µW are needed for the oscillation. This could be a real problem, the top important problem to focus on in order to guarantee a proper working of the circuit.
Nevertheless, the obtained results in terms of power are compared, in the following Table 5.2 with the work [4.7] from which the electrical model of the transducer was taken.

Parameters	**Comparison**	
	Ref. [4.7]	***This work***
Modulation	LSK	OOK
Average Power (µW)	49	9.7
Instant- Power (mW)	3.2	0.81

Table 5.2: Modulation comparison.

Table 5.2 presents a comparison with [4.7] which demonstrates that the here proposed OOK modulation-based implementation shows a 80% reduction in the average power consumption and also a 75% reduction in instant power.
Therefore, this aspect of a reduction of the instantaneous power consumption necessarily is the next step to be done before the final design and, then, fabrication of a first prototype in order to test the chip in real condition of work.

5.5 OCCUPIED AREA

The other important parameter for the aim of this project is the total size required by the designed circuit. Before analyzing more in detail the percentage of occupied area for each block, I want to show the full circuit layout with the graphical partition for each component (Fig. 5.11).

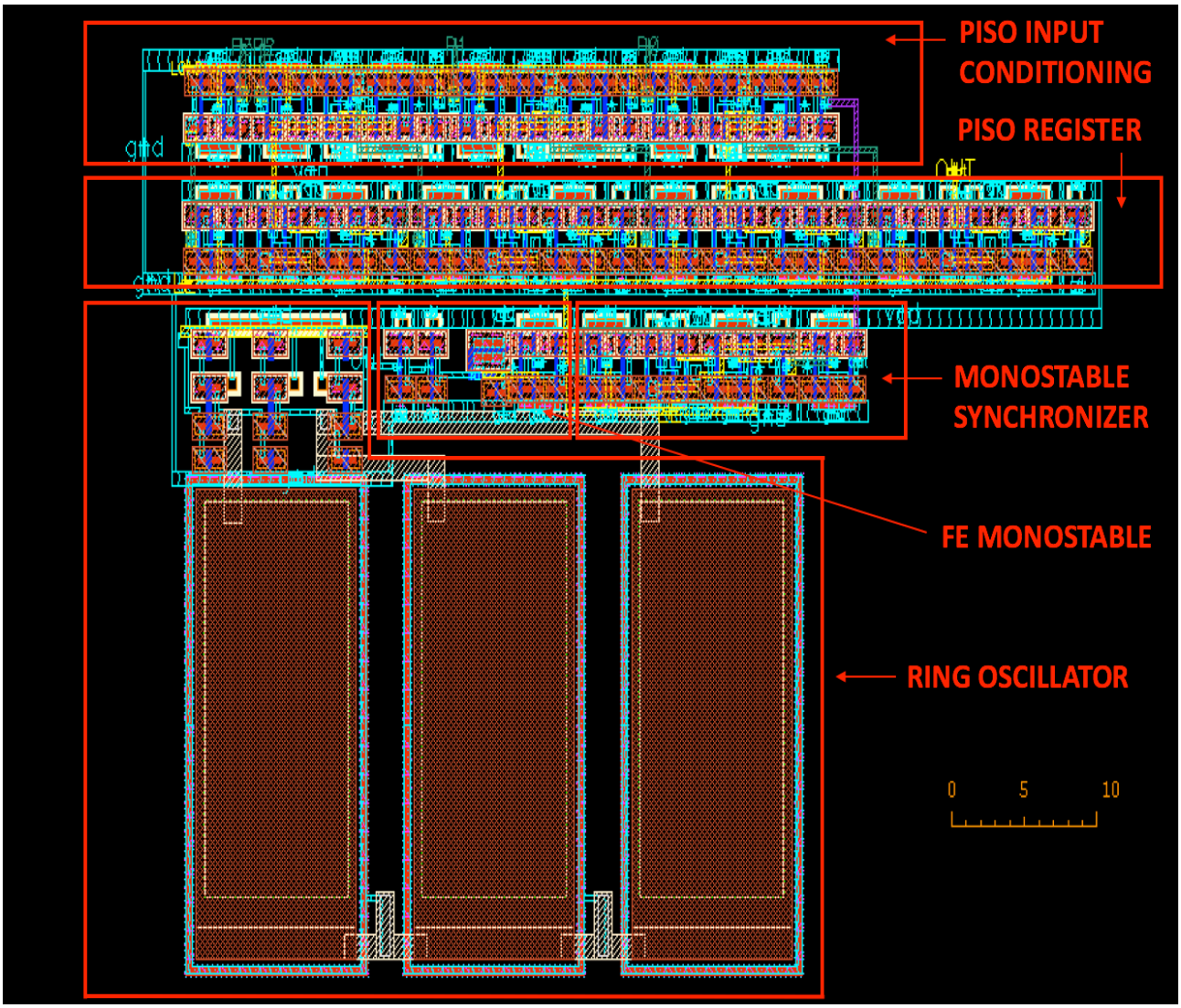


Fig. 5.11: Full-circuit layout with the partition of the occupied area.

In the following Fig. 5.12 the percentage of occupied area for each block of the communication system is depicted.

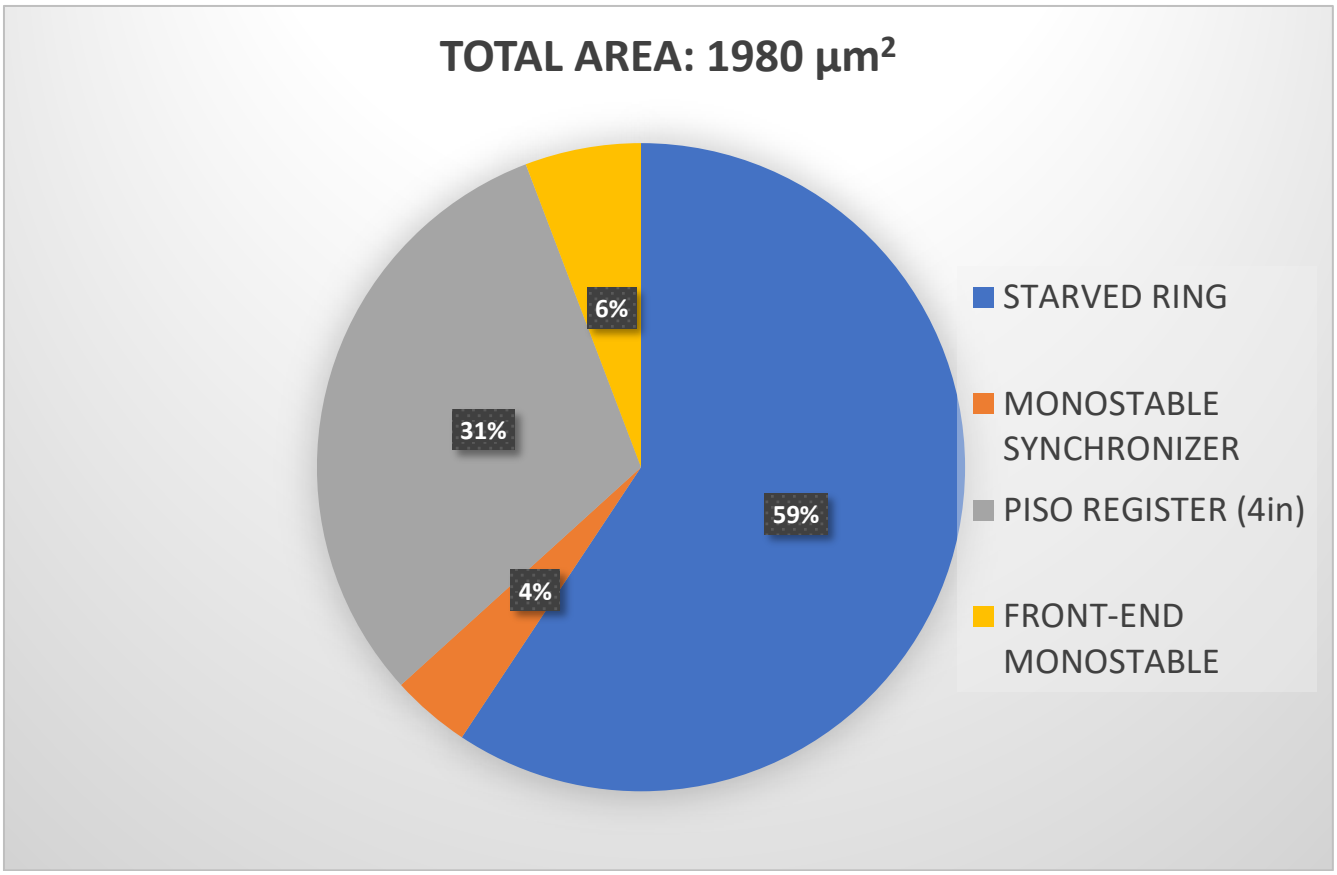


Fig. 5.12: Pie chart for occupied area.

Again, the chart demonstrates as the ring oscillator occupies the majority of the area. The total area is bigger than the desirable one but, in this phase of the research, it is important to understand which block is possible to optimize in order to reduce the sizes. The obtained results are then very significative because they have clearly shown that the ring oscillator is the most critical block, on which work need to focus in future in order to reduce both size and power consumption.

CHAPTER 6

CONCLUSIONS

During this work I present a new concept of CMOS biosensing technology, to design a biosensing chip small enough to be drinkable for in-body diagnostics: called "Body Dust". This proposed new concept will have eventually a big social and economic impact at least on three main socio-economic groups: IC industry, biomedical system community and pharma industry as well.
In particular in diagnostic, new concepts such as home diagnostics health care and remote monitoring are emerging. So, completely new class of autonomous devices is required for commercialization and this is reflected on the new characteristics that these devices need to have. First of all, the equipment needs to support portability, reduced size, low-costs in fabrication, low-power consumption, wireless data transmission, easy-to-use and fully autonomous functions.
"This new emerging market is estimated to reach US $47.40 billion by 2020 with an annual growth rates for investments of around 6% in the period 2016-2020" [2.1].

Even though the research on "Body Dust" is just at the beginning and, then, more deep analysis are still needed in order to prepare the IC to the first prototyping stage, a starting point is made and all of the issues have been investigated, in particular, considering in this master project, the related communication circuit.
In this thesis, a novel architecture for data transmission in "Body Dust" diagnostics has been presented. The results of such feasibility study have demonstrated the possibility to design an architecture for a data transmission transponder by using a 0.18-μm CMOS process, with an average power consumption of less than 10 μW and a total chip area of 43x44 μm^2. Even though we have implemented the design of a starved architecture, the study has shown that the source of major power and area consumption is the ring-oscillator. The obtained results seem to be feasible and acceptable as well, now is possible to start with the optimization step: starting from the ring oscillator (simulated to be the first component in terms of power consumption and sizes). It is also possible, as I mentioned, to scale all the circuit with a smaller node size (e.g., with CMOS 65 nm or smaller).
For what concern optimization, in [6.1] a differential ring is designed with less than 24 nW of consumption, obtained reducing the power supply to 0.3 V and so working on sub-threshold.
Is also possible to think about a distortion of the proposed architecture by removing completely the oscillator and so studying other methods to create the data bit and so to perform the modulation.
The last suggestion could be simplifying the system, removing all the communication circuit as it is, saving so up both area and power consumption, inserting only a switch as a modulator: this is the solution proposed by Maharbiz in [4.10] for neural dust application.

In any case, the research in the area of "Body Dust" is identifying new technological challenges that are addressing important aspect in the CMOS design, in order to make it real its realization in the next future!

BIBLIOGRAPHY

Chapter 2

[2.1] Sandro Carrara and Pantelis Georgiou, "Body Dust: Miniaturized Highly-integrated Low Power Sensing for Remotely Powered Drinkable CMOS Bioelectronics, IEEE Conference BioCAS, 2017.

[2.2] Ghoreishizadeh, S. S., Baj-Rossi, C., Cavallini, A., Carrara, S., & De Micheli, G. (2014). An integrated control and readout circuit for implantable multi-target electrochemical biosensing. *IEEE transactions on biomedical circuits and systems*, *8*(6), 891-898.

[2.3] Humphrey, J. D., Dufresne, E. R., & Schwartz, M. A. (2014). Mechanotransduction and extracellular matrix homeostasis. *Nature reviews Molecular cell biology*, *15*(12), 802.

[2.4] Rothe, J., Frey, O., Stettler, A., Chen, Y., & Hierlemann, A. (2014). Fully integrated CMOS microsystem for electrochemical measurements on 32× 32 working electrodes at 90 frames per second. Analytical chemistry, 86(13), 6425-6432.

[2.5] Baj-Rossi, C., Cavallini, A., Kilinc, E. G., Stradolini, F., Jost, T. R., Proietti, M., ... & Carrara, S. (2016). In-vivo validation of fully implantable multi-panel devices for remote monitoring of metabolism. *IEEE transactions on biomedical circuits and systems*, *10*(5), 955-962.

[2.6] Balasubramanian, V., Ruedi, P. F., Temiz, Y., Ferretti, A., Guiducci, C., & Enz, C. C. (2013). A 0.18$\mu {\rm m} $ Biosensor Front-End Based on $1/f $ Noise, Distortion Cancelation and Chopper Stabilization Techniques. *IEEE transactions on biomedical circuits and systems*, *7*(5), 660-673.

[2.7] Stanacevic, M., Murari, K., Rege, A., Cauwenberghs, G., & Thakor, N. V. (2007). VLSI potentiostat array with oversampling gain modulation for wide-range neurotransmitter sensing. *IEEE Transactions on Biomedical Circuits and Systems*, *1*(1), 63-72.

[2.8] Yang, C., Huang, Y., Hassler, B. L., Worden, R. M., & Mason, A. J. (2009). Amperometric electrochemical microsystem for a miniaturized protein biosensor array. *IEEE transactions on biomedical circuits and systems*, *3*(3), 160-168.

[2.9] Jafari, H. M., & Genov, R. (2013). Chopper-stabilized bidirectional current acquisition circuits for electrochemical amperometric biosensors. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *60*(5), 1149-1157.

[2.10] Taurino, I., Magrez, A., Matteini, F., Forró, L., De Micheli, G., & Carrara, S. (2013). Direct growth of nanotubes and graphene nanoflowers on electrochemical platinum electrodes. *Nanoscale*, *5*(24), 12448-12455.

[2.11] Baj-Rossi, C., Kilinc, E. G., Ghoreishizadeh, S. S., Casarino, D., Jost, T. R., Dehollain, C., ... & Carrara, S. (2014). Full fabrication and packaging of an implantable multi-panel device for monitoring of metabolites in small animals. *IEEE transactions on biomedical circuits and systems*, *8*(5), 636-647.

[2.12] C. Boero, S. Carrara, G. De Micheli, in Biomedical Circuits and Systems Conference (BioCAS), 2011 IEEE. (IEEE, 2011), pp. 357-360.

[2.13] Taurino, I., Sanzó, G., Mazzei, F., Favero, G., De Micheli, G., & Carrara, S. (2015). Fast synthesis of platinum nanopetals and nanospheres for highly-sensitive non-enzymatic detection of glucose and selective sensing of ions. *Scientific reports*, *5*, 15277.

[2.14] Harpster, T. J., Nikles, S. A., Dokmeci, M. R., & Najafi, K. (2005). Long-term hermeticity and biological performance of anodically bonded glass-silicon implantable packages. *IEEE Transactions on Device and Materials Reliability*, *5*(3), 458-466.

[2.15] Atanasov, P., & Wilkins, E. (1993). Glucose biosensor based on oxygen electrode. Part I: silastic coated polycarbonate membranes for biosensor application. *Analytical letters*, *26*(8), 1587-1612.

[2.16] Yu, B., Ju, Y., West, L., Moussy, Y., & Moussy, F. (2007). An investigation of long-term performance of minimally invasive glucose biosensors. *Diabetes technology & therapeutics*, *9*(3), 265-275.

[2.17] Snoeijs, J., Georgiou, P., & Carrara, S. (2017, October). CMOS body dust—Towards drinkable diagnostics. In *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)* (pp. 1-4). IEEE.

Chapter 3

[3.1] Catherine Dehollain, EPFL, Lausanne, Switzerland: slides of the course "Analog Circuits for biochip".

[3.2] Stockman, H. (1948). Communication by means of reflected power. *Proceedings of the IRE*, *36*(10), 1196-1204.

[3.3] K. Kapucu, J.L. Merino, C. Dehollain, PRIME Conference in June 2013 and ICECS Conference in Dec. 2013.

[3.4] K. Kapucu , C. Dehollain: 4 conference papers at PRIME 2014, RFID-TA 2014, RFID 2015, RFID 2017.

[3.5] Azizighannad, M. (2014). *Remotely-Powered Batteryless Implantable Local Temperature Monitoring System for Freely Moving Mice* (No. THESIS). EPFL.

[3.6] Karthaus, U., & Fischer, M. (2003). Fully integrated passive UHF RFID transponder IC with 16.7-/spl mu/W minimum RF input power. *IEEE Journal of solid-state circuits*, *38*(10), 1602-1608.

[3.7] Curty, J. P. (2006). *Analysis and optimization of passive UHF RFID systems* (No. THESIS). EPFL.

[3.8] Wong, A. C. W., Kathiresan, G., Chan, C. K. T., Eljamaly, O., Omeni, O., McDonagh, D., ... & Toumazou, C. (2008). A 1 V wireless transceiver for an ultra-low-power SoC for biotelemetry applications. *IEEE Journal of Solid-State Circuits*, *43*(7), 1511-1521.

[3.9] Curty, J. P., Declercq, M., Dehollain, C., & Joehl, N. (2006). *Design and optimization of passive UHF RFID systems*. Springer Science & Business Media.

Chapter 4

[4.1] Baker, R. J., & Boyce, C. M. O. S. (2005). Circuit design, layout, and simulation. *IEEE Press Series on Microelectronic Systems*.

[4.2] Griffith, D., Røine, P. T., Murdock, J., & Smith, R. (2014, February). 17.8 A 190nW 33kHz RC oscillator with±0.21% temperature stability and 4ppm long-term stability. In *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)* (pp. 300-301). IEEE.

[4.3] Jahan, M. S., & Holleman, J. H. (2010, December). An ultra-low-power 400 MHz VCO for MICS band application. In *International Conference on Electrical & Computer Engineering (ICECE 2010)* (pp. 318-321). IEEE.

[4.4] Al, A., Bin Ibne Reaz, M., Jalil, J., Alauddin, M., & Ali, M. (2015). Design of a low-power flash analog-to-digital converter chip for temperature sensors in 0.18 μm CMOS process. *Acta Scientiarum. Technology*, *37*(1).

[4.5] Ros, P. M., Crepaldi, M., Bonanno, A., & Demarchi, D. (2013, September). Wireless multi-channel quasi-digital tactile sensing glove-based system. In *2013 Euromicro Conference on Digital System Design* (pp. 673-680). IEEE.

[4.6] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital integrated Circuits, 2nd ed. Englewood Cliffs: Prentice Hall, 2002.

[4.7] Mazzilli, F., Kilinc, E. G., & Dehollain, C. (2014, October). 3.2 mW ultrasonic LSK modulator for uplink communication in deep implanted medical devices. In *2014 IEEE Biomedical Circuits and Systems Conference (BioCAS) Proceedings* (pp. 636-639). IEEE.

[4.8] Mazzilli, F., Lafon, C., & Dehollain, C. (2014). A 10.5 cm ultrasound link for deep implanted medical devices. *IEEE transactions on biomedical circuits and systems*, *8*(5), 738-750.

[4.9] Weber, M. J., Yoshihara, Y., Sawaby, A., Charthad, J., Chang, T. C., & Arbabian, A. (2018). A miniaturized single-transducer implantable pressure sensor with time-multiplexed ultrasonic data and power links. *IEEE Journal of Solid-State Circuits*, *53*(4), 1089-1101.

[4.10] Dongjin Seo, Jose M. Carmena, Jan M. Rabaey, Elad Alon and Michel M. Maharbiz, "Neural Dust: An Ultrasonic, Low Power Solution for Chronic Brain Machine Interfaces", July 2013.

Chapter 6

[6.1] Farzeen, S., Ren, G., & Chen, C. (2010, August). An ultra-low power ring oscillator for passive UHF RFID transponders. In *2010 53rd IEEE International Midwest Symposium on Circuits and Systems* (pp. 558-561). IEEE.