POLITECNICO DI TORINO

Facolta' di Ingegneria Elettronica

Master degree course in Sistemi Elettronici

Master Degree Thesis

Design of a low-power, low-cost leaf wetness sensor for smart agriculture application

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This work was realized following my absolute passion for electronics

Summary

In the recent years, it has become more and more important to imply new technologies for monitoring agriculture; the continuous research of better results brought farmers to look for new systems, which imply wireless sensor networks.
Actually plantations have reached an extension too big to be efficiently monitored with traditional methods, therefore "Precision Farming" founds a very interesting application in this new panorama. Thanks to it, almost independently on how big is the area to be monitored, it is possible to have a complete view of how the crops are behaving, saving much time and resources.
"Ixem Wine" consists in a project born at iXem Labs, a research laboratory in Politecnico of Turin, which aims at providing the farmers with innovative systems for precision farming, in order to help them to monitor vineyards growth.
Among sensors implied for precision farming, leaf wetness sensor is of particular interest, since it allows to forecast and avoid issues and plant diseases like "peronospora viticola" and mold formation, which could be hardly predictable in other ways.
The aim of the thesis work is therefore to design a prototypal version of Leaf Wetness Sensor, to be implied in monitoring vine health status, following low-cost and low-power specifications.
The starting point of the project was to choose the implementation technology; two principles could be exploited: resitive or capacitive.
A resistive LWS acs as an electrical resistance, which gets modified by the presence of a conductive material over it, when the surface is dry, maximum resistance is achieved and the sensor measures 0 percent of leaf wetness. If instead the traces of the sensor are put in contact by water droplets, since rain water and dew are more conductive than the air, the resistance of the sensor drastically drops, leading to 100 percent of measured leaf wetness.
This binary behaviour makes resistive sensors to be unsuitable for the thesis project, since a much higher resolution is required.
Therefore for reliability purpose, the capacitive technology was exploited.
Capacitive working principle is different from resisitve one: the presence of a material between two or more conductors that overlap for a certain area, creates a

capacitive coupling between them, therefore an equivalent electrical capacitance can be evaluated.
Such sensor is capable of performing a measurement of the relative water content on its surface, measuring the sensor's electric capacitance, which is modified by the permittivity change of the material present on it. As it can be noticed from figures 3 and 4 both sensors are similarly realized. They consist of two interdigital electrodes, made in mictrostrip techology, separated by a certain spacing.
In the design of the sensor it was adopted also another choice: the interdigital pattern was thought to be present on both top and bottom sides of the sensor, to be capable of measuring water content also on the rear side, which, since it is less exposed to the sun light, has a lower chanche to get completely dry and therefore to increase mold formation risk.
After understanding the physical principle of interdigital capacitors, simulations were performed by mean of "COMSOL multiphysics", a partial differential equation solver with an integrated CAD-like tool.
The candidate created a realistic physical model of the capacitive network and performed electrostatic analyses for different pattern configurations. The model was designed as a couple of interdigital electrodes, with every finger separated from the other by a specific distance. Then the tool was implied to solve a differential problem providing the electrical capacitance as output.
The parameter that mostly influenced the simulation results was, as expected, the dielectric constant of the material superposed to the sensor. It was observed a behaviour reasonably compatible with theoretical calculations: the higher the electric permittivity, the higher the capacitance. A parametric sweep allowed to swap materials, choosing between air and water.
Moreover the water content percentage was simulated, ranging from 0 percent of covered area to 100 percent with steps of 25 percent.
Concerning the trace spacing, it is known from electrostatics theory that the electrical capacitance is inversely proportional to the trace spacing and directly proportional to the number of metal theet of the sensor. In the performed simulations the candidate analyzed also this aspect, designing two different patterns, which differ in the spacing distance and number of theet: in the first model the ratio between trace width and spacing is unitary, while for the second pattern this ratio is doubled. As expected from theory, the capacitance of the two patterns changes by a factor four.
The sensor's board was designed following the simulation models, integrating on each side a capacitive pattern, comprehensive of four 0 ohm resistances which were reserved to manual mounting or unmounting.
This artifice allowed to imply the three arbitrairly choosable measurement systems included on the board to measure either sensor's side, with either measurement system.

The candidate chose to imply an RC charging and discharging circuit as first measurement system.
A 500 ms wide step signal is provided by a GPIO of pin of an STM32 microcontroller at the input terminal, the interdigital capacitor, which is connected through a terminal gets charged through the charge and discharged through the discharge resistance.
A different capacitance changes the discharge curve of the capacitor, since it varies the time constant of the circuit. The piece of circuit after the discharging path is a voltage comparator, useful to raise an interrupt signal as soon as the discharge voltage reaches the threshold given by the Zener diode D1.
The second idea was to compute the capacitance by mean of an LMC555 timer in a-stable configuration. In this case the output waveform frequency of the LMC555 IC, which is proportional to the capacitance, was measured.
Two resisitances fix the thresholds of the voltage comparator contained in the timer. The node between the two resistances is connected to the discharge pin, while the device is made auto-triggering by connecting threshold and trigger pins.
As third measurement system was implied an high resolution and high noise immunity FDC sensor by Texas Instruments, which directly provides on I2C bus the measured capacitance.
An LC resonatoing circuit in which is inserted the measurand capacitance is put externally to the FDC integrated circuit converter. The capacitance to digtal converter excites through a driving current the LC tank and reads back the oscillation frequency of the sensor.
Each component was soldered by hand, using the available instrumentation; Finally measurements were performed.
The FDC method,as expected, provided the most reliable results.

Contents

List of Tables

List of Figures

Part I

Introduction and Project overview

Chapter 1

General introduction

1.1 Thesis objective

The aim of the thesis work is to realize a prototypal version of a low cost and low energy consuming sensor, to be implied for detecting the presence of water on vine leafs' surface. Such sensor, as it will be explained in further detail, ought to be based on a capacitive measurement: the electric permittivity of a medium which covers the sensor's surface leads to an electrical capacitance whose value strictly depends on the material. In this way material change can be sensed and timely measures can be carried out.

1.2 Developement context

The thesis activity was entirely supported by the iXem Labs, in electronics and telecommunication departement (DET) of Politecnico of Turin, under the lead of professor Daniele Trinchero and his team of researchers. Once a week the candidate took appointments with hardware designer Mattia Poletti, in order to refer him weekly updates about the work done at home and get new jobs once the previous ones were completed. Moreover, all practical measurements were performed in the electronics laboratory nearby the iXem Labs, since a more specific equipement was needed in order to perform all the required steps.

1.3 Nowadays agriculture

Technological innovations such as Wireless sensor networks and Internet of things have recently being implied in agriculture world. This allowed the farmers to improve crop quality and to optimize resources thanks to have a complete monitoring of their own plantations. The innovation process started finding a way to completely map the plantations and to insert them into a network, which could be potentially viewed and managed from each device connected to the online platform.
Such an enhanced kind of agriculture has the capability to overcome some of the limits which are normally considered real issues, for instance molds formation risk, plant diseases, icing of the crop and poor optimization of the resources such as water and products well.
It has become clearer and clearer that a plantation which can be completely monitored by its owner, has a lower chance to suffer for the above cited issues.

1.4 Innovative contributions of the thesis work

Different sensor are implied in precsion farming systems, in order to monitor environmental parameters like temperature, wind direction or soil moisture. Another kind of sensor, which has been recently introduced by companies that are involved in smart agriculture, is the leaf wetness sensor (LWS). Such sensor allows to monitor the water coverage of leafs' surface by mean of an electronic measurement.
The sensor can in fact be attached nearby other leafs and act as a sample that could get wet or dry as real leafs do, showing the wetness of the plant.
An array of sensors, placed in proper position could provide a complete mapping of the whole plantations: by monitoring network nodes farmers can have a dedicated view of each node, highlighting the ones at major risk.
The most common vine plant disease is the "peronospora viticola" which is caused by "plasmopara viticola" agent, which manifests whenever the leaf surface stays wet for a certain period of time and under certain temperature condition.

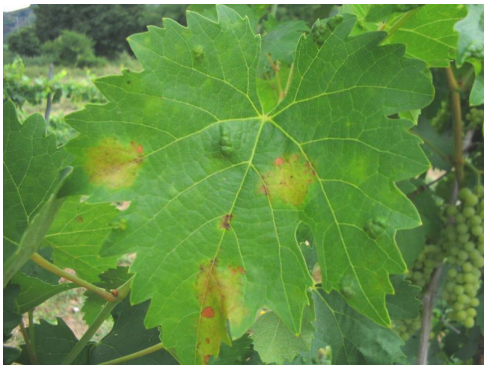


Figure 1.1: Manifestation of "peronospora viticola" on vine leaf, the most common disease due to leaf wetness duration

Chapter 2

The iXem project

Precision Farming System

Links to iXem Labs:
http://www.det.polito.it/it/the_department/internal_structures/research_labs/ixem_laboratory

Links to iXem Wine platform:
https://ixem.wine

2.1 iXem wine

"iXem wine" is a project born at the iXem Labs in Politecnico di Torino. It is composed by professor Daniele Trinchero and his team of researchers and occupies about precision farming.
The project aims at providing vineyards owners a wirless sesor network (WSN) service, to be implied in monitoring grape plantations. Farmers can register on the "iXem wine" network platform and login, gaining access to sensor's measurements in various locations.

Anyone registered in iXem's database can access the online plaform and have the possibility to monitor the status of the whole vineyard. This is possible thanks to the installation of different sensors, capable of communicating to a network server the collected information. This clearly implies a wireless connection, which is achieved by mean of a radio bridge, implemented exploiting the LoRa protocol.

2.2 Wireless Sensor Network

Sensors are placed on one vine plant among others, in this way, each of them circumscribes a node of the sensor network. An hardwired connection links the sensors to a processing-transmitting board, designed by iXem Labs, which has the scope to collect data and send them to the online network platform via an uplink.

2.2.1 iXem board

In order to exploit the wireless connection, it is soldered on the PCB of the iXem board the CMWX1ZZABZ MuRata chipset, which integrates in a single package an ultra low power STM32L0XX microcontroller and a Semtech's SX1276 LoRa transceiver.

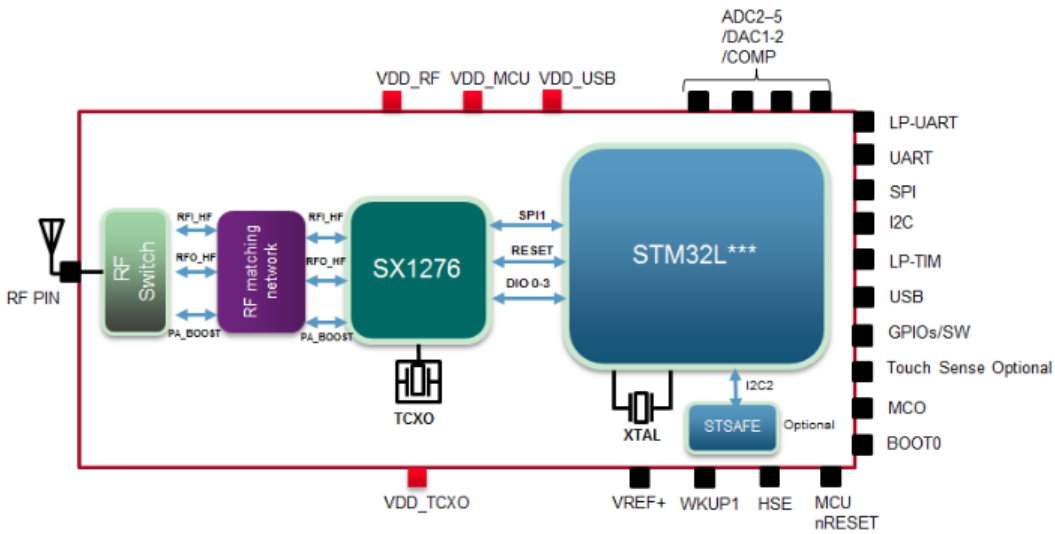


Figure 2.1: MuRata Type ABZ wireless module block diagram

For the purpose of the thesis work, the system designed by the candidate interacted only with the microcontroller part, more precisely with the I2C peripheral and some GPIOs pins mapped to perform different tasks, such as receive interrupt signals or periodic signals for evaluating their frequency.
Recalling that the system, object of the thesis work was designed as a prototypal version of the end product, different measurement systems were implemented on a single printed circuit.

The front view of the iXem board is presented in figure 2.2.

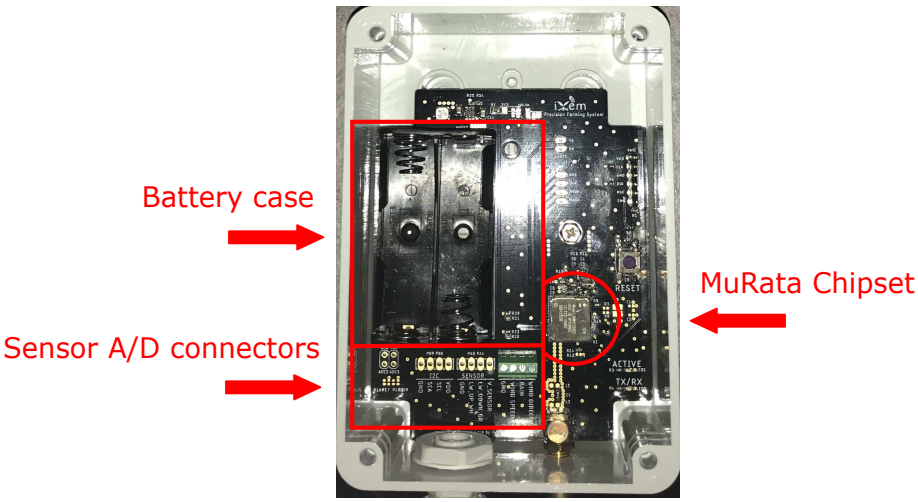


Figure 2.2: iXem's board

As it can be noticed, the red patterns enlight the components and the connections which are of major interest for the thesis seek.
First of all the iXem's device gets the supply from a couple of 1.5V AA batteries, this perfectly meets the low-power constraints of the IOT.
Second, the MuRata chipset allows long range wireless communication with the LoRa access point, in this way it is possible to reach a very large area of covering.
The third point consists in sensor connectors, which permit to the various sensors to interact with the STM32 microcontroller.
Since the LWS realized for the thesis work mounts a connector specifically designed for communicating collected data to the board, the connector part of the iXem board may have to be redesigned.

2.2.2 Wirelss communication protocol

LoRaWAN is the media access control (MAC) protocol which was chosen by iXem Labs team in order to perform the data transmission to the online network. It is specifically suitable for wide area networks and it is designed to allow low-powered devices to communicate with Internet-connected applications over long range wireless connections. In order to better clarify the features of LoRaWAN protocol a more detailed description of such technology is reported in Appendice A.

Chapter 3

LWS Project characterisitics

In the following sections are reported the given project specifications, which should satisfy the iXem project requirements.

3.1 Low power constraint

Since the iXem board is supplied only by a DC internal source, the designed sensor should have an extremely low power consumption, in order to exploit the same power supply of the board.
To do this, ultra low power components to be placed on the sensor's board were chosen and the power and ground lines were included on the sensor's connector toward the iXem motherboard.

3.2 Low cost constraint

Low power constraint is not the unique specification which has to be met.
The production cost of the iXem board is around 40 USD, therefore all products which contribute to the sensing equipment should not overcome this price.
All sensors which are already included in the measurement system have an affordable cost, lower than the 40 dollars upper bound, except for the one that detects the water contant on the surface of the leafs: the leaf wetness sensor.
LWS are sold on the market at a rather high cost, since only a few companies in the world have produced this kind of device.
For seek of clarity are reported in table 3.1 the prices of most commercial leaf wetness sensor models on the market.

Manufacturer	Model	Sensor type	Price[USD]
Davis instruments	6420	Resistive	108.89
Deltaohm	HD 3901.5	Capacitive	143.00

Table 3.1: Table containing some of the most commercial LWS devices and their market price

As it can be seen from the above table, the field "Sensor type" refers to the technology adopted by the manufacturing companies for realizing the sensor.

3.3 Reliability constraint

The harder specification to meet was the one concerning the reliability of the designed sensor.
As it can be noticed after a further reading of the thesis dissertation, the candidate was put in front of a real challenge. The designed sensor should be capable of performing a measurement, within a reduced uncertainty range, of a device which can be modeled as an electrical capacitor, whose capacitance floats in the range of tens of pF in a dry condition, untill few nF when the surface is covered by water.

Another aspect that was analyzed by the candidate is the possibility to have a dual side measurement on leaf's surface.
Actually each commercial sensor, studied for seek of better result of the thesis work, exploits a double face configuration.
This is necessary since the sides of a leaf are subject to different environmental conditions.
For instance in a sunny day, the rear side of the sensor is the one which is less exposed to sun light, therefore it gets dry at a lower rate with respect to the illuminated face.
An analogous reasoning could be thought in case of a rainfall: the exposed side of the sensor gets wet immediately, while the back surface implies more time to reach the same condition.

In order to exploit this aspect a dual side configuration of the sensor was previewed, instead of a single side, this brought to a more comprhensive design, which was fidelly reproduced in the PCB creation.

In chapter 4 it is reported a detailed dissertation about two different technologies which are usually implied in leaf wetness sensors design.

Chapter 4

Leaf Wetness Sensor technology

The realization technology mainly divides between resistive technology and capacitive technology.
The difference stands, as the name says, in the physical principle exploited by the sensor: a resistive device acts as a variable resistor while a capacitive one acts as a variable capacitance.

4.1 Resistive sensors

A resistive sensor appears like a PCB where copper traces are placed in al ladder-like structure, this structure is fundamental for the working of the sensor, since this kind of sensor performs a resistive measurement.
In figure 4.1 is reported the resistive sensor designed and realized by Davis instruments.

Figure 4.1: Resistive sensor by Davis instruments

The presence of water among metal traces causes a reduction of the electric resitance of the sensor, according to the second Ohm's law.

$$R = \frac{1}{\rho}\frac{l}{A} \tag{4.1}$$

Where ρ is called the resistivity of the conductor used to physically realize the resistance and it is inversely proportional to the electric conductivity, l is the length of the resistor and A is the cross section of the conductor.
If a droplet falls between two biased adjacent traces, it creates a conductive path between the electrodes, reducing the overall resistance of the sensor, therefore a higher current will flow through the metal plates.
By measuring this current it is possible to evaluate the water content on the sensor's surface.
Never the less resistive sensors have an important drawback, which makes them unsuitable for the application in precision agriculture systems. When the sensor's surface is completely dry, the measured resistance approximately tends to infinite, since no conductive path between positive and negative terminals of the sensor in present. When the sensor gets wet, even a single droplet causes an immediate connection between the sensor's electrodes, leading to a 100 percent of measured water, as shown in figure 4.2

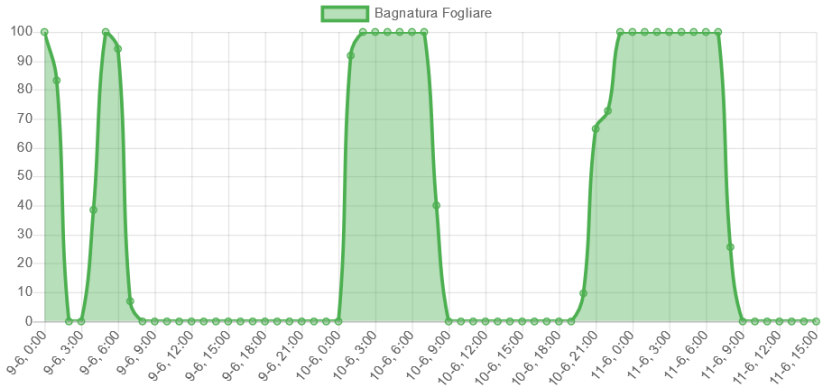


Figure 4.2: Leaf wetness measured by a resistive sensor versus time

Moreover, if a water drop is too small with respect to the inter electrode distance, such as dew droplets, which have a size much smaller than rain droplets, the presence of water is not sensed at all, since no conductive path between the electrodes is created.
The above cited issues make resistive sensor have huge reliability problems, therefore a better solution was implied for the seek of this thesis work.

4.2 Capacitive sensors

Capacitive sensors have a similar shape to the resistive ones, but they work in a completely different way: they measure the dielectric change of a material between two conductive electrodes, behaving like a variable parallel plate capacitor.
The strucutre considered in figure 4.7 represents two coplanar microstrip lines on FR4 substrate, particularly this structure is electrically equivalent to a variable capacitor.

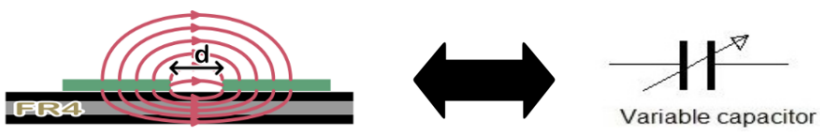


Figure 4.3: Coplanar traces' equivalent capacitance model

The application as a wetness sensor can be explained by considering that, in presence of different materials on the sensor' surface, the electric field between the metal electrodes propagates with different intensity, leading to different capacitance values.

Capacititve devices are rather complex systems, therefore a dedicated section to capacitor's physics is presented in the dissertation.
In section 4.3 a brief mathematical model of a parallel plate capacitor is reported, this would help the reader to better understand the physical behaviour of capacitive devices.

4.3 Parallel plate capacitor model

Beginning from a parallel plate structure is possible to evaluate the electric field localized between the capacitor arms.

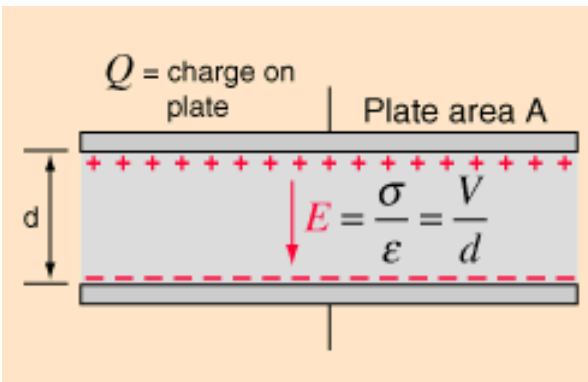


Figure 4.4: Parallel plate capacitor side view

The electric field in a dielectric medium is defined as the ratio between the density of charge per unit area of a metal plate and the electric permittivity of the dielectric.

$$E = \frac{\sigma}{\epsilon} \tag{4.2}$$

It is also known from the electrostatics theory that the Electric field between two parallel plates is computed as the ratio between the voltage applied accross the capacitor's leads and the distance between the two arms of the capacitor.

$$E = \frac{V}{d} \tag{4.3}$$

Combining the two relationships, taking into account that the charge density per unit area σ is equal to $\frac{Q}{A}$ and considering the definition of electrical capacitance $C = \frac{Q}{V}$, the electric capacitance stored between two parallel metal plates of area A, separated by a distance d, is given by the following formula.

$$C = \frac{\epsilon A}{d} \tag{4.4}$$

Where ϵ is the product by the dielectric constant of the void ϵ_0, which is equal to $8.854E - 12\frac{F}{m}$, and the relative permittivity of the material present between the capacitor arms.

4.4 Inter-digital parallel plate capacitors

Extending the concept of a couple of parallel plates to many parallel plates it can be modeled the behaviour of an iterdigital capacitor.

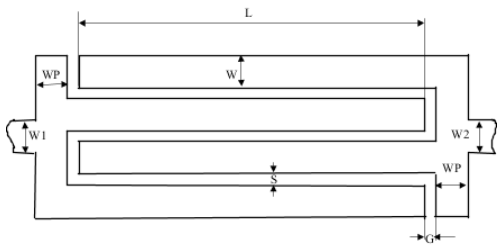


Figure 4.5: Front view of an interdigital structure.

Such structure is composed by various two terminals parallel plates capacitors, set up in a configuration that extends the overall capacitance.

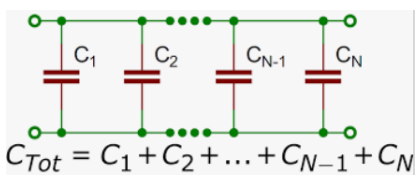


Figure 4.6: Front view of an interdigital structure.

As reported in figure 4.6, the total resulting capacitance is given by the parallel of all capacitive contributions, which corresponds to the sum the contributions of each single parallel plate capacitor.

An electric potential is applied to alternate metal traces, in such way adjacent traces are excited the one with respect to the other, making the electric field propagate through the dielectric present between them.

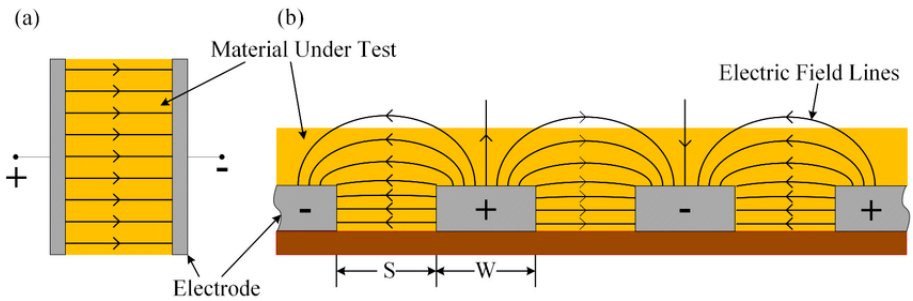


Figure 4.7: Transversal section of a PCB with interdigital pattern on it.

A variation of the dielectric above the traces brings to a different value of the sensor's capacitance, making the sensor capable of measuring surface covering changes. In this way a rather high measurement resolution is achieved.
In order to better understand the capability of LWSs, it is considered the following example. Considering the case of rain precipitation, for instance, since the rain water has a relative dielectric constant higher than the air, a higher capacitance will manifest. Measuring such capacitance it is therefore possible to evaluate the water content on the sensing surface.

4.5 Analysis of commercial capacitive leaf wetness sensors

Considering commercial LWS available on the marketplace, in figure 4.8 is presented the PHYTOS 31 capacitive sensor designed by Decagon, while in figure 4.9 is presented the HD3901 sensor by Delta Ohm, which was bought by the iXem Labs and provided to the candidate, who deeply studied and analyzed the provided sample.
Relying on a reference model, a more focused design was performed.

Figure 4.8: Decagon's capacitive LWS

Figure 4.9: Decagon's capacitive LWS

4.5.1 Interdigital pattern

A more detailed picture of the HD3901 is reported in figure 4.10.

As it can be noticed, on the sensor surface is present an interdigital pattern of

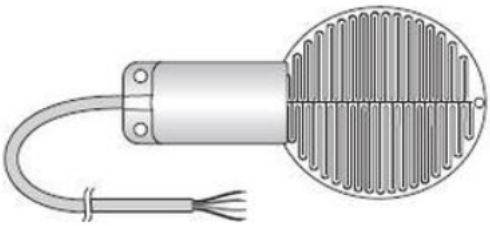


Figure 4.10: Transversal section of a PCB with interdigital pattern on it.

metal traces, eched on the substrate of a printed circuit board (PCB).
A remake of the PCB was accurately reproduced in the simulation step.

4.5.2 Hydrophobic coating

The white coating in figure 4.9 is made of an waterproof material that protects the metal plates from water corrosion. Usually as covering material is implied latex paint, which needs a specific treatment in order to properly work. After the treatment the latex paint has very low hygroscopic properties and it can be adopted to protect the sensor from water corrosion.

Moreover, the coating acts also as an insulator, avoiding ohmic contact between the electrodes beneath the covering. In measurement step it was understood that the coating layer is fundamental for the correct functioning of the sensor, since it avoids direct contact between the traces, which would bring to an extremely high value of the capacitance, which is totally out of the thesis purpose.
As it it will be noticed futherly, the insulating coating was realized with the PCB soder resist, which has the same function of the latex paint.

Part II

System design

The design part was organized resorting to "divide et impera" algorithm, that allowed to fix the fundamental steps required to perform a complete work.
A stepladder of the steps performed during the design part is reported below.

- INTERDIGITAL CAPACITOR SIMULATION
  Used tool: COMSOL Multiphysics

- MEASUREMENT SYSTEMS SIMULATION
  Used tool: Ltspice

- INTERDIGITAL PATTERN DESIGN
  Used tool: Eagle schematic editor

- MEASUREMENT SYSTEMS DESIGN
  Used tool: Eagle schematic editor

- PCB DESIGN
  Eagle PCB layout editor

Chapter 5

Interdigital pattern simulation

The simulative model was achieved by mean of COMSOL simulator, particularly, resorting to the ELECTROSTATICS AC/DC module, which allowed to perform an electrostatic analysis of the model. To achieve the correct simulation output, the simulator implies a solver which linearizes the differential problem given to it and provides the electric potential distribution between the capacitor's arms. By tuning global probe parameters in the simulation the model's electrical capacitance is also achieved as simulation output.

5.1 Preliminary model

Before proceeding with the interdigital capacitor simulation, it was necessary to verify the accuracy of the simulation tool, therefore, a known-value 1nF parallel plate capacitor was developed. In figure 5.1 it is reported the reference designed parallel plate model.

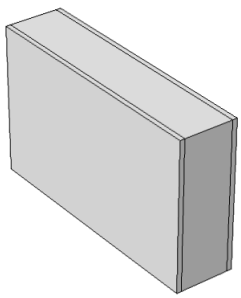


Figure 5.1: Model of designed parallel plate capacitor with fixed value of 1nF, used as reference to verify the simulation correctness

The physical dimensions and electric permittivity were properly chosen to achieve an approximate capacitance value of 1nF.
The electrical capacitance of the above model was computed first by hand, resorting to the formula which allows to compute the electric capacitance, knowing the electric permittivity coefficient of the insulating material in between the arms, the overlapping area and the spacing of the metal arms.

$$C = \frac{\epsilon A}{d} \tag{5.1}$$

The manual computation brought to a value of 9.99e-10 F.
As second step, the same capacitance was measured by mean of the electrostatic tool and it resulted to be 1.00E-9 F.
Considering the value of 1nF as the correct one, no appreciable error was introduced by the simulator.

As a further proof of correctness, the same capacitance was then measured on COMSOL by mean of a time constant simulation.
To do this the RC circuit presented in figure 5.2 was designed, then two electric terminals were assigned to the arms of the capacitor and a 1Mohm resistance was connected in series with it. A voltage step triggers the charging of the capacitor.

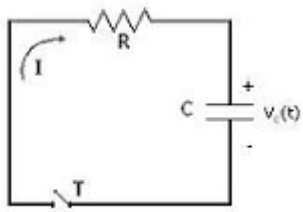


Figure 5.2: RC circuit used for time constant based simulation

After a time corresponding to the circuit time constant τ, the voltage across the capacitor will have reached the 63 percent of the steady state voltage, as it is known by RC circuits theory.
From the circuit's time constant the capacitance value was retrieved simply by

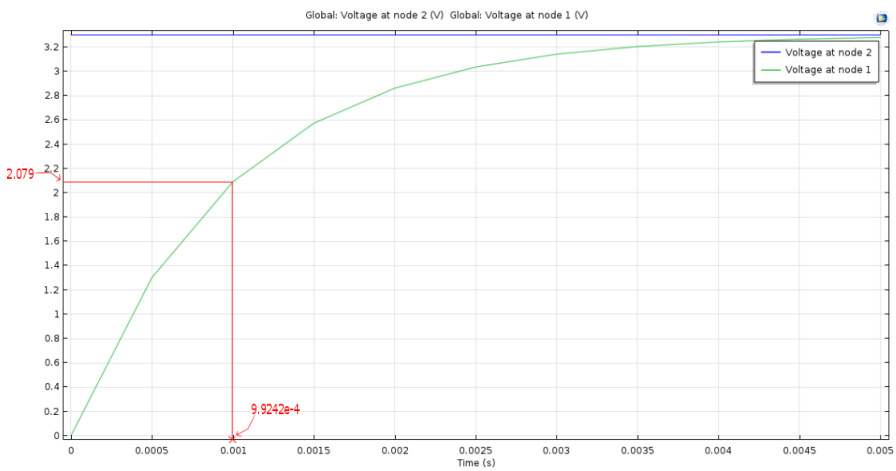


Figure 5.3: Charge curve of the reference capacitor when a 3.3V step is applied

computing the fraction $\frac{\tau}{R}$ The result of division was equal to 0.99nF, also this value is very similar to the ones produced by the other methods.

Considering the value of 1nF as the correct value, the time-based simulation reaches the correctness with an error of 0.1 percent.
As it can be noticed, the achieved capacitance values resulted to be impressively similar to each other, therefore the simulation tool was considered to work properly.

5.2 Interdigital model

After the correctness of the simulation tool was deeply verified, the actual interdigital electrodes model of the sensor was developed.

5.2.1 Geometry

Since the overall model resulted to be rather complex, a preliminary step was performed: before starting with the 3D design, a 2D plane geometry was realized. In figure 5.4 is presented the plane geometry designed by the 2D tool.

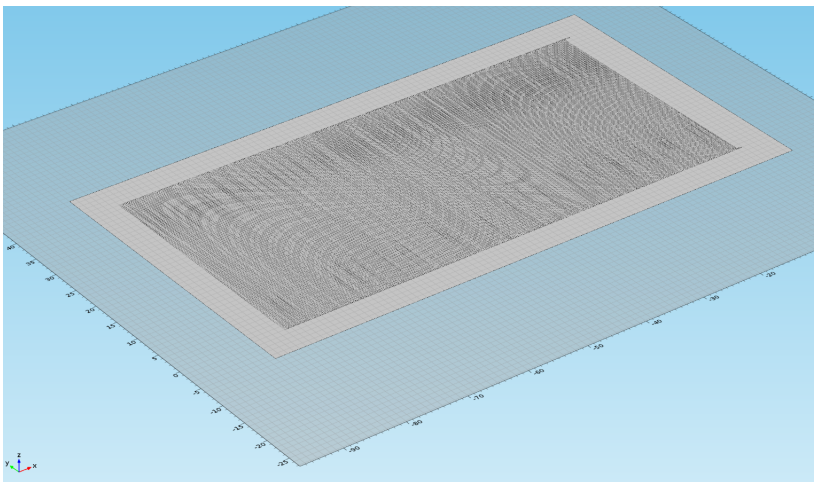


Figure 5.4: View of the designed plane geometry of intergdital pattern

The geometry was then imported into a 3D model to be extruded and make the actual simulative model take form.
The physical dimensions adopted for the PCB, which are reported in table 5.1 for sake of clarity, were therefore passed as parameters to the plane geometry.

Parameter name	Value[mm]	Description
W	80	pattern transversal length
L	40	metal arm length
w	0.2	trace width
s	0.2	trace spacing

Table 5.1: Table containing all parameters used for the plane geometry modeling

Then the 2D geometry was exported in two files, named POSITIVE.mphbin and GND.mphbin, which contained respectively the interdigital positive and ground terminal of the sensor. The generated files were then imported in the main simulation, to serve as 2D geometry to be extruded by mean of the "extrude" command.

In figure 5.5 is presented the 3D geometry designed by the 3D tool.

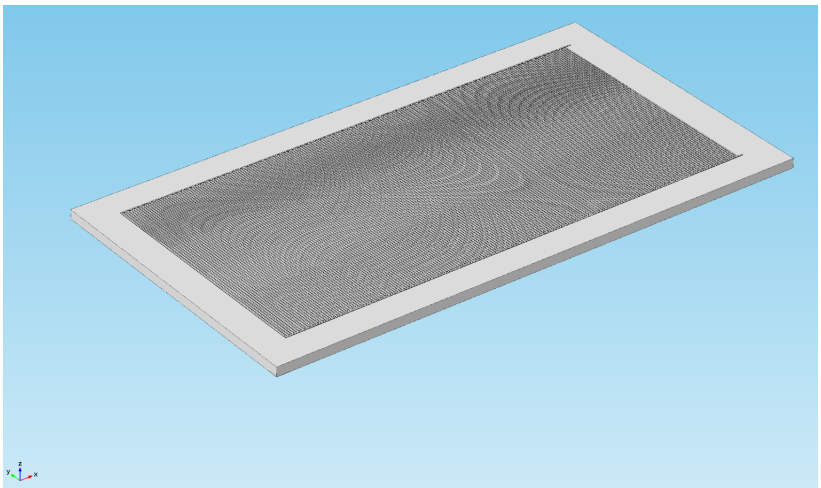


Figure 5.5: View of the designed 3D geometry of intergdital pattern

The extrusion parameters were passed to the 3D geometry by mean of the "parameters" field.
In table 5.2 are reported all parameters needed to set up the 3D simulation.

Parameter name	Value[mm]	Description
t	0.07	trace width
H	1.6	FR4 substrate height
h_{sold}	0.07	solder resist layer height
h_{cov}	0.1	covering material height

Table 5.2: Table containing all parameters used for the 3D geometry modeling

The extrusion of parts played a fundamental role about the complexity of the simulation, which translates in terms of computation complexity and needed hardware resources.
All simulation were carried out by mean of an elaborator present at the iXem Labs, which has the following hardware characteristics.

CPU: Intel Core i5 4670K, 3.4GHz, 4 Core

RAM: 12GB

After the paremeters insertion, hierarchical groups of geometric elements were created, in order to simply the material assignments in the simulation.
This step was performed through the "definitions" tab, in which many elements were added to different selections.
In figure 5.6 are reported the various definitions used to define the material domains of the model.

Figure 5.6: List of definition used in the simulation

At each selection was associated a set of domains or boundaries, as figures 5.7 to 5.10 show. More over the whole 3D model was inserted into a sphere which was assigned to air material, in order to make the simulation more realistic.

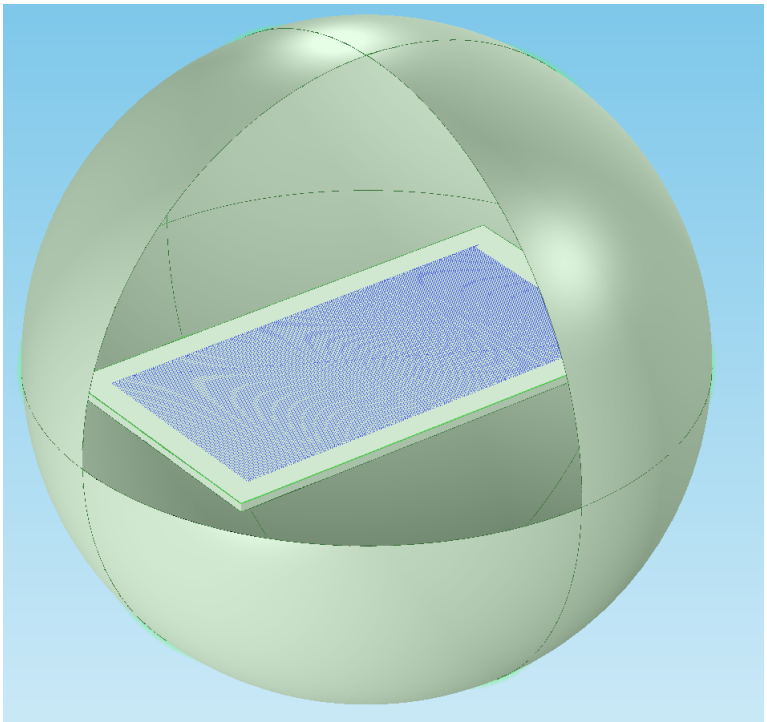


Figure 5.7: Selection including all domains

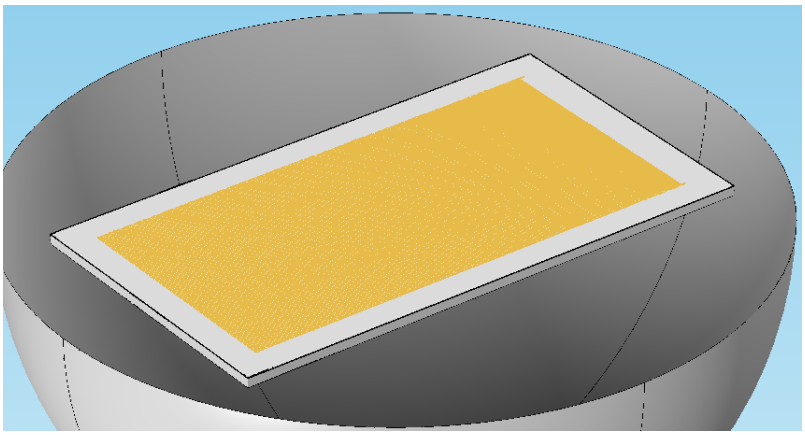


Figure 5.8: Selection including metallic boundaries

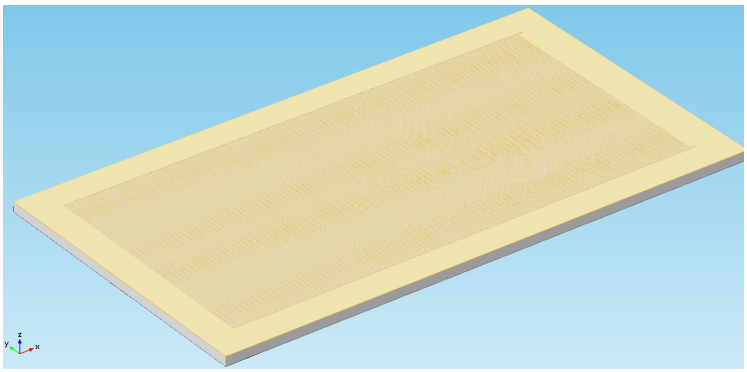


Figure 5.9: Selection including solder resist domain

5.2.2 Material Selection

After the geometry was designed, the candidate proceeded with the materials selection. The material choiche was performed in different ways, depending on the relevance of the material properties on the simulation result: air and water materials are quite standard, therefore they were available directly from Comsol's internal library.
Concerning FR-4 and solder resist materials instead, they depend strictly on the PCB manufacturer specifications.
Therefore they were set as generic materials but the dielectric properties fields were filled with the information provided by the PCB manufacturer.

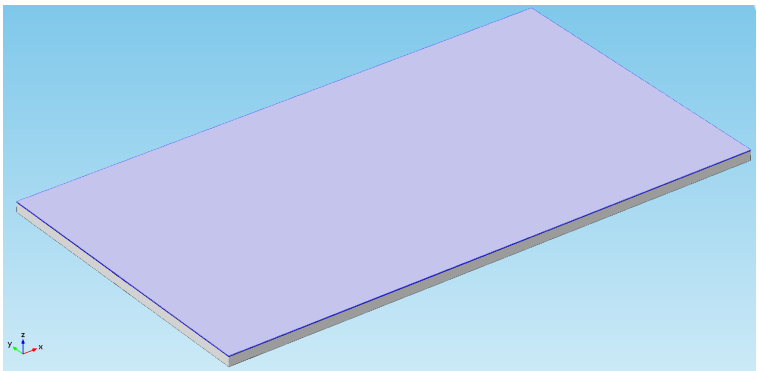


Figure 5.10: Selection including covering material domain

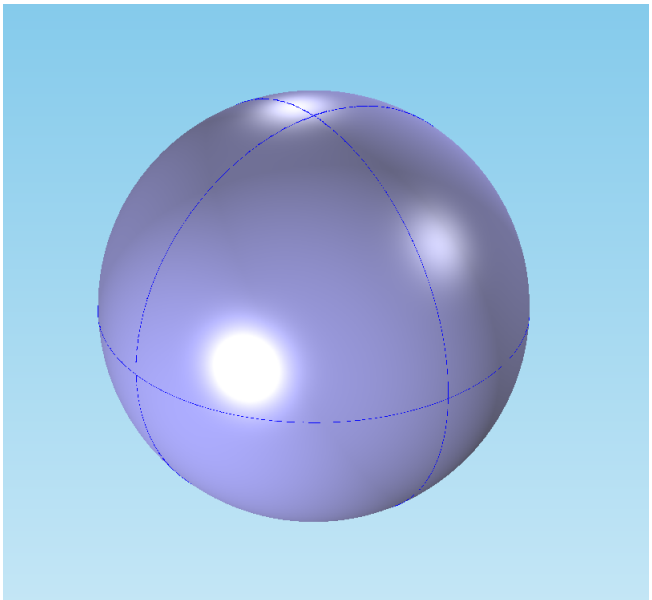


Figure 5.11: Selection including air sphere domain

In figure 5.12 is presented a sheet containing the properties of the FR-4 material implied for the manufacturing of the board.

The dielectric constant is directly proportional to the value of the capacitance, while the loss factor parameter models the dielectric losses due to the electric field propagating in the dielectric.

介电常数 Dielectric Constant	—	Etched/@1 MHZ IPC-TM-650 2.5.5.2	≤5.4 IPC-4101C 3.11.1.1	4.29
介质损耗 Loss Tangent	—	Etched/@1 MHZ IPC-TM-650 2.5.5.2	≤0.035 IPC-4101C 3.11.1.2	0.020

Figure 5.12: Image capture of PCB manufacturer data sheet for FR4 dielectric

The way to insert dielectric losses was taken by the Comsol'forum, whose link is provided below.
https://cn.comsol.com/forum/thread/92581/where-to-enter-dielectric-loss

Concerning the solder resist material, no information was provided by the PCB manufacturer, therefore the material properties were found in the datasheet of a high performance soldermask, which can be reasonably comparable to the one in analysis.
In figure 5.13 is presented a sheet containing the properties of the FR-4 material implied for the manufacturing of the board.

Electrical Properties

Electrical Properties			
Dielectric strength	IEC 60243-1		140 V/µm
Surface resistance	IEC 60167		8.7×10^{12} Ω
Volume resistivity	IEC 60093		8.2×10^{14} Ω/cm
Comparative Tracking Index (CTI)	IEC 60112		600 – 0.0 V [1)]
Dielectric constant ε_r at 1 MHz	IEC 60250		3.8-4.2
Dielectric loss factor tan δ at 50 Hz	IEC 60250	(77 °F)	25°C 1.5 ± 0.1
		(122 °F)	50°C 1.8 ± 0.2
		(167 °F)	75°C 2.0 ± 0.3
		(212 °F)	100°C 4.0 ± 0.4
		(248 °F)	120°C 5.5 ± 0.5

1) on CTI 400 laminate or with double coating

Figure 5.13: Image capture of the electric properties of PCB solder resist

The link to the datasheet is provided below:
https://www.holderstechnology.com/wp-content/uploads/2017/06/Probimer-77-72101_Hardener-77-79001_apac_e.pdf

Figure 5.14 shows the graphical interface for the choice of the materials in comsol multiphysics.

The material set was maintained constant except for the covering material, which could be either air or water, to have a more complete view a material sweeping was performed by the candidate, that provided the simulation results for both materials.

Figure 5.14: List of all materials used for the simulation

5.2.3 Mesh

Once the materials were set up the meshing was performed resorting to a manual meshing, in order to customize the element size depending on their position in the 3D model. In such way a more precise result was achieved and the simulation could be considered more accurate.
Meshing is important to divide the 3D model in sub pieces which the equations of the solver are applied to.
In figure 5.15 is presented the geomoery once the mesh was completed.

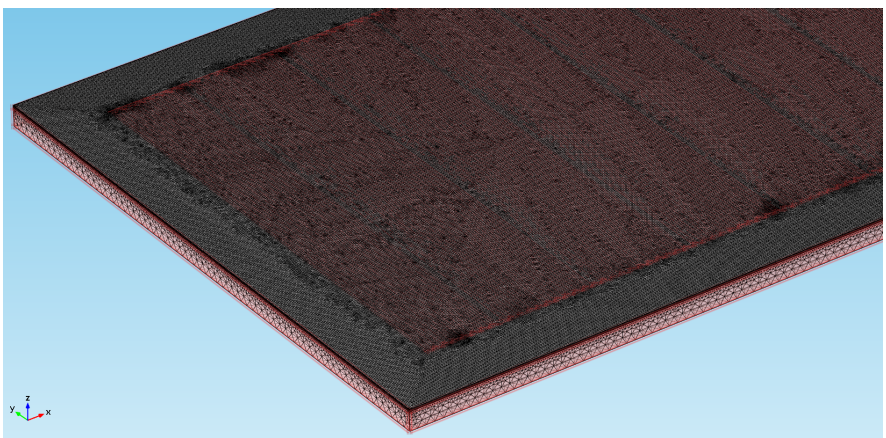


Figure 5.15: Zoomed view of the free tethrahedral meshing

After the meshing there are other two tabs that were authomatically compiled by mean of the model wizard at the start of the project.
So meshing was actually the last step of the simulation set up.
Afterwards the candidate could run the solver and wait for the result to be presented in the output table relative to the electric capacitance probe.

.

5.2.4 Solver run

After a long computation time the capacitance value was provided by the tool in the related probe table.
Moreover a "multislice" plot was provided on the "graphics" interface, containing the electric potential distribution for the designed component, as figure 5.16 shows.

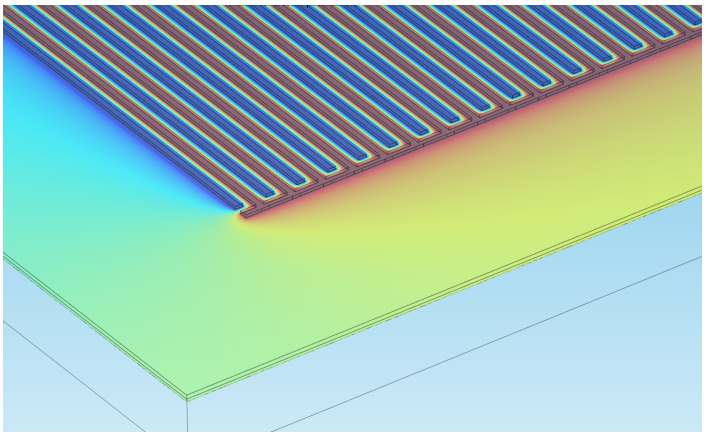


Figure 5.16: Zoomed view of the multislice potential

The red pattern has a positive potential while the blue one has a ground potential

Furthermore a plot of the electric field was obtained by simply requesting it to the program, through the "3D plot group" function, selecting the electric field voice.

As it can be noticed, the electric field propagates in the dielectric between the electrodes, particularly from the positive terminal to the negative one.

Along with the air covering the various wet conditions were therefore modeled and simulated properly, leading to a different capacitances, proportional to the water surface covering.
The various simulations brought the following results, which are summarized in table 5.3 for sake of clarity.

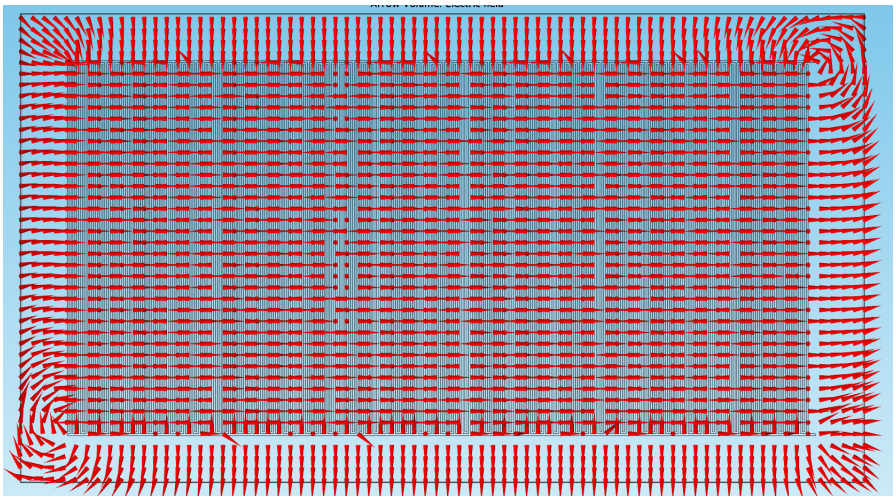


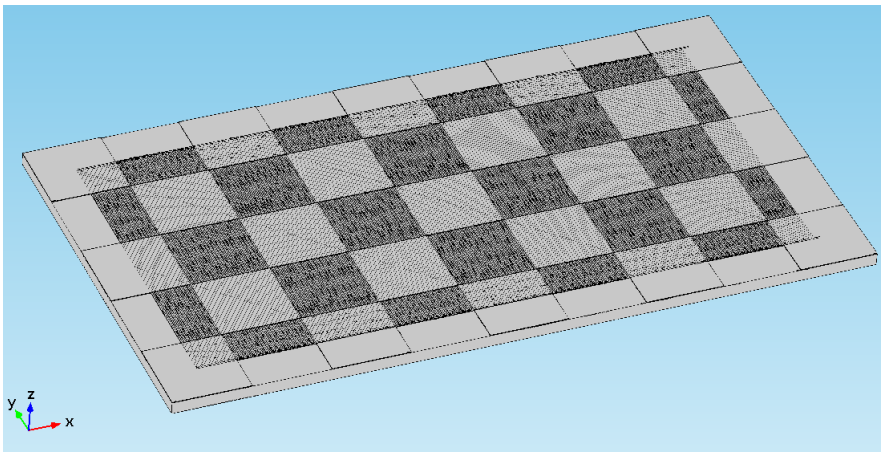
Figure 5.17: Front view of the electric field distribution between the electrodes

Water covering [%]	Capacitance value [F]
0	300 e-12
25	743e-12
50	1.32e-9
75	1.9e-9
100	2.33e-9

Table 5.3: Table containing COMSOL simulation results for different water covering percentages

A final step was performed, simulating a realistic situation: the sensor surface was covered by water at alternate regions forming a chess-like pattern, in order to model a water precipitation, then the capacitance value was retrieved by mean of the procedure already described.

The value provided by the simulation was C=1.3 nF which is, as expected, the same of 50 percent uniform covering case.
After the simulation step the candidate proceeded with the measurement systems design, which is described in chapter 6.


y
z
x

Chapter 6

Measurement systems simulation

The produced board was a prototypal version of the end product, so the retrievment of the measurand capacitance was deeply studied and analysed by the candidate; for this purpose various measurement systems, able to evaluate the same capacitance in different ways were simulated.

6.1 Measurement system overview

The very first method relies on a capacitance to digital (CDC) integrated circuit by Texas instruments, the fdc2112, which performs a frequency measurement and produces as output the measured capacitance on the I2C serial bus.
In figure 6.1 is reported the FDC2112 simplified block scheme. The measurand

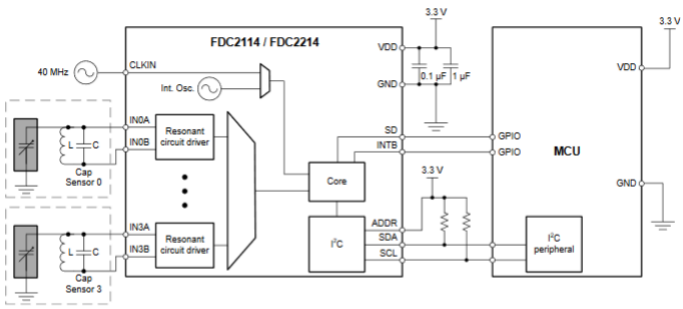


Figure 6.1: Simplified block diagram of the FDC2112 IC by Texas Instruments

capacitance is the greysquared one that is present at either of the two channels available on the FDC.

The second method relies on the LMC555 low-power timer integrated circuit, set up in a-stable multivibrator configuration, which generates an output signal whose frequency is proportional to the measured capacitance.
In figure 6.2 is reported the LMC555 integrated circuit in SOIC package.

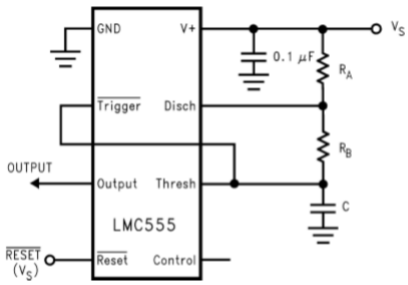


Figure 6.2: LMC555 application circuit for a-stable operation

The third way to measure a capacitance, as discussed also in the simulation section, is the time constant measurement: Basically the unknown capacitor is put in a low-pass filtering configuration and charged by mean of a time varying voltage stimulus (e.g step signal).
In figure 6.3 is presented a basic RC circuit, the capacitace charges until the switch is open, when it closes the capacitor gets deischarged.

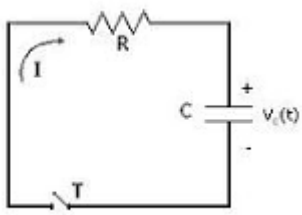


Figure 6.3: RC circuit used as model for time constant simulation

For the thesis purpose a voltage comparator was also implied in series to the RC circuit. The output of the RC circuit feeds the comparator, whose threshold is set to a value corresponding to the 63 percent of the supply voltage, this value

pinpoints the time constant of the circuit.

Design circuito RC

It can be noticed that for the second and third methods further processing will be needed in order to retrieve the value of the capacitance, while for the FDC method the capacitance value is directly provided by the integrated circuit on serial bus and can be immediately read by the microcontroller.

6.2 Details on measurement systems

In the following are presented the LTSPICE simulation models chosen for the implementation of the measurement systems.

6.2.1 Measurement system #1

The measurand capacitor is inserted in a resonant LC circuit, which is put in oscillation through the fdc internal drivers.
Then, the fdc performs a comparison between the oscillation frequency of the LC circuit, opportunely scaled through an internal prescaler, and a reference frequency, provided either by an external source or an internal one; Particularly, this last choice depends on the precision required for the measurement, for the purpose of LWS application, the internal 40MHz reference is sufficient to correctly perform tehe measurement. As told previously, the output of the fdc2212 is directly the measured capacitance.

No available spice model was found for the fdc family, therefore the simulation of this circuit could not be performed.

6.2.2 Measurement system #2

This second measurement system relies on the generation of a square waveform signal from a 555-timer in a-stable configuration. In figure 6.4 is reported the circuit scheme adopted in the simulation for the timer in a-stable configuration.

The values for Ra and Rb were properly chosen to provide a output signal frequency in the range 500 Hz : 5kHz, respectively for capacitance range (6n - 300p)F. Ra = 56kohm Rb = 470kohm The frequency of the generated signal is

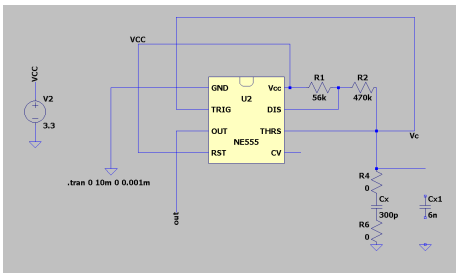


Figure 6.4: LMC555 for a-stable operation simulation circuit

proportional to the measured capacitance value, according with the formula taken from LMC555 datasheet.

$$C = \frac{1.44}{(R_a + 2R_b)f} \tag{6.1}$$

The measurement of the signal frequency is performed by the STM32 MCU itself, resorting to its high resolution internal timer. The reason of choice of this second measurement technique is in order to understand if the measurement achieved in this way is accurate enough to compete with the fdc2212. If the two measurement outputs were comparable, then a solution which implies only an external timer plus some internal components of the MCU, would have drastically reduced costs with respect its counterpart.
The electrical simulation was performed by mean of LTSPICE simulator. First the circuit was designed on the CAD-like interface, then the simulation parameters were chosen in order to produce a realistic output.

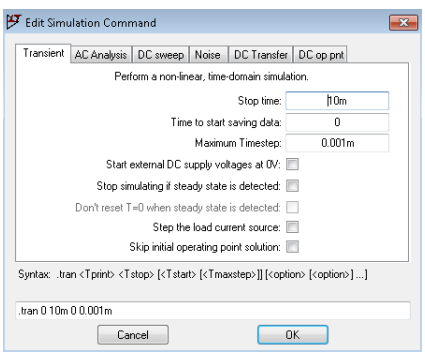


Figure 6.5: Simulation command window showing the simulation parameters

The circuit in figure 6.5 was designed in order to perform a swap of the resistances R4 and R6, which are simple 0 ohm resistances and can act as ideal jumpers. By mean of such trick it is possible to switch between the two capacitances, depending on which one is the target of the measurement.
In figures 6.6 and 6.7 are reported the simulation outputs for capacitance value of 300pF and 6nF respectively.

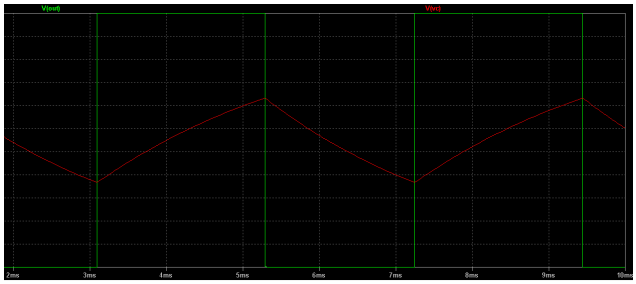


Figure 6.6: Simulation output for a capacitance of 300pF, corresponding to a dry condition

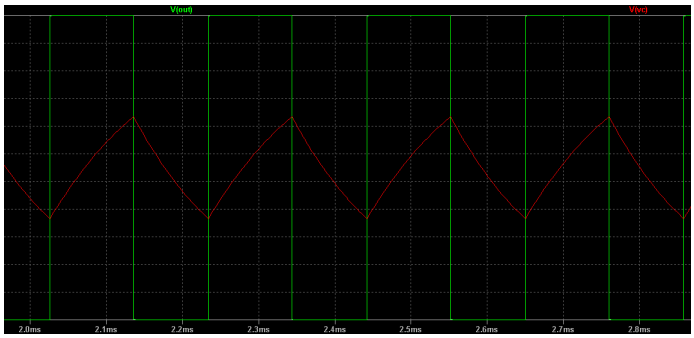


Figure 6.7: Simulation output for a capacitance of 6nF, corresponding to a wet condition

The green signal is the square waveform in output from the timer, while the red one tracks the voltage across the capacitor.
As it can be noticed from the circuit, the a-stable configuration, achieved linking the threshold and the trigger pin of the LMC555, makes the capacitor to charge until the upper threshold is reached, then discharge until the lower limit is overcome.

6.2.3 Measurement system #3

The third implemented measurement system exploits the basic circuit of passive filter theory, the RC-circuit. This circuit is supplied by a time varying stimulus whose rising edge starts to charge the measurand capacitor. The charging curve is expressed by

$$V(t) = V_0 + V_\infty[1 - e^{\frac{t}{\tau}}] \tag{6.2}$$

Where V_0 is the starting voltage of the input signal, V_∞ is the steady state voltage and τ is the time constant of the circuit RC.

Since it is assumed that the circuit is fed by a linear step, the variation of voltage with time can be considered as a constant, therefore the measurand capacitor is charged by a constant current, until it reaches its steady state value, which is equal to the supply voltage. Once the capacitor is fully charged, the step is removed and a constant current discharges the capacitor.
The time implied to get the capacitor discharged is proportional to the target capacitance.

The circuit was designed taking into account that when the step generated by the microcontroller reaches its end, the microcontroller's pin that provides the step is left floating and reaches a high impedance state.
Considering this, it was necessary to provide a discharging path toward ground, in order to make the capacitor discharge.
This condition was obtained by adding a resistor tied to ground in parallel to the capacitor.
In this way a charge path, highlighted in red, and a discharging path,highlited in green, are achieved, as shown in figure 6.8.

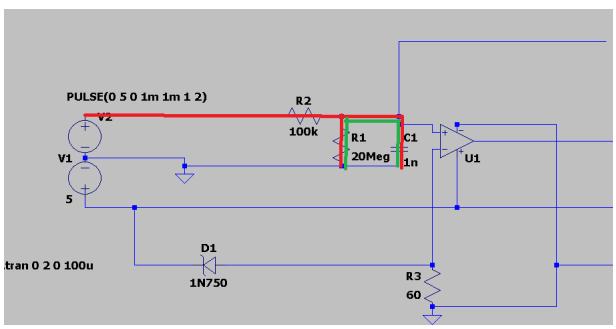


Figure 6.8: RC circuit charge and discharge paths

The voltage pulse is generated by the STM32 internal timer and provided to

the RC circuit through microcontroller's GPIO port. The comparator's threshold voltage is obtained through a Zener regulator. Modifying the value of resistor R4 it is possible to pinpoint the desired threshold voltage.
The op-amp in voltage follower topology models the output pin of the microcontroller, since it decouples the RC section from the step generator. Thanks to the path to ground introduced by the resistance R1, the capacitor manages to discharge, otherwise the capacitor wuold not discharge properly.

6.2.4 Circuit explaination

When the step is generated, the STM32 internal timer is reset and it starts to count in free-running mode. As soon as the voltage across the capacitor overcomes the threshold of the zener regultor, the comparator digital output switches, providing an output signal which acts as an interrupt for the microcontroller timer, which in turn will stop the free running count, giving a precise value of the discharge time, from witch it can be retrieved the capacitance.

In figure 6.9 is reported the simulation output, obtained for a capacitance value of 6nF.
In figure 6.10 instead is presented the simulated discharge curve for a target

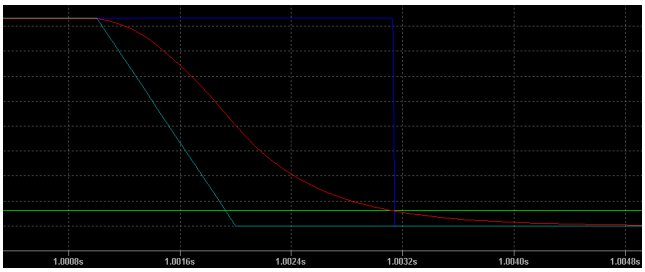


Figure 6.9: RC circuit simulation for 6nF capacitor

capacitance of 300pF.
As it can be noticed from the charge curve, the voltage accross the capacitor never reaches the supply voltage since there is a voltage partition between the step input and the capacitor voltage.
For this reason the RC model was considered unreliable for the measurement and therefore the other solutions were preferred.
A possible soltuion to this issue is to program the microcontroler pin to end the step in low state , instead of high impedance state.
Another solution is to decouple the output of the microcontroller by mean of a

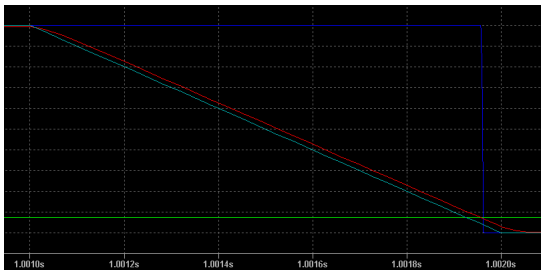


Figure 6.10: RC circuit simulation for 300pF capacitor

pulse driven mosfet, as figurre 6.11 shows.

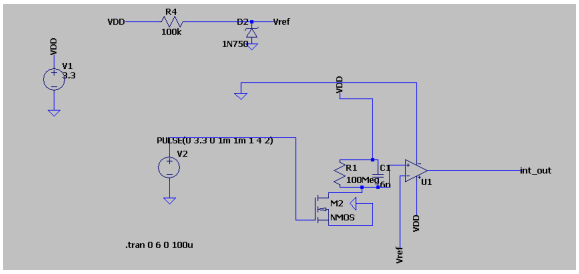


Figure 6.11: RC circuit with input decoupled from microcontroller output pin

Altought the result obtained is better than the previous case, the issue of voltage partition in this configuration is still present, since the R_{DSON} of the n-mosfet M2 is not negligible.

Making all consideration about the best measurement circuit to imply, it was chosen the one with the capacitance to digital converter IC by Texas instruments, which in results step provided the more accurate results.

Chapter 7

Schematic design

The interdigital pattern strategy was adopted after a deep documentation on scientific paper which discuss the interdigital sensor topologies.
According with artcle **??**, the chosen topology should allow the designer to achieve a rather high capacitance value, maintaining good stability and reducing power consumption.
Moreover, the candidate took inspiration from the Delta ohm's HD3901 LWS to design his own sensor.
So the chosen topology of the pattern was decided to have two electrodes with alternated fingers, which are excited by the applied voltage in order to make the electric field to propagate between them.
The designed pattern was drawn following the same specifications adopted for the COMSOL 3D model designed in the simulation step.
In this way a the reference model remains the same and a more focused design could be performed.
In the schematic editor, the interdigital capacitance doesn't have a specific symbol, therefore a connector was used to model it, as reported in figure 7.1.

All simulated measurement systems were drawn by mean of schematic editor of Autodesk Eagle.
First of all the two measurand capacitances network were created.
As it was previously told in the thesis summary, the interdigital capacitors were designed to be arbitrairly coupled or decoupled via the 0 ohm resistances whose footprint was predisponed on the PCB.
In oder to clarify this concept are reported in figure 7.1 the designed capacitors.

As it can be noticed, the capacitors' symbols are not the usual ones, in fact an interdigital pattern is equivalent to a capacitor, but obviously doesn't have the same footprint, since there is no manufacturer that has produced it.

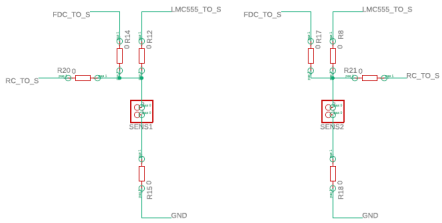


Figure 7.1: Interdigital capacitor elements in the schematic editor

The measurement systems instead were designed precisely importing the CAD model from the manufacturers site, following the already designed circuit schemes achieved in the simulation step.
The various measurement systems are presented in figure 7.2 to 7.4.

Concerning the components implied, the bill of materials of the schematic is

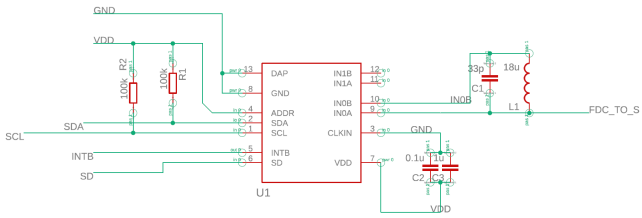


Figure 7.2: Measurement circuit implying the FDC2112 chip

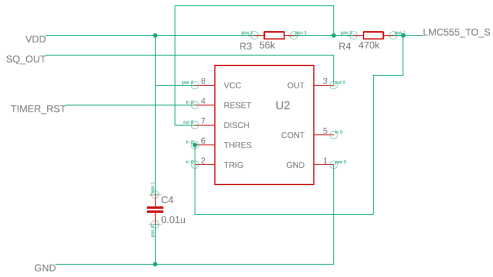


Figure 7.3: Measurement circuit implying the LMC555 timer

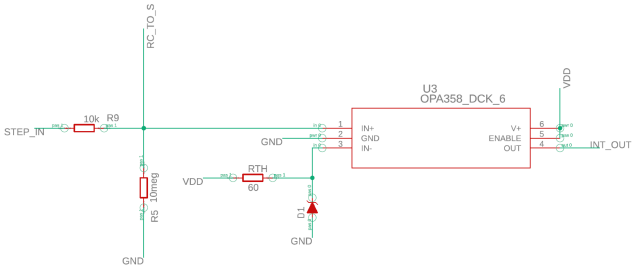


Figure 7.4: Measurement circuit implying RC topology

presented below.

Part	Value	Device	Package	Description
C1	33p	CC0603	C0603	CAPACITOR, European symbol
C2	0.1u	CC0603	C0603	CAPACITOR, European symbol
C3	1u	CC0603	C0603	CAPACITOR, European symbol
C4	0.01u	CC0603	C0603	CAPACITOR, European symbol
D1	3V	DIODE-ZENER-BZT52C3V6S	SOD-323	Zener Diode
JP1		PINHD-1X10	1X10	PIN HEADER
L1	18u	INDUCTOR	L0603	Inductors
R1	100k	RR0603	R0603	RESISTOR, European symbol
R2	100k	RR0603	R0603	RESISTOR, European symbol
R3	56k	RR0603	R0603	RESISTOR, European symbol
R4	470k	RR0603	R0603	RESISTOR, European symbol
R5	10meg	RR0603	R0603	RESISTOR, European symbol
R8	0	RR0603	R0603	RESISTOR, European symbol
R9	10k	RR0603	R0603	RESISTOR, European symbol
R12	0	RR0603	R0603	RESISTOR, European symbol
R14	0	RR0603	R0603	RESISTOR, European symbol
R15	0	RR0603	R0603	RESISTOR, European symbol
R17	0	RR0603	R0603	RESISTOR, European symbol
R18	0	RR0603	R0603	RESISTOR, European symbol
R20	0	RR0603	R0603	RESISTOR, European symbol
R21	0	RR0603	R0603	RESISTOR, European symbol
RTH	60	RR0603	R0603	RESISTOR, European symbol
SENS1		PINHD-1X2	1X02	PIN HEADER
SENS2		PINHD-1X2	1X02	PIN HEADER
U1	Value	FDC2112DNTR	DNT0012B	
U2	Value	LMC555IPW/NOPB	D0008A_N	
U3	OPA358_DCK_6	OPA358_DCK_6	DCK6	

Figure 7.5: Part list of the PCB

After all parts were placed on the schematic editor, the candidate proceeded with the implementation of the PCB layout, by mean of Eagle's PCB editor.

Chapter 8

Printed circuit board design

The PCB design was performed making different considerations about the cost of a real implementation of an IDC in printed circuit board technology.
First of all were considered the technological parameters that were allowed by the PCB manufacturer, in order to have a low cost solution.
In figure 8.1 are reported all the technological choices for the customization of the PCB.
In the rows following the instant quote picture, ethe major characteristic analyzed analyzed from a cost-reliability point of view.

Product Detail

Product No. :	W40986ASS42	**Gerber File :**	LWS_2019-01-16.zip		
Board type :	Single PCB	**Panel Way :**			
Size :	137.5 x 53 mm	**Quantity :**	10	**Layers :**	2 Layers
Material :	FR-4 TG130	**Thickness :**	1.6 mm	**Min Track/Spacing :**	6/6mil
Min Hole Size :	0.3	**Solder Mask :**	Green	**Silkscreen :**	White
Gold fingers :	No	**Surface Finish :**	Immersion gold	**Via Process :**	Tenting vias
Finished Copper :	2 oz Cu	**Additional Options :**			
Create Time :	2019/1/16 20:49:51	**Build Time :**	3-4 days	**Estimated Finish Time :**	2019-01-20 China Time Zone(GMT+8)

Figure 8.1: PCB product characteristics

- **Layers:** The total number of layers was decided at design step, fundamentally to try to maximally reduce the production cost.
  Unfortunately, as it was evidenced by the laboratory measurements, the capacitance present on the top side and the one on the bottom side interfere with each other, leading to a strict correlation of the two capacitance values. Therefore in the aftermath it was realized that in order to increase the reliability of the sensor a quad layer structure could fit better this constraint.

- **Material**: Is the dielectric chosen for the substrate of the PCB, it is characterized by a dielectric constant of 4.29 and a loss factor equal to 0.02
  These parameters were directly taken by the datasheet provided by the manufacturer and placed into the simulation parameters' table, in order to achieve a more reliable result.
  The number 130 in the product name refers to the heat temperature in celsius degrees that the material can sustain without getting damaged.
  For the purpose of the thesis application, since the environmental temperature never reaches high temperature, the temperature coefficient was not considered for the design.

- **Min track/spacing** With this parameter is intended the traces width and spacing allowed by the manufacturer, in fact if a reduced width would be required, a much precise technology must be implied, resulting in a doubled price of the board.
  More over the elaborator used to perform the simulations, did not allow to furtherly reduce the track width below the 6mils, since it ran out of memory.

- **Finished Copper** The precision of the simulation tool, did not allow to reduce the domain dimensions below 70 μm, therefore 2oz of copper were simulated, providing a satisfying result.

First of all the mechanical drawing was done, the capacitive patter was designed referring to the COMSOL model, while the electronics were placed on the area beside the pattern.
Therefore the whole PCB occupied an area of 137 x 53 mm^2, in order to make place fot the measurement circuitry, which includes, as previously explained, an LMC555 timer, an FDC2112 IC, and an OPA380 3.3V supply operational amplifier, plus some passive components such as resistors, inductors and capacitors.
In the following picture, are reported the various parts placed on the top layer, then the bottom layer will be examined.

8.1 Top layer

Following the simulated model, the top bottom IDC was realized with 8 mils wide metal traces, spaced by 8 mils distance.

The 100 fingers arrays were created resorting to the "pattern" command in Eagle. For the supply traces a wider trace dimension of 16 mils was chosen, since supply lines usually carry much more current with respect to signal lines.

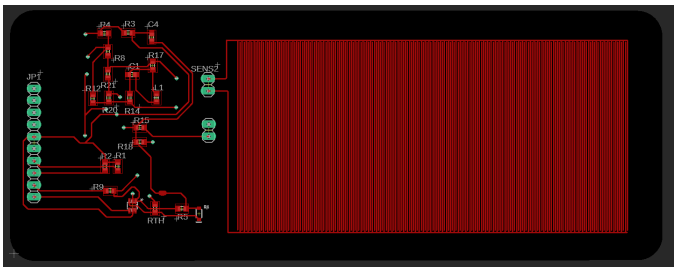


Figure 8.2: Top layer view of the PCB

8.2 Bottom layer

For the bottom layer a sparser pattern with electrodes spaced by 16 mils was created.
According to the interdigital capacitance relationship in 8.1, the capacitance value modifies by a factor four with respect to the pattern on the top layer.

$$C \sim \frac{(N-1)\epsilon A}{d} \tag{8.1}$$

Where N is the total number of fingers, A is the area of the lateral sturface of the metal traces and d is the trace spacing. As it can be noticed, the value of the capacitance is proportional to the number of theet and to the track thickness, while it is inversely proportional to the track spacing.

The choice to implement different patterns on each side comes from the need to try different pattern configurations, in order to have a more complete view of the possible patterns and selecting which one is the best for the thesis purpose.

8.3 PCB finishing

After the PCB was designed the gerber and drill files were exported by the tool and sent to the manufacturer to make the board.
The components were bought on Mouser and mounted manually.

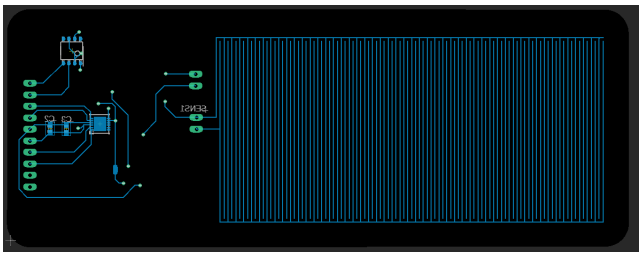


Figure 8.3: Bottom layer view of the PCB

In figures 8.4 to 8.6 there is the list of the components bought on the seller site.

Product Detail	Customer No	Order Qty.	Price (EUR)	Ext. (EUR)	Status	Date	Invoice No.
Mouser No: 595-OPA358AIDCKR Mfr. No: OPA358AIDCKR Desc.: High Speed Operational Amplifiers High Speed Operational Amplifiers 3V Single Supply 80MHz High-Speed		8	1,14 €	9,12 €	8 Shipped	24-Jan-19	51149238
Mouser No: 595-LMC555IMX/NOPB Mfr. No: LMC555IMX/NOPB Desc.: Timers & Support Products Timers & Support Products CMOS Timer		8	1,32 €	10,56 €	8 Shipped	24-Jan-19	51149238
Mouser No: 595-FDC2112DNTT Mfr. No: FDC2112DNTT Desc.: Proximity Sensors Proximity Sensors Noise-immune Capacitive Sensing Solution for Proximity Sensing 12-WSON -40 to 125		8	3,48 €	27,84 €	8 Shipped	24-Jan-19	51149238
Mouser No: 810-MLF1608C180KTA00 Mfr. No: MLF1608C180KTA00 Desc.: Fixed Inductors Fixed Inductors 18 UH 10%		8	0,166 €	1,33 €	8 Shipped	24-Jan-19	51149238
Mouser No: 81-GCM0335C1E330JA6D Mfr. No: GCM0335C1E330JA16D Desc.: Multilayer Ceramic Capacitors MLCC - SMD/SMT Multilayer Ceramic Capacitors MLCC - SMD/SMT		15	0,035 €	0,53 €	15 Shipped	24-Jan-19	51149238
Mouser No: 603-AC0603FR-0756KL Mfr. No: AC0603FR-0756KL Desc.: Thick Film Resistors - SMD Thick Film Resistors - SMD 1/10W 56K ohm 1% AEC-Q200		15	0,019 €	0,29 €	15 Shipped	24-Jan-19	51149238

Figure 8.4: part 1 of the list of bought components

Mouser No: 603-RC0603FR-070RL Mfr. No: RC0603FR-070RL Desc.: Thick Film Resistors - SMD Thick Film Resistors - SMD 0.0ohm 1%		30	0,013 €	0,39 €	30 Shipped	24-Jan-19	51149238
Mouser No: 603-AC0603FR-13100RL Mfr. No: AC0603FR-13100RL Desc.: Thick Film Resistors - SMD Thick Film Resistors - SMD 100 ohm 1% 1/10W AEC-Q200		10	0,019 €	0,19 €	10 Shipped	24-Jan-19	51149238
Mouser No: 603-AC0603FR-0768RL Mfr. No: AC0603FR-0768RL Desc.: Thick Film Resistors - SMD Thick Film Resistors - SMD 1/10W 68ohm 1% AEC-Q200		10	0,019 €	0,19 €	10 Shipped	24-Jan-19	51149238
Mouser No: 833-BZT52C3V0S-TP Mfr. No: BZT52C3V0S-TP		10	0,17 €	1,70 €	10 Shipped	24-Jan-19	51149238
Desc.: Zener Diodes Zener Diodes 200mW 3V							
Mouser No: 71-CRCW060356R0FKEB Mfr. No: CRCW060356R0FKEB Desc.: Thick Film Resistors - SMD Thick Film Resistors - SMD 1/10watt 56ohms 1%		10	0,011 €	0,11 €	10 Shipped	24-Jan-19	51149238
Mouser No: 771-PDZ27B135 Mfr. No: PDZ2.7B,135 Desc.: Zener Diodes Zener Diodes DIODE ZENER 2 PCT		2	0,175 €	0,35 €	2 Shipped	24-Jan-19	51149238
Mouser No: 771-BZX84J-C3V0115 Mfr. No: BZX84J-C3V0,115 Desc.: Zener Diodes Zener Diodes DIODE ZENER 5 PCT		2	0,314 €	0,63 €	2 Shipped	24-Jan-19	51149238

Figure 8.5: part 2 of the list of bought components

Mouser No: Mfr. No: Desc.:	771-BZX84J-B2V7,115 BZX84J-B2V7,115 Zener Diodes Zener Diodes Diode Zener Single 2.7V 2% 550mW 2-Pin		2	0,323 €	0,65 €	2 Shipped	24-Jan-19	51149238
Mouser No: Mfr. No: Desc.:	71-CRCW0603306JT CRCW060330M0JPTAHR Thick Film Resistors - SMD Thick Film Resistors - SMD 1/10watt 30Mohms 5%		5	0,524 €	2,62 €	5 Shipped	24-Jan-19	51149238
Mouser No: Mfr. No: Desc.:	71-CRCW0603J-100M CRCW0603100MJPTAHR Thick Film Resistors - SMD Thick Film Resistors - SMD 1/10watt 100Mohms 5%		7	0,498 €	3,49 €	7 Shipped	24-Jan-19	51149238
Mouser No: Mfr. No: Desc.:	603-RC0603FR-0710ML RC0603FR-0710ML Thick Film Resistors - SMD Thick Film Resistors - SMD 10M OHM 1%		10	0,016 €	0,16 €	10 Shipped	24-Jan-19	51149238

Figure 8.6: part 3 of the list of bought components

The overall cost for ten boards, comprehensive of the electronic components to be mounted on is of 68 USD for the PCBs and 60.39 for electronics, resulting in 128.39 USD total.

Part III

Laboratory practice

After the design part it came the more practical laboratory part, in which the candidate could perform the manual assembly of the PCB, the fixing of the PCBs and the laboratory measurements.
It is presented in table8.1 the list of laboratory instrumentation implied for the more practical part of the thesis work.

Producer	Instrument type	Serial number
Essemtech	Manual pick and place machine	203719
Atten	Signal generator	308302
Tektronix	Digital signal oscilloscope	203612

Table 8.1: Table containing all used instrumentation in the laboratory part

More over a soldering station with a microscope and a programmable heater were implied for manual soldering and boards baking.

Figure 8.7

Figure 8.8

Chapter 9

PCB troubleshooting

Once the board was produced, the components were ordered and manually soldered on the PCB.
In order to perform this task, the instrumentation available in electronics laboratory beside the iXem Labs was implied.
After the placing of the components, an hard bake process allowed to fix the microball tin on the copper places.
At mounting time, the first project mistake was individuated.
The implied Zener diode was designed to work as a voltage reference of 300mV but among the Zeners available on the marketplace it was very difficult to find one below the 1V breakdown voltage, there fore a circuit topology like the one in figure 9.1 was adopted, implying a 3V diode.

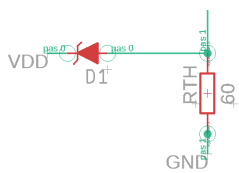


Figure 9.1: $3V_{br}$ diode implied for a 300mV reference

Other tries were performed mounting different break down voltage diodes, but in order to index a completed discharge it is necessary a rather high brekdown voltage, as close as possible to the supply voltage.
However the candidate should have provided more care to this aspect, since in order to make the cirucuit properly working, the threshold resitance R_{th} and the

Zener diode ought to be swapped, as shown in figure 9.1.

The second mistake committed was that, since many by pass 0 ohm resistors were implied, the routing tool did not consider the nets with the by pass resistances belonging to the same net, therefore the input pins of the FDC2112 were not properly connected to the measurand capacitance.
The candidate tried to repair the issue by hand but the WSON package complexity did not allow a successful fixing of the problem.
Therefore in order to provide a measurement by mean of the FDC2112 the ready

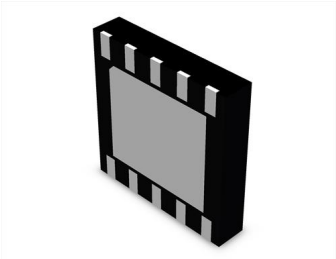


Figure 9.2: WSON package bottom view

made evaluation module by Texas instruments in figure 9.3 was implied, allowing the candidate to correctly perform the measurements.
Afterward the board was tested, the results were compared with the one achieved

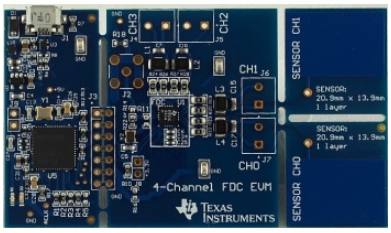


Figure 9.3: Top view of the FDC2112-EVM board

in the simuulation step.
All measurements outputs of the interdigital sensor are reported in chapter 10.

The final issue, that could hardly be predicted in simulation step, is that the two metallic patterns of the sensor overlap for a certain area and have a dielectric in between, which is the FR4 of the subtrate. This causes a strong correlation

between the value measured on each face, since one measurements overlaps to the other, making the result extremely confusive.
The solution which was evidenced is to produce the sensor on a quad layer PCB, in this way thanks to the intermediate ground planes each pattern is minimally influenced by the opposite one.

Since in the two patterns only one has the solder resist on it, the water content can be measured only on it, therefore the other pattern was not considered in the measurement.
The initial idea was in fact to avoid the presence of the solder resist on one side of the sensor, in order to analyze also the contribution of the resist covering.
The result was surprisingly determined by the fact that in case of no insulator present on the top of the sensor, the metallic plates of the sensor are put directly in contact by mean of the water droplets.
However this behaviour implements a resistive sensor, which is out of the project specifications, as reported in part I.

Chapter 10

Results

The measurement step was performed carefully, trying to maintain as much as possible the traceability of the measurements.
For this reason the temperature was verified to be as constant as possible and the air humidity was under control as well.
The measurements analyzed different leaf wetness configurations, the same described during the simulation step, which are water covering from 0 percent till 100 percent, with step 25 percent.
For the measurements were implied the available AC to DC Power supply unit, the Atten signal generator and the Tektronix digital oscilloscope.
First the dry condition were measured, then water was deposed on sensor's surface and the new capacitances were measured.

10.1 LMC555 measurments

The candidate started to measure the output frquency of the LMC555 timer with the oscilloscope, providing a 3.3V unipolar supply voltage.

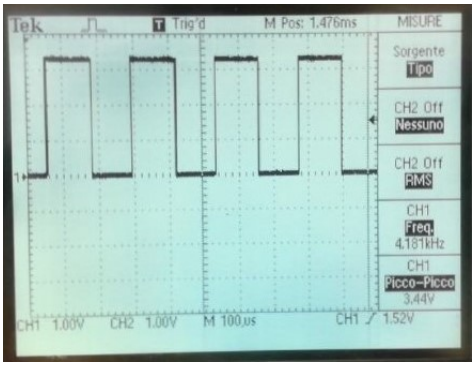


Figure 10.1: Oscilloscope view for the LMC of the case with 0% of water

After the first measurement was performed, the other cases of increased leaf humidity were realized by submerging for two minutes some absorbing paper stripes, which model covering percentages.
The paper sheets were retailed meauring with a caliper the dimensions of the intergital pattern of the sensor.
The dimension of the pattern in analysis resulted to be 9.4x5.6 cm.
The frequency measurements of different leaf wetness conditions are reported in figures 10.2 to 10.9.

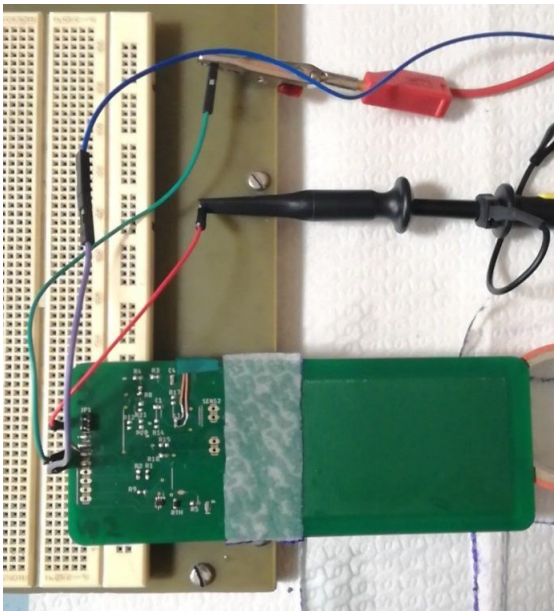


Figure 10.2: Frequency measurement for 25% water covering

For sake of clarity a table with all LMC555 measurements is reported in 10.1

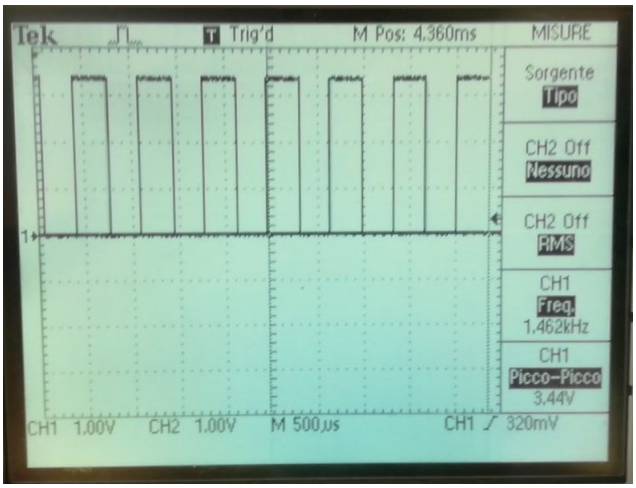


Figure 10.3: Oscilloscope view for the LMC of the case with 25% of water

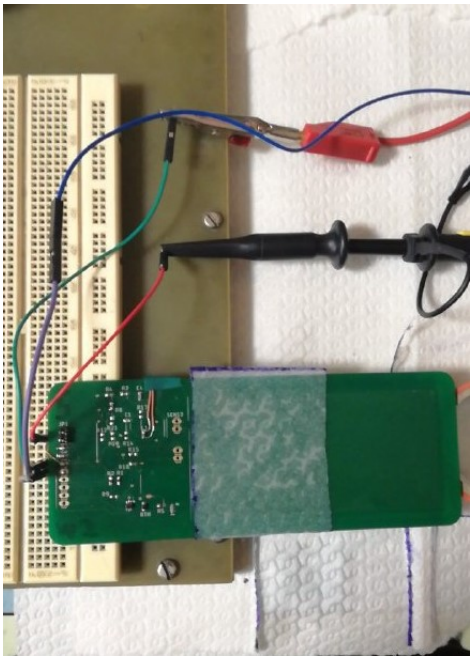


Figure 10.4: Frequency measurement for 50% water covering

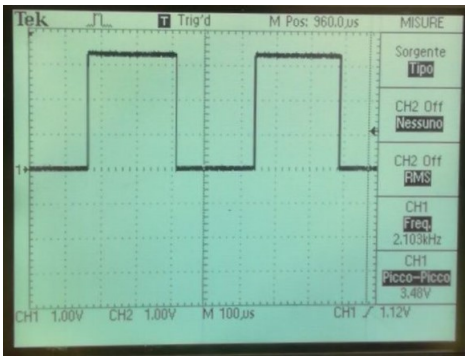


Figure 10.5: Oscilloscope view for the LMC of the case with 50% of water

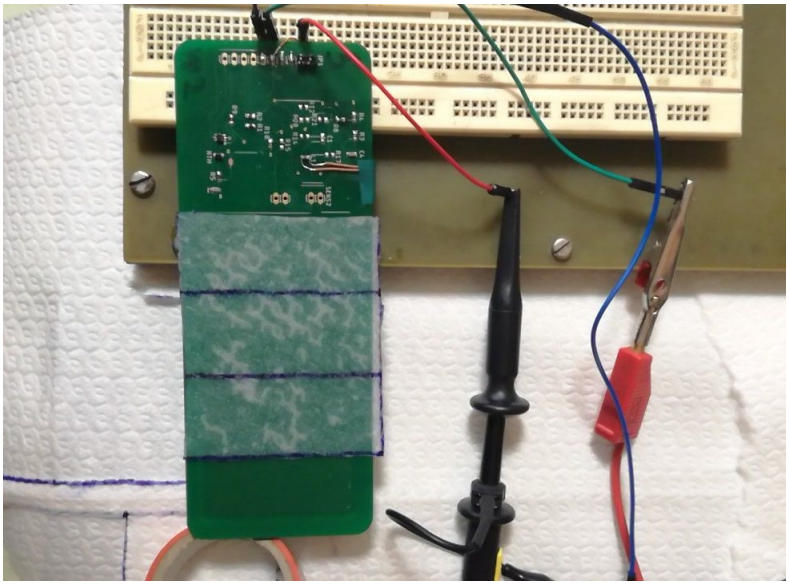


Figure 10.6: Frequency measurement for 75% water covering

10.2 FDC2112 measurments

Since the evaluation module of FDC2112 was implied, the candidate could perform the capacitance measurements with the aid of the Texas instruments' GUI of the evaluation module.
The sensor was connected to the developement board as reported in figure 10.10.

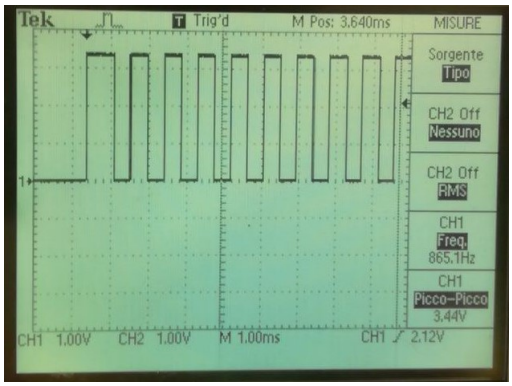


Figure 10.7: Oscilloscope view for the LMC of the case with 75% of water

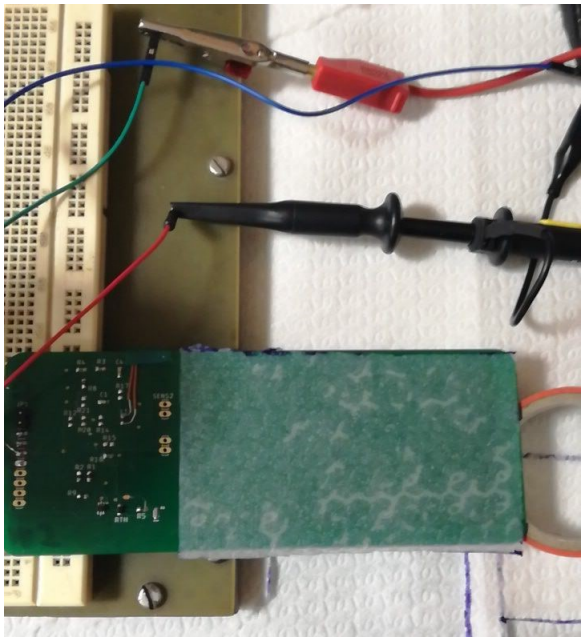


Figure 10.8: Frequency measurement for 100% water covering

The same condition measured with the LMC555 were repeated and the capacitance was measured by mean of the FDC2112 capacitance to digital converter.

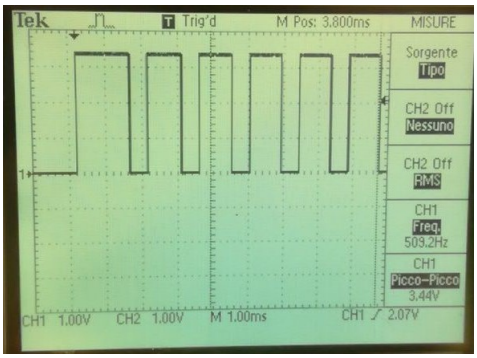


Figure 10.9: Oscilloscope view for the LMC of the case with 100% of water

Covering [%]	Capacitance [F]
0	3,46E-10
25	6,88E-10
50	9,89E-10
75	1,67E-09
100	2,84E-09

Table 10.1: Table containing measurement results of the LMC555 integrated circuit

In table 10.2 are reported the results achieved by mean of the FDC2112 EVM.

Covering [%]	Capacitance [F]
0	3,80E-10
25	6,79E-10
50	1,04E-09
75	1,41E-09
100	1,71E-09

Table 10.2: Table containing measurement results of the FDC2112 integrated circuit

For both measurement systems the results matched quite well the simulation results. The results provided by the LMC timer were extremely similar to the ones provided by the FDC2112.

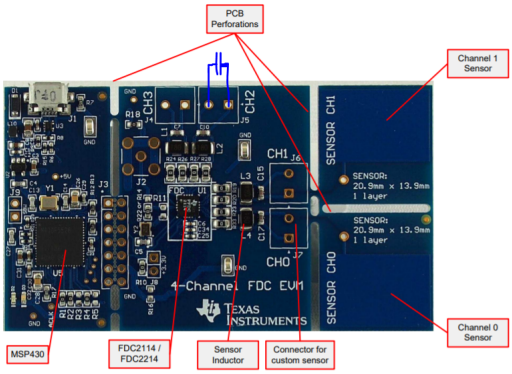


Figure 10.10: Sensor connection to the FDC2112 integrated circuit, in blue

Part IV

Conclusions

The overall project was divided in steps, in order to make the design as simple as possible.
First it was required to have a sufficient knowledge about capacitors physics, particularly it was needed to clearly understand how interdigital capacitors work, since the sensor to be developed behaves like a variable interdigital capacitor.
After the documentation step, there was the modeling step, in which the candidate created a reliable 3D model of the sensor and simulated it through a multiphysics simulator.
The third thing to think about was the real implementation of the sensor, therefore the printed circuit board was designed and produced.
Once the PCB arrived from the manufaturer, the bought components were mounted, after this the candidate had also to verify the system correct functionality, fixing the issues that came out and trying alternative solutions to improve the results.
This allowed the candidate to make a lot of practice with the available laboratory instrumentation.
More over, the support offered by the team of the iXem Labs, particularly by Eng. Mattia Poletti, was necessary to perform a correct design without loosing too much time, which in an experimental thesis is one of the major issues that affetct its realization.
The output of the thesis will result useful to the iXem Labs which, starting from the obtained results, will have a reference model to study, improve and transofrm into a commercial solution for their precision farming activity.

Appendices

Appendix A

A brief introduction to LoRa alliance

All the information provided in this appendix was taken from https://lora-alliance.org/ and it is reported here for sake of clarity.

A.1 Lora wan devices

LoRaWAN devices have a particular configuration: They support bi-directional communication between a device and a gateway. Uplink messages (from the device to the server) can be sent at any time (randomly). The device then opens two receive windows at specified times (1s and 2s) after an uplink transmission. If the server does not respond in either of these receive windows (situation 1 in the figure), the next opportunity will be after the next uplink transmission from the device. The server can respond either in the first receive window, or in the second receive window, but should not use both windows.

A.2 Operating frequency

LoRaWAN operates in unlicensed radio spectrum. This means that anyone can use the radio frequencies without having to pay million dollar fees for transmission rights. LoRaWAN transmission frequency is different for worldwide countries, for instance in Europe LoRaWAN operates in the 863-870 MHz frequency band. European frequency regulations impose specific duty-cycles on devices for each sub-band. These apply to each device that transmits on a certain frequency, so

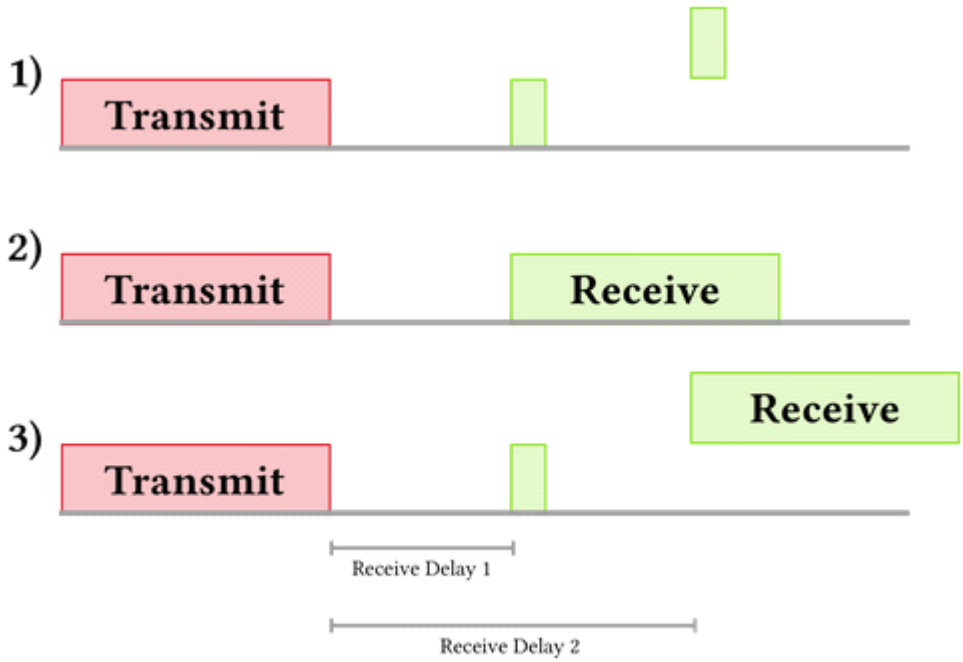


Figure A.1: LoRa wan handshake

both gateways and devices have to respect these duty-cycles.

A.3 modulation

In most cases LoRaWAN uses LoRa modulation. LoRa modulation is based on Chirp spread- spectrum technology, which makes it work well with channel noise, multipath fading and the Doppler effect, even at low power.

A.4 data rate

The data rate depends on the used bandwidth and spreading factor. LoRaWAN can use channels with a bandwidth of either 125 kHz, 250 kHz or 500 kHz, depending on the region or the frequency plan. The spreading factor is chosen by the end-device and influences the time it takes to transmit a frame.

[1] Biradar, Hemavathi B., and Laxmi Shabadi. "Review on IOT based multi-disciplinary models for smart farming." 2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT). IEEE, 2017.

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