

POLITECNICO DI TORINO

Faculty of Engineering
Master of Science in Electronics Engineering

Master's Thesis

**Lab-On-Chip Device for
High Throughput Multi-Analysis
Single Cell Studies**



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*Children are born with wings,
teachers help them to fly*

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*Federico Bedini
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Summary

Lab-on-chip (LoC) devices embody several key features, including the use of small sample volume, control over fluid dynamics, easy integration of cell manipulation techniques (cell sorting, cell isolation) and higher throughput than conventional analytical methods (e.g. patch clamp). Impedance flow cytometry (IFC) has been widely adopted for high-throughput cell detection and manipulation, sorting and counting. IFC works by measuring the impedance between a set of electrodes as single cells pass through a microchannel. IFC, however, allows only for short-term single-cell analysis. Microelectrode arrays (MEAs) are often used to perform long-term analysis of cell populations. Coupled with electrical impedance spectroscopy (EIS), adhesion, morphology, proliferation and temporal evolution of cells can be analysed.

In this work, a novel LoC device is proposed, which integrates in-channel IFC and in-chamber MEAs in the same microfluidic platform. The microfluidic chip is fabricated on standard Si wafers through a CMOS-compatible photolithographic process, allowing for future microelectronics integration. Several versions of the chip are realized on the same Si wafer, diced and singularly tested to evaluate the effect of the geometrical parameters and channel configuration on the detection sensitivity. The first design includes IFC electrodes of different sizes at the bottom of a $10 \times 10 \mu\text{m}^2$ microchannel, and a culture chamber comprising of 9 microwells with interdigitated electrodes. Different IDEs parameters (width from $10 \mu\text{m}$ to $100 \mu\text{m}$, gap from $5 \mu\text{m}$ to $20 \mu\text{m}$) are also realized to assess optimum geometries for high sensitivity and SNR. The IFC and MEA electrodes are characterised using a multichannel impedance analyser.

Integration of IFC and MEAs in the same platform enables automated, high-throughput single-cell sorting and manipulation and long-term network analysis, allowing for more comprehensive studies of cell cultures.

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Part I

Theory and Background

Chapter 1

Introduction

Lab-On-Chip technology is gaining more and more interest in the scientific community, for its promises of enhancing the capabilities of biomedical instrumentations with reduced sample volumes, small dimensions, multiple functions integration. The precision of microfabrication techniques, applied to the biomedical world, created a new paradigm for biological analysis, with microchannels where fluids don't answer to physical laws as we're used to, electrodes so small that are able to study single cells individually, and the prospective of a combination between the biological, the electrical and the mechanical world. In this scenario, addressing the technological challenges for the co-integration of microfluidics and microelectronics becomes of the foremost importance, to unlock the potentialities of such a device, as sub-micrometric resolution, ultrafast response time, automatic measurements and compactness.

In this thesis, a novel Lab-On-Chip device is proposed, which integrates two state-of-the-art techniques for cell analysis: Impedance Flow Cytometry (IFC) and Electrochemical Impedance Spectroscopy (EIS). IFC, that is a fast, single-cell detection strategy, cannot provide long-term analysis of cells, while EIS, despite being suitable for long-term analysis, can only detect average data from cell populations. Beside the analysis of the advantages obtained by merging the two detection methods, the aim of this project is the realization of a proof of concept to demonstrate the co-integration of microfluidics and CMOS processing, leading the way toward a next generation of microfluidic devices (by some defined as Lab-On-CMOS/Bio-CMOS). The work is subdivided as follows:

Chapter 2 wants to give some insights on blood composition and cell biology, to acknowledge the reader on the measurand quantities when performing impedance cytometry. A section on electrical models of cells is present, the idea is to investigate equivalent circuits to interface biological characteristics with cells impedance spectrum.

Chapter 3 is a short review on Lab-On-Chip research, which tries to introduce the reader to the field of microfluidics and to the main techniques to perform cytometry (i.e. to study cell characteristics). Flow Cytometry is described, as state-of-the-art technique to count, separate and characterize cells, and Impedance Flow Cytometry is presented as possible candidate for a label-free, lens-free, cheap, automated alternative. Analogously, Electrochemical Impedance Spectroscopy is proposed as a long-term, lens-free, real-time imaging system to be used with Interdigitated Electrodes microfabricated on the bottom of microwells.

Chapter 4 explains the design choices taken to realize the chip. The chapter starts with a description of the geometries, highlighting parameters that should be analysed to improve the signal-to-noise ratio (SNR). Several parameters were investigated, and ten different designs were realized, all subsequently fabricated on silicon wafers. Then, a description of the materials of which the chip will be made is presented, as an introduction to microfabrication techniques. Finally, last section addresses photolithographic masks design and fabrication (mask designs can be found in the Appendices).

Chapter 5 is dedicated to the microfabrication of the chip. The facility in which the chip was fabricated is the Else Kooi Lab (EKL), comprising of cleanrooms class 100 and 10'000. A short description of the lab is given, together with the main rules of behaviour. A second part of the chapter is dedicated to describe tests and trials that have been run before the actual production. After that, the whole fabrication process of the chip is addressed step by step (flowcharts for trials and for chip fabrication can be found in the Appendices).

Chapter 6 describes the system integration of the chip. After cleanroom fabrication, wafers are diced and single chips are tested to ensure functionality. PCB are designed, pin headers are soldered to them, and the chips are ultrasonically bonded. To finish system level integration, a lid to cover the microchannel would be needed, to seal the chip and to host microfluidic interconnection. The last part of this chapter is therefore dedicated to briefly explore some sealing choices.

Chapter 7 deals with the measurements performed on the chips after they have been fabricated. A first description of the electrical characterization is provided, then the electrochemical testing setup is described and curves representing the dependency of electrode impedance on frequency are shown.

Chapter 8 summarizes the results obtained, showing the goals reached and highlighting the recognised lacks, a set of proposed steps for the continuation of the work is presented, and a final brief paragraph on the future perspectives of this project concludes the thesis.

Chapter 2

Cells in Human Blood

Blood is a complex fluid, composed by $\sim 55\%$ of a liquid phase (plasma, which is $\sim 90\%$ water and $\sim 10\%$ proteins), and by $\sim 45\%$ of suspended cells. We can subdivide these cells in erythrocytes (red blood cells, RBCs), that are the majority and outnumber other cells by 1000:1; leukocytes (white blood cells, WBCs), subdivided in lymphocytes, monocytes and granulocytes; and thrombocytes (platelets) [1]. RBCs are responsible of carrying oxygen from lungs to the rest of the body, are $6-8\mu\text{m}$ of diameter, and have no nucleus. WBCs are less numerous but bigger (from $7-8\mu\text{m}$ to $15-30\mu\text{m}$), and have the duty to protect the body from infections and foreign invaders, they are in fact part of the immune system. Platelets are lens-shaped structures of $2-3\mu\text{m}$ of diameter, and they are actually fragments of cytoplasm derived from cells of the bone marrow. They coagulates when an injury happens, and they form a fibrin clot which covers the wound and prevents blood from leaking out. Fig. 2.1 shows a colourized SEM picture of these three kinds of cells.

Peripheral blood test is one of the most common medical exams, and the analysis of its content is critical for the detection of numerous pathologies. Several medical tests are available to study blood cells (e.g. complete blood count, CBC), but they tend to be slow, and bulky instrumentations and trained staff is required in order to analyse the data, which makes it difficult to realize on-site analysis, especially in areas where a biotechnology lab is not present. Furthermore, despite being suited for measuring huge numbers of blood parameters, they usually lacks in single-cell precision, which can be a problem when dealing with particular pathologies (e.g. detection of circulating tumor cells for early diagnosis of metastasis). For this reason, several new approaches have been investigated, in order to provide new cytometry devices able to measure cell characteristics in a fast, cheap and automated way. Usually these new devices rely on the use of microfluidic channels and Lab-On-Chip technology (more details in chapter 3).

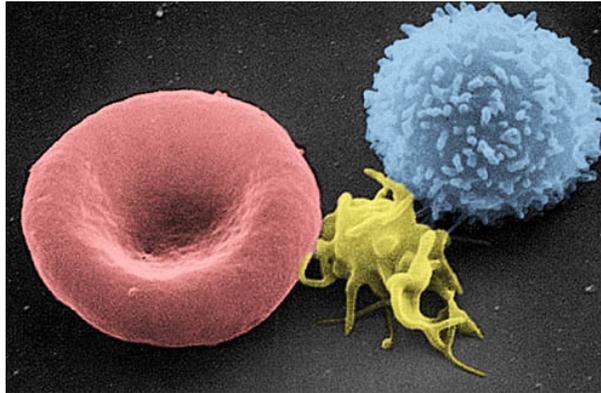


Figure 2.1. SEM micrograph of the three types of cells of human blood: erythrocyte, thrombocyte, leukocyte (from left to right). Public domain picture from Electron Microscopy Facility at The National Cancer Institute at Frederick.

In this work a device able to measure biological characteristics of cells is presented, that uses high frequency impedance sensing to investigate variability in cell populations. In the following chapters the device will be described, starting from its design and explaining fabrication choices, while this chapter will explain how it is possible to perform cytometry using cell impedance as measurand, i.e. trying to match biological characteristics and electrical characteristics of cells: section 2.1 will give a brief description of the main components of an animal (eukaryotic) cell, section 2.2 will describe some electrical models proposed as equivalent circuits for cell impedance.

2.1 Biology of a Cell

Cells are the functional units of living beings, and the smallest structures to be considered "alive". They can live on their own, thus constituting a unicellular organism, or create complex structures and systems, giving rise to very complex multicellular organisms. Cells are subdivided in eukaryotes (cells with a membrane separating the nucleus from the cytoplasm) and prokaryotes (much simpler cells with genetic material mixed in the cytoplasm). Animals are eukaryotes, and their cells, despite some major differences coming from their functions, can all be described following a similar model (see Fig. 2.2): a lipid bilayer cell membrane that contains a fluid, i.e. the cytoplasm, where several organelles float, each one with its duty. The core of the cell is the nucleus, a region delimited by a membrane that contains the genetic code in the form of DNA. Around it there is the endoplasmic reticulum, a series of membranes covered by ribosomes, that perform protein synthesis.

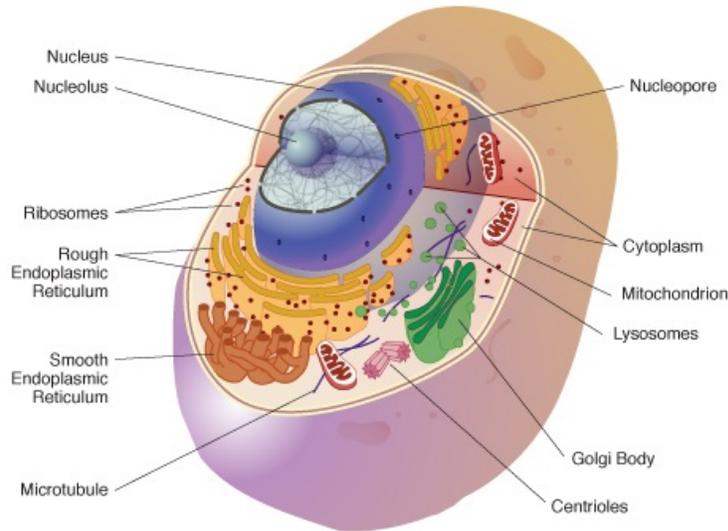


Figure 2.2. Drawing of an animal cell, with a representation of its interior and organelles.

Many biological parameters could influence the impedance of a cell. First of all its size, spanning from few μm to several tens of μm , is an important factor, but also the thickness of its membrane, its health state, and its content can influence the impedance spectrum. An important thing to notice is that membranes are made of a lipid bilayer, which is a dielectric, thus it is usually considered source of capacitance (C in the order of $\sim 2 \mu\text{F}/\text{cm}^2$), while the interior of a cell, mainly cytoplasm, for its rich concentration of ions is usually considered a conductive fluid (conductance of $\sim 1 \text{ S}/\text{m}$) [2].

2.2 Electrical Models

To study the electrochemical impedance of a cell in a conductive medium, by means of two metal electrodes, several models have been proposed, on the basis of cell structure, electrochemical measurements and curve fitting. When two electrodes are separated by a high impedance medium (e.g. air), they create a circuit with a very high R (hundreds of GOhms). It is, in fact, the definition of open circuit, but if the electrodes are close enough the circuit represents a capacitor. When the two electrodes are wetted with a conductive solution, the behaviour changes: the first thing to be noticed is the creation of a ionic double layer on the surface of the electrodes, which acts as a very big capacitor (C_{DL} , depending on electrode size, solution conductivity and other geometrical parameters).

The equivalent circuit of two electrodes in a conductive medium is therefore a capacitor representing the double layer in series with the resistance and the conductance of the medium (this last one usually is omitted since its negligible with respect to C_{DL}). When a cell (to be considered as a dielectric particle) passes between the two electrodes, what happens is that the electromagnetic field generated between the two metals is deviated by it, producing a variation in terms of the equivalent circuit elements.

On the basis of the structure of an eukaryotic animal cell, a simple circuital model of a cell passing between two electrodes in a conductive medium was proposed by Foster and Schwan in 1989 [3], where the impedance of the cell (capacitors indicating the lipid bilayer cell membrane, resistance indicating the cytoplasm) is put in parallel with the impedance of the electrodes and the medium (double layer capacitance, resistance and capacitance of the medium, see Fig. 2.3). Wenwen Gu and Yi Zhao in [4] propose a slightly modified version of equivalent circuit, where the resistance of the medium is split, and only the capacitance of the medium is in parallel with cell impedance (that now comprises also the capacitance of the cytoplasm, see Fig. 2.4). The most complex models in literature take also in consideration the role of the nucleus, that with the endoplasmic reticulum creates the biggest organelle of a cell, as in the case of [5], where resistance and capacitance of the nucleus are put in parallel with the resistance of the cytoplasm (some theoretical values are also simulated, to give a quantitative idea of the equivalent model).

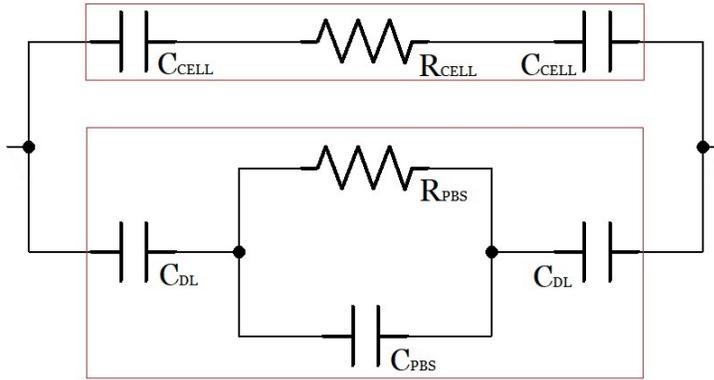


Figure 2.3. Electrical model of a cell as proposed by Foster and Schwan in [3]. Top branch represents the cell, with C_{CELL} as the capacitance of the lipid bilayer cell membrane, and R_{CELL} as the resistance of the cytoplasm; bottom branch represents the electrodes wetted with PBS solution, where C_{DL} is the double layer capacitance, and R_{PBS} and C_{PBS} are resistance and capacitance of the solution

Given the equivalent model, it is important to correlate biological parameters of cells with the discrete elements of the electrical circuit. Variations in size, content, composition, will modify cells impedance spectrum, that can therefore be considered

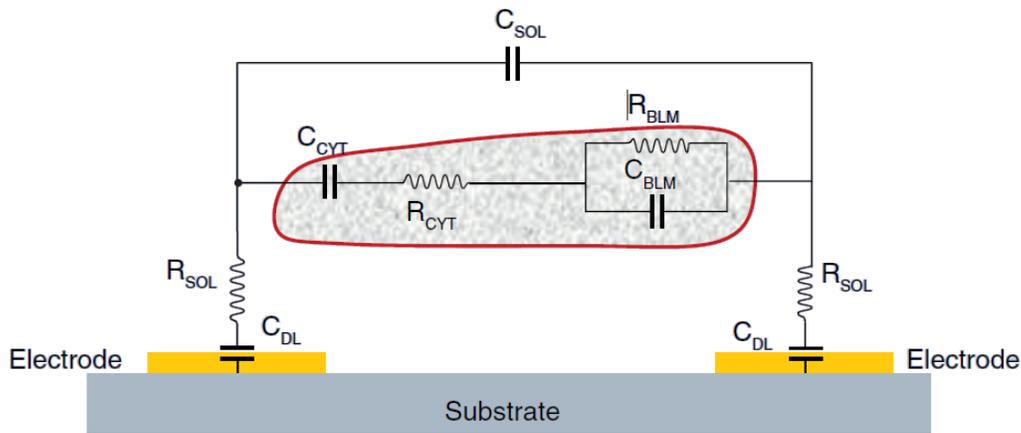


Figure 2.4. Electrical model of a cell as proposed by Wenwen Gu and Yi Zhao in [4]. In this case the cell is represented by resistance and capacitance of both the bilayer membrane (R_{BLM} and C_{BLM}) and of the cytoplasm (R_{CYT} and C_{CYT}).

as an intrinsic label, useful to distinguish between various types of cells. Confronting magnitude and phase of the impedance at various frequencies, it was possible to differentiate RBCs from WBCs [6], particles of different sizes [7], normal RBCs from ghost RBCs (emptied cells) [8], different types of WBCs (lymphocytes, monocytes, granulocytes) [9], proving that the impedance spectrum of cells can be correlated to biological characteristics, and can be used to differentiate them via high frequency investigation (usually frequencies between 100kHz and 10MHz are used, to bypass double layer capacitance without bypassing membrane capacitance, even if higher frequencies could be used to investigate the interior of a cell [10]).

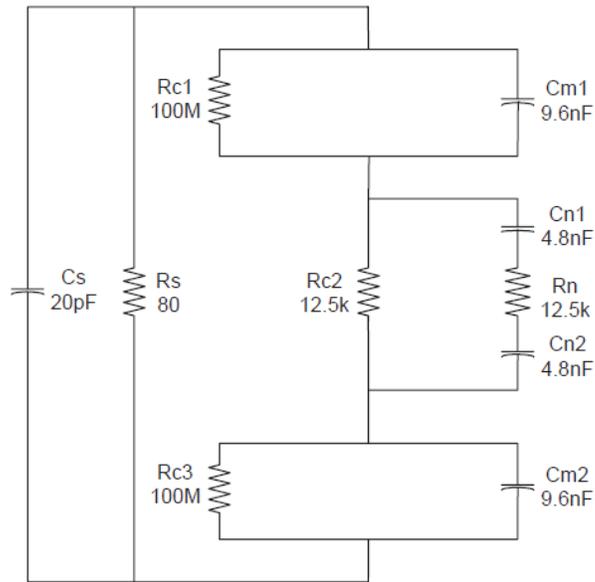


Figure 2.5. Electrical model of a cell as proposed in [5]. In this case a complete electrochemical simulation was carried on, and theoretical values have been extracted from the model. R_{C1} , C_{M1} , R_{C3} , C_{M2} are resistances and capacitances of the bilayer membrane; R_{C2} is the resistance of the cytoplasm; R_N , C_{N1} , C_{N2} are resistance and capacitances of the nucleus; R_S , C_S are resistance and capacitance of the solution.

Chapter 3

Microfluidics

Microfluidics is the science that deals with the study of fluid behaviour at the micro/nano scale, and with the manufacturing techniques for realizing devices for the transport and handling of microliters (or even smaller quantities) of fluids. Microfluidic systems dealing with such small fluid samples can support different applications, such as DNA sequencing, chemical synthesis/analysis and ink-jet printing.

Microfluidic systems consist of devices for control, monitoring, transport, mixing and analysis of fluid samples [11]; such devices, commonly known as "Lab-On-Chip" or " μ TAS" (Micro Total Analysis Systems), must be functionally integrated on a microfluidic platform by adopting the appropriate micro and nano-manufacturing techniques.

An important thing to keep in mind when dealing with the micro/nano world, is that physical laws not always scale linearly with dimensions: most of the times, to a decrease of dimensions of α corresponds a quadratic (α^2), cubic (α^3) or even greater variation of the other laws. Table 3.1 summarizes scaling law for some of the forces that play an important role in microfluidics. This is a fundamental property of microfluidics, as many phenomenons that happen at the macroscale are different at the microscale (e.g. gravity doesn't play an important role, and capillarity becomes fundamental).

One of the most visible characteristics of fluidodynamics at the microscale is the absence of turbulence, i.e. if a fluid has a Reynold's number $R_e < 2000$ it will be denoted as laminar, meaning that there won't be mixing due to turbulences. Reynold's number is defined as:

$$R_e = \frac{\rho d \nu}{\eta}$$

where ρ is the density of the fluid, d is the diameter of the channel where the liquid is passing, ν is the velocity of the fluid and η is its viscosity.

Intermolecular Van der Waals force	α^{-7}	Diffusion time	α^2
Density of Van der Waals force bw interfaces	α^{-3}	Volume	α^3
Time	α^0	Mass	α^3
Capillary force	α^1	Force of gravity	α^3
Distance	α^1	Magnetic force with an ext. field	α^3
Flow velocity	α^1	Magnetic force without an ext. field	α^4
Thermal power transferred by conduction	α^1	Electrical motive power	α^3
Electrostatic force	α^2	Centrifugal force	α^4

Table 3.1. Summary of scaling law for principal forces in micro/nano fluidics.

In a microchannel Reynold's number is always < 100 , and this means that the flux is always to be considered laminar.

3.1 Lab on Chip

After the discovery of microtechnology to build integrated semiconductor structures for microelectronic chips, these technologies based on lithographic techniques were soon applied to create Micro Electro Mechanical Systems (MEMS), microdevices able to act as sensors and actuators. Lab-On-Chip (LOC) is a sub-category of MEMS, meaning a device made of a single chip that integrates multiple functions, usually performed in a laboratory (Fig. 3.1). The chip goes from a few millimetres to a few centimetres square and is able to handle extremely small volumes of fluids, even under the picolitres. Although the LOC reality is still new, a series of advantages is already clear:

- Low volumes of fluid consumption, given the small internal volume of the chip, which is beneficial for environmental pollution (less waste), lowers the cost of expensive reagents and less sample fluid is used for diagnosis;
- Better analysis and chip control, and better efficiency thanks to fast diffusion and fast heating (low distances, high ratio between the surface and the volume of the fluid, low energy capacity);
- Better process control thanks to faster system response (temperature control for exothermic chemical reactions);
- System compactness, due to the great integration of functionalities and small volumes;
- Enormous parallelization, which makes high output analysis possible;

- Lower manufacturing costs, with the possibility of producing low-cost disposable chips, manufactured through mass production;
- Safer platform for chemical, radioactive or biological studies thanks to high integration and isolation of very small quantities of fluids.

Initially, LOCs were realized like their MEMS counterpart in silicon, with microelectronics fabrication techniques, but more recently, to add optical/chemical properties to the chip, or to speed up prototyping, new fabrication techniques have been investigated, as stereolithography, injection moulding, hot embossing, PDMS casting, additive manufacturing [12], [13].

Many fields of biotechnology have taken advantages from microfluidics and Lab-On-Chips, and many operations that used to take days/weeks, like DNA sequencing and PCR, now last just few moments [11]. Another fundamental application where Lab-On-Chip gave a major contribution is cytometry, i.e. the measurements of the characteristics of cells. With the aid of microchannels and electrodes cells are moved, sorted, and their electrical properties are measured, and by data analysis it is possible to refer those measurements to biological characteristics (size, type, presence of abnormalities, and so on).

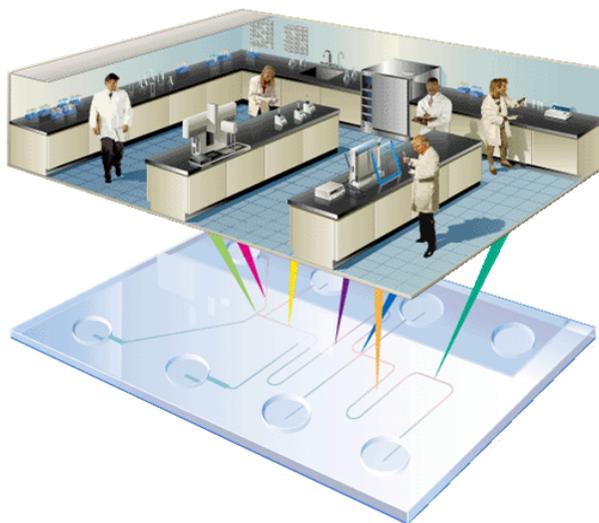


Figure 3.1. Concept of a LOC: several analytical tools and protocols, often performed in a biotechnology lab, can be recreated in few mm^2 using microfabrication techniques and electronics.

3.2 Flow Cytometry

Flow cytometry is a laboratory technique in the biomedical field that uses a laser light beam for detection, counting, characterization of suspended cells. It relies on the use of a flow cytometer, which is able to simultaneously measure several morphological parameters deriving from the crossing of single cells through a beam of laser light, which is scattered and detected by means of lenses and optical filters (Fig. 3.2). Usually, this method requires a labelling operation on cells that have to be analyzed, utilizing fluorochromes (fluorescent molecules), in which case it is called fluorocytometry.

Using multiple laser beams, several parameters of cells can be detected simultaneously. Moreover, some flow cytometer are provided with a splitter, that first separates the flux in droplets, each one containing a cell, and subsequently, reading the information obtained by fluorocytometry, it is able to send each droplet in a different compartments using electromagnetic fields, thus obtaining samples of already subdivided populations (e.g. all the differentiated cells in one compartment, cells that still have to be differentiated in another compartment, dead cells in waste). In this case the technique is called Fluorescent-Activated Cell Sorting (FACS).

Fluorocytometry and FACS have been used for decades for several different applications [14], [15]. Beside the bulky and expensive instrumentation required, the main drawback is the need of the labelling operation, requiring trained staff and additional time. To avoid this, an alternative to fluorocytometry has captured the attention of researchers: impedance flow cytometry.

3.2.1 Impedance Flow Cytometry

The idea of using impedance measurements to reveal biological parameters of cells is actually older than fluorocytometry: in the '30s Wallace Coulter developed a system able to count cells suspended in an electrolyte solution by using electrodes and a microchannel. The device, called Coulter Counter, evolved until becoming the standard in cell counting, but its development eventually stopped, in favour of the more advanced flow cytometer, able to detect much more parameters thanks to the use of different markers [16], [17].

With the advancements of microtechnology and its contributions to microfluidics, Lab-On-Chip research became huge, giving a new life to the idea of electrodes measuring the impedance of cells [18], [19]. The aim of this new research topic is to develop devices integrating electrodes inside microchannels, in order to measure the impedance of fast travelling cells, allowing for a label-free, automatic and fast measurement.

The first results in this direction have been obtained at EPFL by Ayliffe et al.

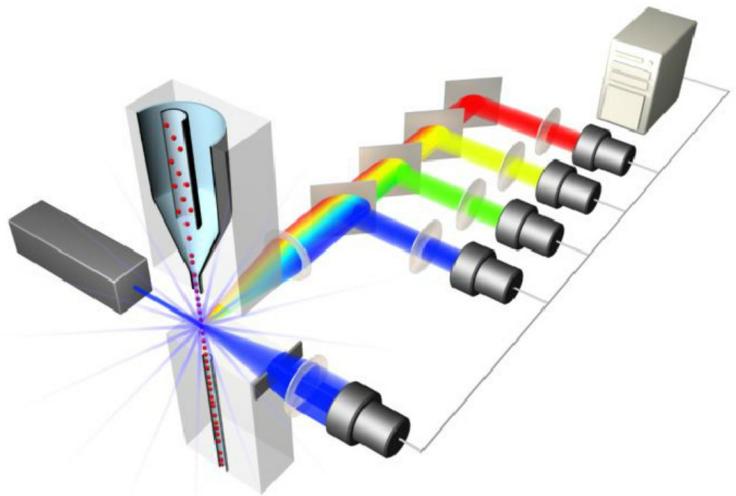


Figure 3.2. Graphical representation of the functioning method of a fluorocytometer. Cells are aligned thanks to a microchannel in a flux of individual particles. A laser is pointed at the flux, and when it hits a cell, light will scatter, with an intensity proportional to the size of the particle and a wavelength depending on the fluorochrome bonded to the cell. Scattered light is directed, with lenses and filters, to photodiodes, and analysed with a PC.

first [6] (see Fig. 3.3) and then by Gawad et al. [7], [8]. Subsequently, Lab-On-Chip devices for impedance flow cytometry have been developed and tested for a series of different operations, as particle sizing [20], leukocyte analysis [9] (see Fig. 3.4), differentiation of stem cells [21] (see Fig 3.5), and using different approaches, e.g. using different frequencies [10], removing sheat fluid [22], investigating design choices for the realization of microelectrodes in order to optimize particle readout [23].

3.3 Long-Term Cell Analysis

One drawback of flow cytometry is that the sample of cell used to perform the measurement gets lost in the process, i.e. there is no further way of collect the population of cell to perform long-term analysis. The common way to perform long-term analysis on cells is to study them in a Petri dish under optical microscope (advanced instrumentations can be used to improve resolution, i.e. fluorescent microscope, confocal microscope, phase-contrast, etc), but they require trained staff, they can't be automatized and they require time, reason why usually cell cultures are not constantly monitored.

A recent advance toward the automation of measurements comes from the development of culture wells equipped with interdigitated electrodes (IDEs), that can

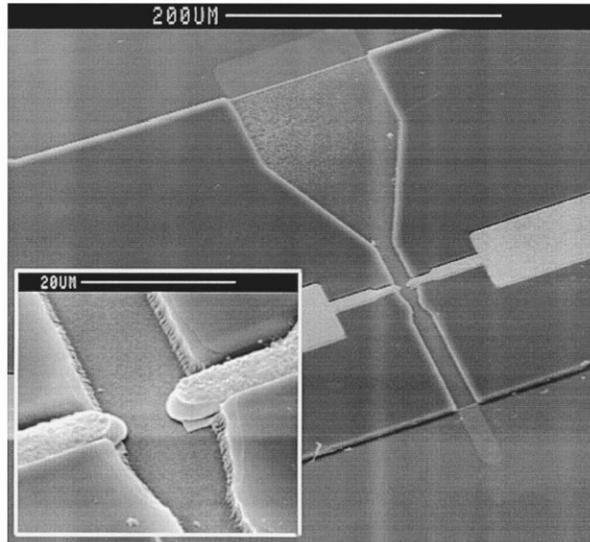


Figure 3.3. SEM micrograph of the microchannel (and zoom on the electrodes) realized in [6]. The two gold electrodes were patterned such that only one cell at a time could cross them, modifying their impedance.

be individually addressed and used for electrical stimulation/sensing of the cultured cells (Fig. 3.6). Microtechnology advancements have provided a way of integrating IDEs in microfabricated wells, to address cells directly at the microscale. Wells can be realized with standard microfabrication techniques (Fig. 3.7), and IDEs can be used to perform several kind of measurements on cells, like cyclic-voltammetry, i.e. varying voltage to read current response, or electrical/electrochemical impedance spectroscopy (EIS), i.e. interrogating cells at multiple frequencies to read their impedance spectrum.

3.3.1 Electrochemical Impedance Spectroscopy

Electrochemical Impedance Spectroscopy (EIS), thanks to the advantages of being a real-time, label-free, non-invasive technique, and intrinsically scalable nature, has been proven to be a great option for cellular biochemical sensing. With EIS it is possible to monitor small regions using IDEs, and convert the information in spectral impedance values. It works by applying a V_s (at different frequencies) to one of the electrodes, and reading the current I_s (also function of frequency) from the other electrode. The impedance Z_s is therefore calculated as V_s/I_s , considering both magnitude and phase of the applied signal and of the sensed current [4].

The first approach of IDEs to perform EIS in electrolytic solution was investigated by Norman Sheppard et al, from John Hopkins University, Baltimore, that in 1993 built and tested microfabricated IDEs to be used as miniature conductivity

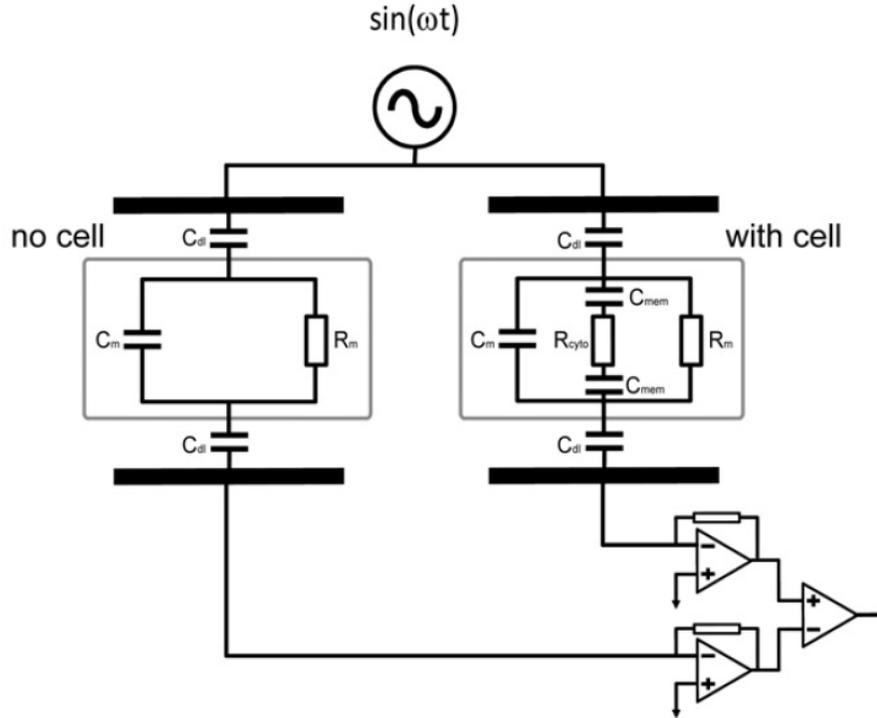


Figure 3.4. Example of readout circuit proposed by Holmes et al. in [9]. In this case two coplanar pair of electrodes are used to sense the cell. A sinusoidal signal at a predefined frequency is applied on one side, and current is sensed on the other side, converted in voltage with two transimpedance amplifier and measured with a differential amplifier.

cells [26]. Microfabrication of electrodes was done in the Microsystems Technology Laboratory of MIT. Later on, this method was employed and investigated by several research institutes worldwide, because of its advantages in terms of integration.

Frank Alexander et al. from University of South Florida used IDEs to perform an impedance based evaluation of Hs 578T cancer cells [27], while Xin Liu et al., from University of Missouri, Columbia, created a device with microwells able to address, thanks to microelectrodes, single cells, for amperometric detection of quantal exocytosis [28].

Kosuke Ino et al., from Tohoku University, Japan, proposed a device composed with 1024 microwells equipped with IDEs (see Fig. 3.8), placed in a 32x32 matrix configuration, singularly addressable with row and column multiplexers, for high-throughput electrochemical detection using redox cycling [29]. Later on, they proposed a modified version of the device, with new well and electrode design [30].

Akram El Hasni et al. (Aachen University, Germany) managed to realize a device for EIS, realized in SU-8 and PDMS, able to hydrodynamically trap cells

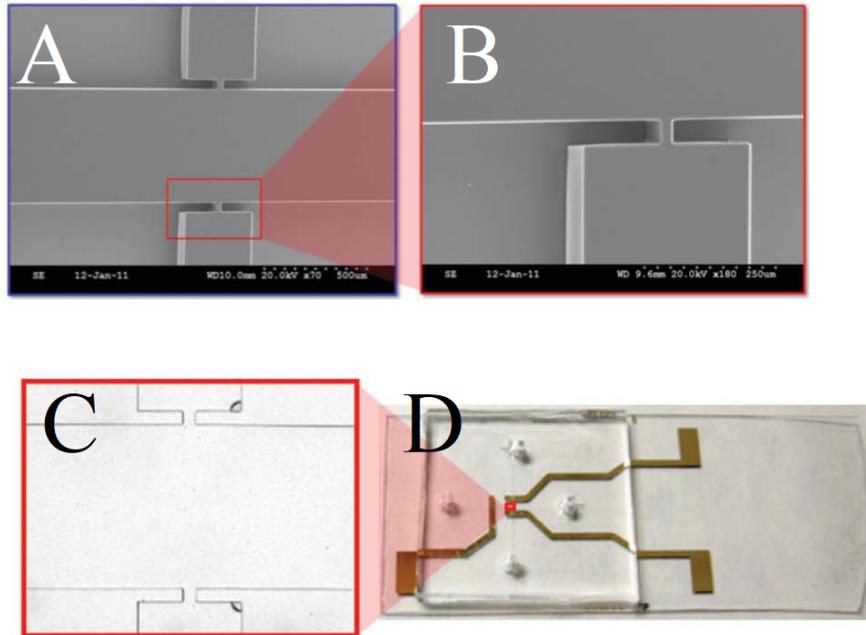


Figure 3.5. Pictures (from [21]) of the device proposed by Song et al. for the identification of differentiation state of stem cells. A) SEM micrograph of the middle chamber, with the two side chambers; B) SEM micrograph of the channel between middle chamber and one of the two side chamber; C) picture taken under microscope of the middle chamber, with the two side chambers; D) picture of the device, where the electrodes are visible.

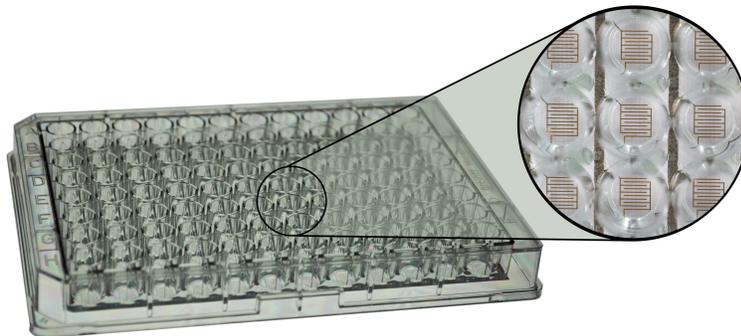


Figure 3.6. A standard microwell plate from Applied BioPhysics [24], equipped with IDEs for every well, used for cell culturing and electrical data acquisition.

in wells equipped with 4 golden electrodes (covered with PPy:PSS, a conductive polymer, to decrease interface impedance), to perform EIS on single cells, with a multi-impedance technique [31] (it was possible to correlate the impedances between each pair of electrodes, the most significative being $Z_{14, 13}$, Z_{24} , Z_{23}).

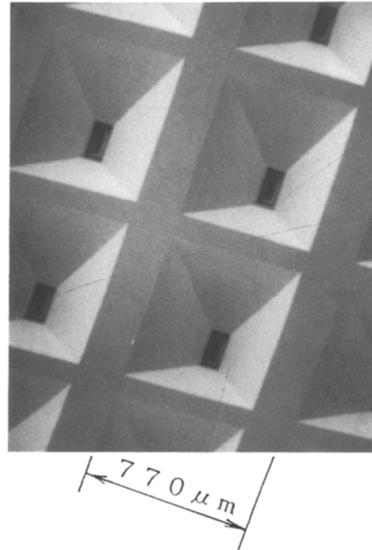


Figure 3.7. Microfabricated wells from Kazuo Sato et al. [25], that in 1990 first addressed micromachining techniques to realize devices for cell studies. The wells were etched from a single-crystal silicon wafer with (100) surface orientation by KOH etching, thus creating the usual inverted-pyramid shape.

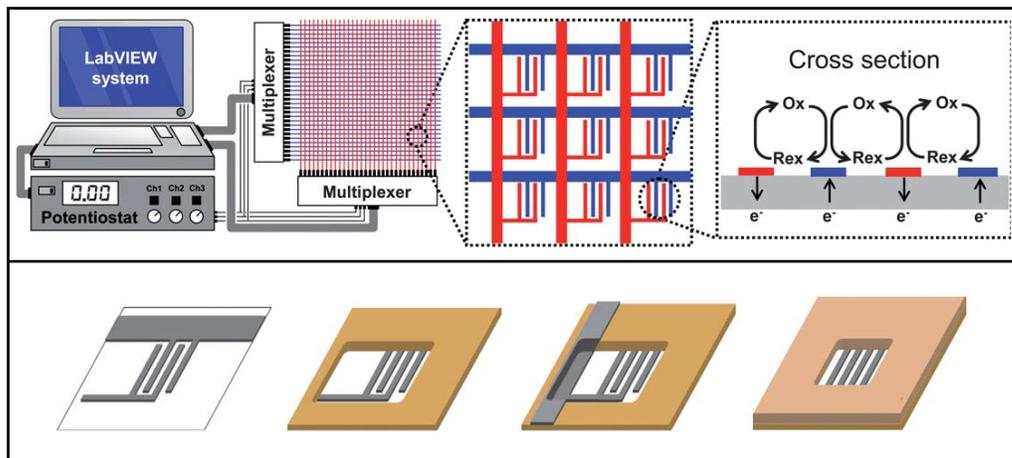


Figure 3.8. Graphical representation of the 32x32 matrix of IDEs (top) and of the realization steps needed to realize a single well (bottom) of the device proposed by Kosuke Ino et al. in [29].

Several other research institutes investigated IDEs sensor for EIS on living cells,

proposing them as solutions for highly integrated, fast, label-free, automated, long-term analysis of cells (for additional applications refer to [4], [32]), but to the knowledge of the authors the co-integration of impedance flow cytometry and electrochemical impedance spectroscopy in the same chip has not been investigated yet. The scope of this thesis was therefore to model, design, realize and test a Lab-On-Chip device able to simultaneously perform IFC and EIS, in order to obtain the advantages of both techniques (fast, high-throughput, single-cell measurements from IFC and multi-frequency, long-time analysis from EIS).

Part II
Device Fabrication

Chapter 4

Design

The aim of this work was to design, realize and test a Lab-On-Chip device able to perform multiple impedance sensing operations on living cells, exploiting both the fast, single cell sensing capabilities of the flow cytometry, and the long-term monitoring capability of wells with interdigitated electrodes (IDEs). In order to do so, the desired Lab-On-Chip must have a combination of narrow channels, where electrodes would perform Impedance Flow Cytometry (IFC), and microwells, where cells would accumulate and IDEs would perform Electrochemical Impedance Spectroscopy (EIS). The first concept of the device was therefore designed to have a central chamber with 9 wells for EIS, and 2 microchannels (one inlet and one outlet) for IFC (Fig. 4.1). This chapter describes the several design choices that have been made in order to optimize the device: first the geometries of the microfluidic chip will be discussed, with a focus on the different designs, then the materials chosen to be used in the cleanroom are presented, and finally an insight on photolithography mask design/fabrication is given.

4.1 Geometries

Before deciding the dimensions our microfluidic system would have, we investigated possible uses of the chip, to adapt dimensions to the specific aim, thus improving the performances. The main concept was that the chip would be used to perform cytometry, i.e. cell detection/measurement, and we decided to optimize the chip for cells of 6-8 and up to $10\mu\text{m}$ in diameter (e.g. erythrocytes). The channel have therefore been designed to have a square aperture of $10\mu\text{m}^2$, to allow cells to align and pass through the IFC electrodes. These electrodes have been designed to be planar, patterned at the bottom of the microchannel, so that when cells pass on top of them, their EM field will be altered, detecting the passage.

In order to increase the Signal-to-Noise Ratio (SNR) three electrodes were used

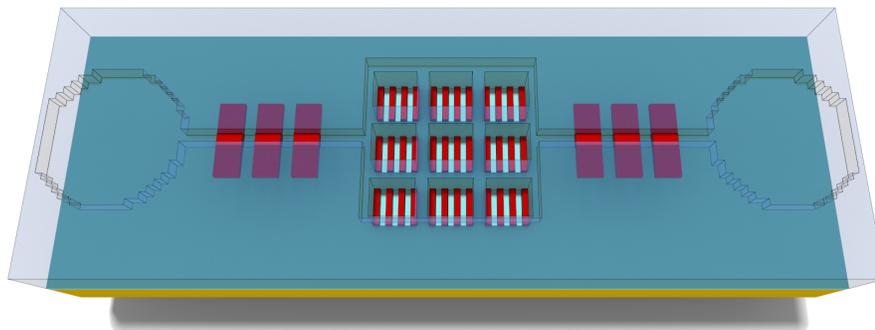


Figure 4.1. 3D concept drawing of the device. A central chamber includes 9 microwells with IDEs for Electrochemical Impedance Spectroscopy, with one inlet and one outlet microchannel with electrodes for Impedance Flow Cytometry.

for IFC measurement, in a pseudo-differential scheme that compare the impedance between the first and the middle electrode, with the impedance between the middle and the last electrode (already proposed by Gawad et al in [7]). A representation of the detection scheme is shown in Fig. 4.2, while Fig. 4.3 proposes a readout circuit based on transimpedance amplifiers.

To test the effect of geometrical parameters on the SNR and to characterize the device, 10 different designs were realized, all of them to be included in the wafer level design of the masks, i.e. all of the 10 designs could be microfabricated using the same flowchart and the same masks. Moreover, all 10 designs are created respecting the same 2cm x 1cm outline and, with the exception of design #9 and #10, the same pinout, to somehow standardize the system level integration of the chip (same PCB, same microfluidic interconnections). Fig. 4.4 show the layout of the 10 designs from the layout editor used to realize the masks (Tanner L-Edit) details on the design choices of each design are presented in the following sections.

4.1.1 Design #1,2,3 and 4

The first series of designs is inspired by the initial concept drawing of the device, and present two circular apertures of 3mm of diameter, connected by a microchannel with height of $10\mu\text{m}$, that starts from a width of $200\mu\text{m}$ and shrinks down to $10\mu\text{m}$ (Fig. 4.5). In the middle there is a wider chamber of $500\mu\text{m} \times 500\mu\text{m}$ with

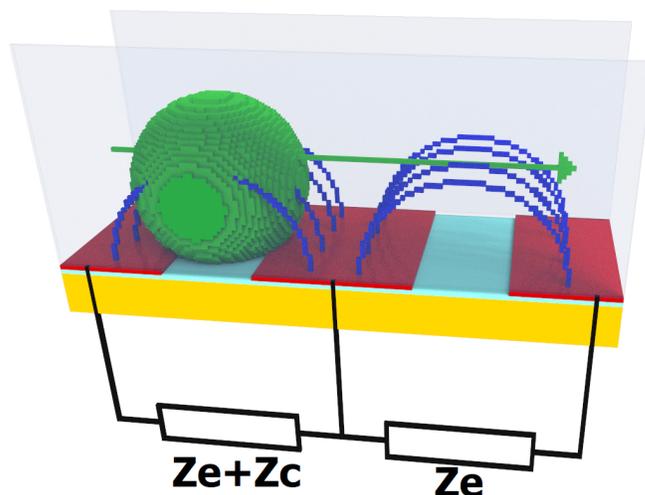


Figure 4.2. 3D concept drawing of the detection mechanism of the 3-electrode configuration for IFC proposed by Gawad et al. in [7]: the cell (green sphere) passes on top of the electrodes (red squares), and varies the impedance of one couple of electrodes at a time, from Z_e (impedance of electrodes in PBS solution) to $Z_e + Z_c$ (impedance of electrodes modified by the presence of a cell interfering with the EM field generated by the electrodes). When the cell moves, the first couple of electrodes will have again impedance Z_e , and now the second couple of electrodes will have impedance $Z_e + Z_c$. The variations will be sensed by a differential amplifier.

9 wells ($100\mu\text{m} \times 100\mu\text{m}$, and $10\mu\text{m}$ deep). Inside the wells there are interdigitated electrodes, in particular there is a common ground electrode and 9 singular IDEs (10 pads in total, see Fig. 4.6). The difference in these four designs regards the IFC electrodes: Carminati et al. in [23] gives a way on how to design an Impedance Flow Cytometer in a 2/3 planar electrode configuration, mathematically optimizing channel width and height, electrode length, width and gap (a 3D representation of the IFC electrodes with the relevant geometrical parameters is shown in Fig. 4.7), suggesting that the most important parameter to be fixed is the gap between the electrodes (G_e), since it is strictly related to the height of the fringing electromagnetic field between the electrodes, that has to be similar to the dimensions of the objects to be measured. The channel height (H_c) is therefore important because it confines the EM field. Electrode width (W_e) loses importance since the actual exposed area of the electrode depends on channel width (W_c) and on electrode length (L_e). Increasing the active electrode area ($W_c \times L_e$) could decrease the double layer capacitance, thus improving the measurement, but this parameter seems to saturate

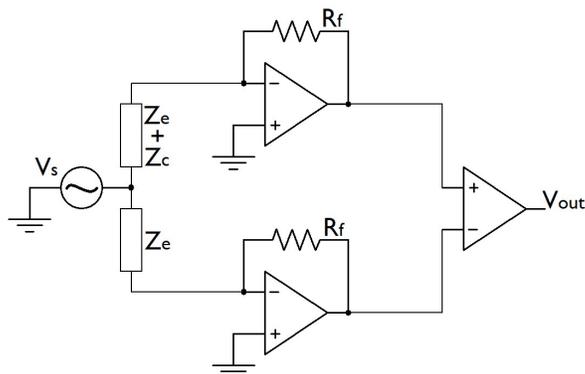


Figure 4.3. Schematic of the proposed readout circuit to sense impedance variation on the IFC electrodes: the central electrode is stimulated with a HF signal (V_s), and the other electrodes are connected to transimpedance amplifiers. The output voltage of the two transimpedance amplifiers go into a differential amplifier. When no cells are passing, the impedance between first and middle electrode and the impedance between middle and last electrode are equal, producing a V_{out} equal to V_{in} , but when a cell is passing, the differential amplifier will detect a change in amplitude and phase with respect to V_s .

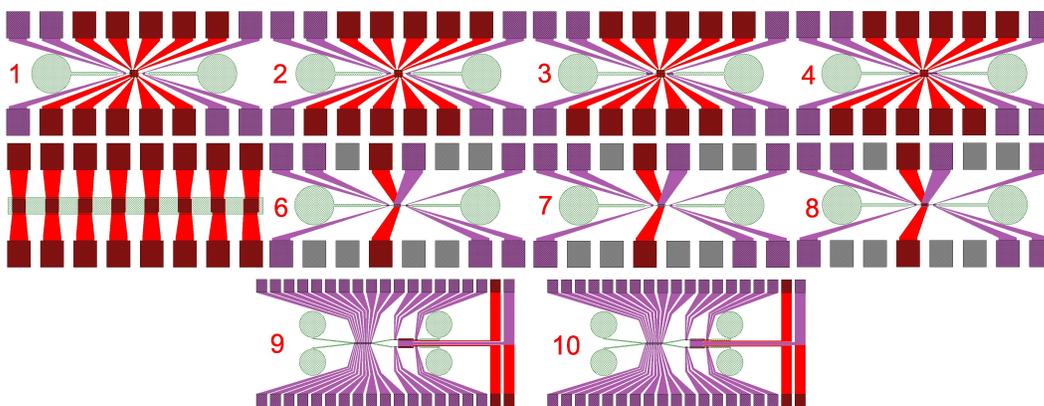


Figure 4.4. Screenshots from the layout editor software (Tanner L-Edit) of the 10 different designs. It is possible to notice the electrodes for IFC (in purple), the electrodes for EIS (in red) and the microfluidic circuit (in green).

after a certain limit. After setting $G_e=10\mu\text{m}$ and $W_c=H_c=10\mu\text{m}$ (optimal for particles with our dimension requirements), the only degree of freedom is L_e . The first 4 designs are therefore created to investigate the effect of this parameter on the SNR: design #1 has $L_e=50\mu\text{m}$, design #2 has $L_e=100\mu\text{m}$, design #3 has $L_e=150\mu\text{m}$ and design #4 has $L_e=200\mu\text{m}$ (Fig. 4.8).

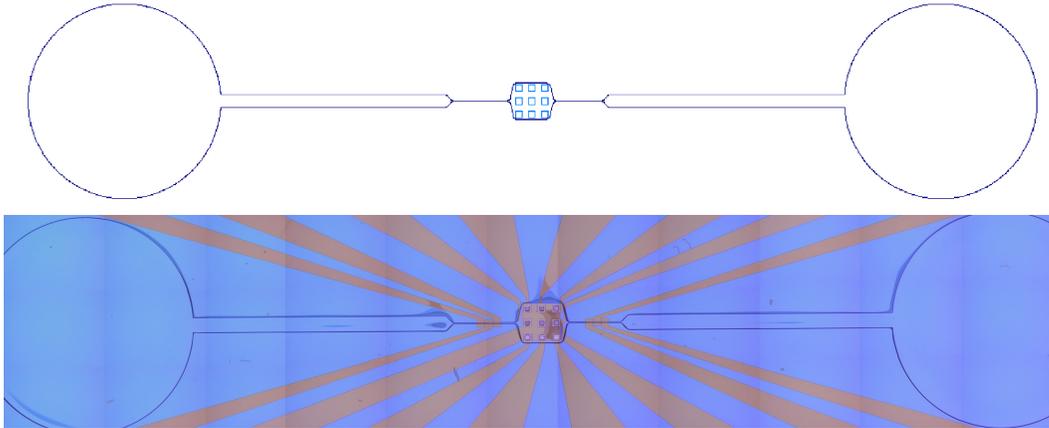


Figure 4.5. Top: screenshot from the layout editor software (Tanner L-Edit) of the microchannel structure, with the central chamber and the 9 wells. Bottom: picture under optical microscope of the actual device after fabrication.

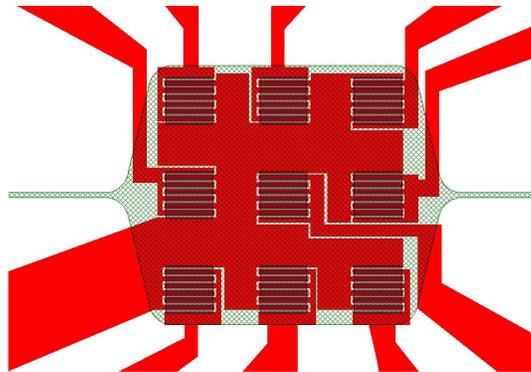


Figure 4.6. Screenshots from the layout editor software (Tanner L-Edit) of a zoom on the central chamber. In red are displayed the EIS electrodes (one ground + 9 IDEs), in green the chamber structure with the $10\mu\text{m}$ channels on the left and on the right.

4.1.2 Design #5

In order to optimize the $\Delta R/R$ during EIS measurements, design #5 was created, to test how the different parameters regarding the microwells could influence the SNR. In [33] Ibrahim et al. suggest a way of optimizing IDEs to perform Electrochemical Bio-Impedance Spectroscopy, varying length (L_e), gap (G_e), width (W_e) and number of the electrodes (a 3D representation of the IDEs with the relevant geometrical parameters is shown in Fig. 4.9). The main parameter to be optimized is the ratio between electrode width and spacing between the electrodes (W_e/G_e) that is optimum at the value of $3/2$. Design #5 therefore aims at finding the best values for

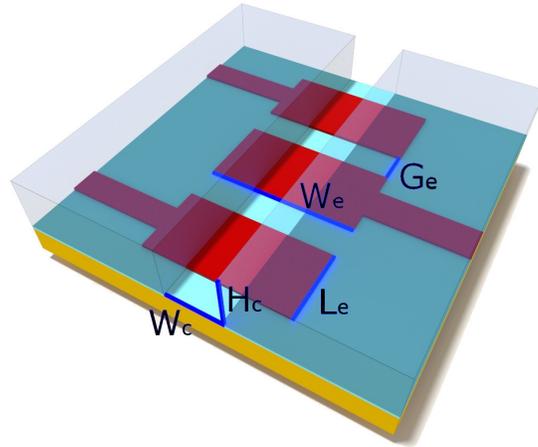


Figure 4.7. 3D drawing of the IFC electrodes below the microchannel, where the design parameters have been highlighted (W_c is channel width, H_c is channel height, L_e is electrode length, W_e is electrode width, G_e is gap between electrodes).

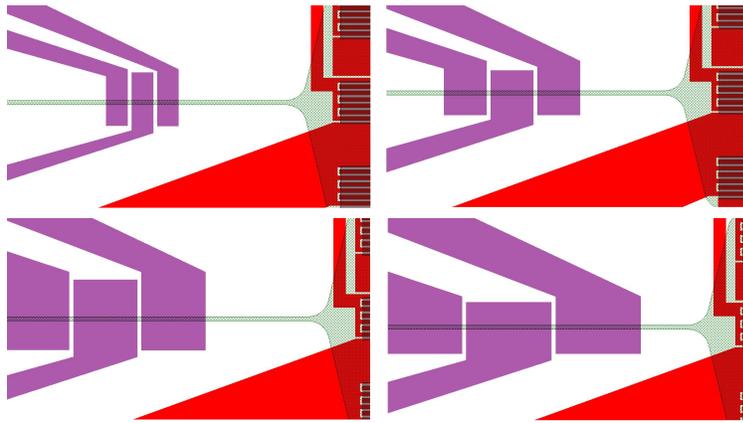


Figure 4.8. Screenshot from the layout editor software (Tanner L-Edit) of the 4 different designs, zoom on the IFC electrodes: it is possible to notice the dimension increase of the electrodes, from $50\mu\text{m}$ to $200\mu\text{m}$.

W_e and G_e , maintaining constant the area of the well ($100\mu\text{m} \times 100\mu\text{m}$) and their depth ($H_w=10\mu\text{m}$). The design consists in a series of 8 microwells of the same size, with IDEs at the bottom, with a progressive increase of W_e and G_e (the list of the chosen values for W_e and G_e is reported in table 4.1). The number of fingers for each IDE becomes a secondary parameter, equal to $\frac{100}{W_e+G_e}$.

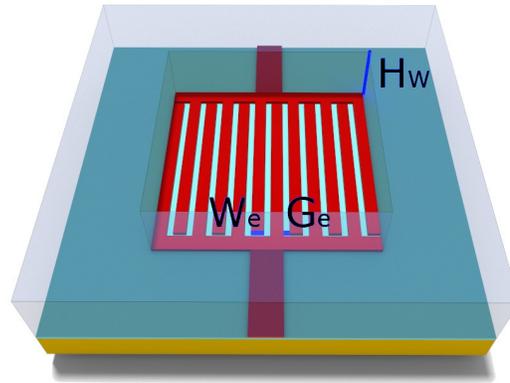


Figure 4.9. 3D drawing of the IDEs inside a microwell, where the design parameters have been highlighted (H_w is microwell height, W_e is electrode width, G_e is gap between electrodes).

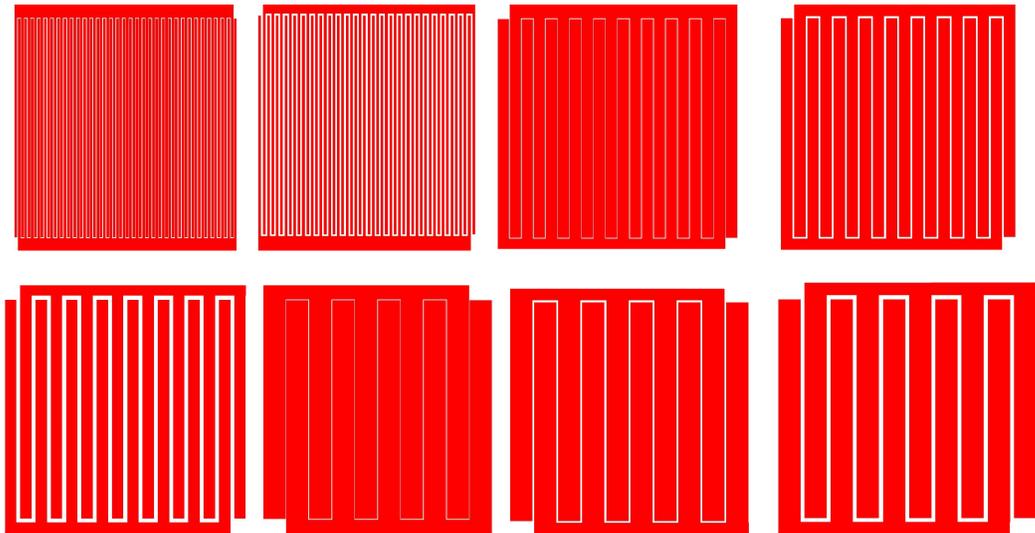


Figure 4.10. Screenshot from the layout editor software (Tanner L-Edit) of the IDEs inside the 8 different wells: W_e increases from $10\mu\text{m}$ to $100\mu\text{m}$, G_e increases from $5\mu\text{m}$ to $20\mu\text{m}$.

4.1.3 Design #6,7 and 8

The devices of designs #1 to #5, even if realized with different parameters, rely only on gravitational force to trap cells inside the wells. In designs from #6 to #8 the concept of Dielectrophoresis (DEP) is investigated, to improve cell trapping inside

Well nr.	1	2	3	4	5	6	7	8
We (μm)	10	10	50	50	50	100	100	100
Ge (μm)	5	10	5	10	20	5	10	20

Table 4.1. List of values for the We and Ge parameters of the microwells in design #5.

the microwells.

Dielectrophoresis is a phenomenon in which dielectric particles are subjected to a force (DEP force) in the presence of non-uniform electric fields: inside the field, dielectric domains (dipoles) of the particle become locally polarized, and even if inside a uniform electric field the attractive forces towards the electrodes generating the field would be balanced, in a non-uniform field they are different, and the particle is pushed towards the regions where the field is bigger [34], [35], i.e. the smaller electrode (see Fig. 4.11).

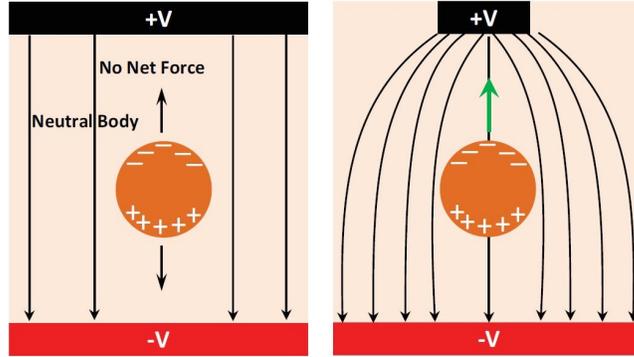


Figure 4.11. Graphical explanation of DEP force: on the left, where the electric field is uniform, the dielectric particle doesn't move, since forces are balanced; on the right, where the electric field is non-uniform, the dielectric particle is subjected to a net force since the attraction of the locally-polarized domains to the smaller electrode is stronger [34].

DEP force is defined as:

$$F_{DEP} = 2\pi\epsilon_0\epsilon_{rs}r^3 Re[f_{CM}]\nabla|E_{rms}|^2$$

where r is the radius of the cell, $\epsilon_0\epsilon_{rs}$ is the permittivity of the solution, E_{rms} is the root-mean-squared value of the non-uniform electric field, $Re[f_{CM}]$ is the real component of the Clausius-Mossotti factor, that is:

$$f_{CM} = \frac{\epsilon_c^* - \epsilon_s^*}{\epsilon_c^* + 2\epsilon_s^*}$$

where ϵ_c^* and ϵ_s^* are complex permittivities of the cell and of the solution, defined as:

$$\epsilon^* = \epsilon + \frac{\sigma}{j\omega}$$

DEP force therefore depends on several parameters, in particular it increases if the radius of the particle to be moved increases (with cubic relation), if the permittivity of the solution increases (linear relation), if the gradient of the electric field increases (quadratic relation).

The real part of Clausius-Mossotti factor is bonded between -0.5 and 1, depending on the ratio between the permittivity of the solution and of the cell, which means that the force could be both positive (pDEP, attracting cells towards areas with stronger electric fields) and negative (nDEP, repelling cells from areas with stronger electric fields). This value depends on frequency, therefore it is important to select the right frequency value to maximize opacity (ratio of $\text{Re}[f_{\text{CM}}]$ at different frequencies). To create a strong attraction, i.e. a strong pDEP ($\text{Re}[f_{\text{CM}}] \rightarrow 1$) is necessary to maximize the ratio $\epsilon_c^*/\epsilon_s^*$, by also selecting a solution with very low permittivity.

Literature presents several exploitations of DEP force to create cell cages, using either positive or negative DEP force, various frequencies, and various electrode geometries, eventually using ITO electrodes on top of the chip to create a vertical force to push cell inside wells, maintaining transparency [36], [37], [38], [39], [40], [41], [42], [43]. The microwells of designs #6 to #8 try to create a non-uniform electric field by exploiting the same fabrication method used to create the other designs (two conductive layers separated by a $10\mu\text{m}$ dielectric), utilizing the IFC electrode layer to create a big top electrode, and the EIS IDEs as the smaller electrode, where E field is stronger, and where it will also be possible to perform measurements on cells. Three different configurations are designed (the EIS electrodes are the same in all three designs, and are IDEs with width= $10\mu\text{m}$ and gap= $5\mu\text{m}$):

- Design #6: a grid of dielectric material is created on top of the IDEs, with square holes of $10\mu\text{m} \times 10\mu\text{m} \times 10\mu\text{m}$, spaced $5\mu\text{m}$, slightly displaced with respect to the IDEs so that the left side of one finger and the right side of the adjacent finger are exposed at the bottom of the hole. On top of the dielectric grid, a layer of conductive material is patterned in order to create the same grid, with matching holes (see Fig. 4.13 for a schematic view of the structure). This top electrode is significantly bigger than the small portions of the bottom electrodes that appear at the bottom of the holes. To validate this idea, i.e. to visualize the areas with stronger electric field, simulations were run on COMSOL Multiphysics (see Fig. 4.12), with promising results;
- Design #7: this time, the grid of dielectric has rectangular holes that have the same length of the bottom IDEs, exposing all the sides of the IDEs (see

Fig. 4.14 for a schematic view of the structure). The top grid is realized in the same way, with the same matching rectangular holes. In this case the ratio between top and bottom electrodes dimensions decreases, in favour of bigger holes (to increase the chances of cell deposition);

- Design #8: this last case is a control structure, where the grid of dielectric material is not deposited, and a single big hole of the dimension of the chamber is created, exposing all the IDEs (see Fig. 4.15 for a schematic view of the structure). The top electrode surrounds the chamber.

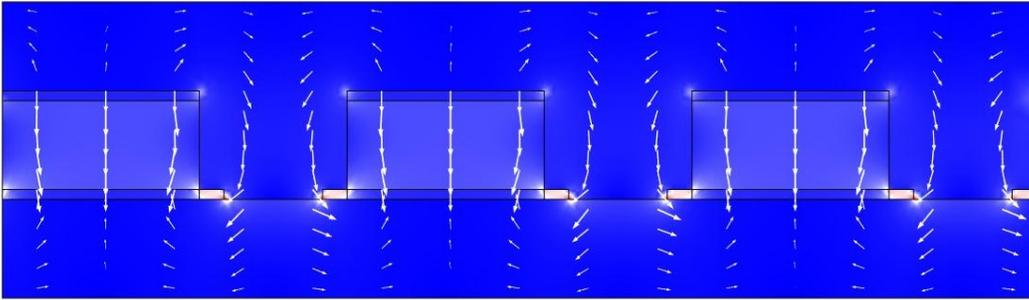


Figure 4.12. Simulation in COMSOL Multiphysics of a grid of walls that covers the middle part and exposes the sides of the bottom electrodes, with an additional metal grid on top of the walls (2D section from microwells of design #6 and #7). An AC voltage of 5Vpp at a frequency of 10kHz was simulated between the top grid and the bottom electrodes. E field is depicted, from 0 (blue) to $5 \cdot 10^5$ V/m (white). DEP is directly proportional to the square of the E field gradient (depicted with white arrows), and this means that cells would be trapped at the bottom of the wells, and in contact with the sides of the bottom electrodes.

4.1.4 Design #9 and 10

In all the designs showed until now, the cells are obliged to go from the only inlet to the only outlet, passing through a middle chamber with IFC electrodes at the entrance and at the exit. There is no way to select in which of the 9 wells the cells would go, since there is no actuation. In design #9 and 10, a sorting mechanism is integrated before a ramification of the microfluidic circuit: cells, on the basis of their dielectric properties, will either go in one well or in the other. The sorter relies on dielectrophoresis force (DEP sorter [34]), and it's a combination of two sorting mechanisms already seen in literature, the first relying on the concept of "liquid electrodes" on the sides of the channel [44], [45], [46] and the second utilizing two parallel and diagonal electrodes at the bottom of the channel [47], [48], [49] (Fig. 4.16). The way in which the sorter works is the following: in one of the inlets, e.g.

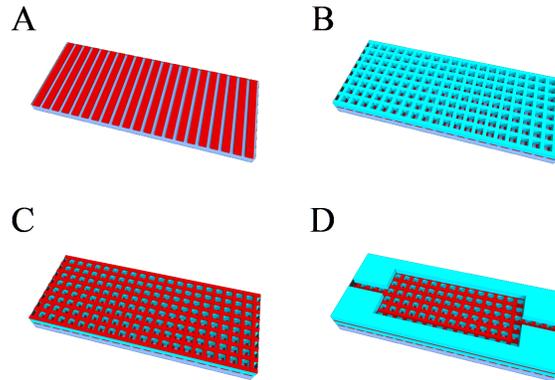


Figure 4.13. 3D representation of a stratified view of the well in design #6. A) IDEs for EIS are patterned on the bottom of the well; B) a $10\mu\text{m}$ structural layer is deposited, leaving square holes to expose the sides of the electrodes; C) the DEP electrode is deposited and patterned on top of the grid-like structural layer, respecting the holes geometry; D) the second $10\mu\text{m}$ structural layer is deposited, creating microchannel and chamber geometries.

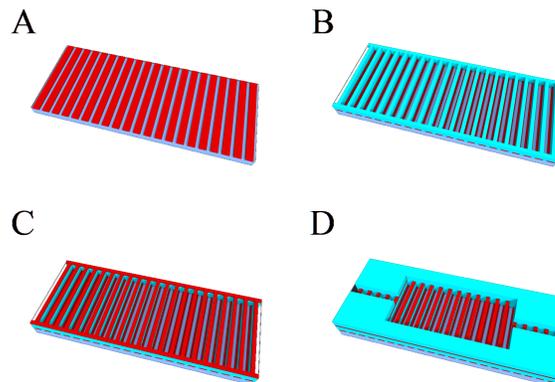


Figure 4.14. 3D representation of a stratified view of the well in design #7. A) IDEs for EIS are patterned on the bottom of the well; B) a $10\mu\text{m}$ structural layer is deposited, leaving rectangular holes to expose the sides of the electrodes; C) the DEP electrode is deposited and patterned on top of the grid-like structural layer, respecting the holes geometry; D) the second $10\mu\text{m}$ structural layer is deposited, creating microchannel and chamber geometries.

the top one, the solution with cells to be sorted is injected, while in the second inlet a sheet solution is injected. Thanks to laminar flow, if the sorter is "off" (not powered), the fluid with cells will remain on the top part of the channel, while sheet fluid will stay on the bottom, separated by the fact that without turbulence

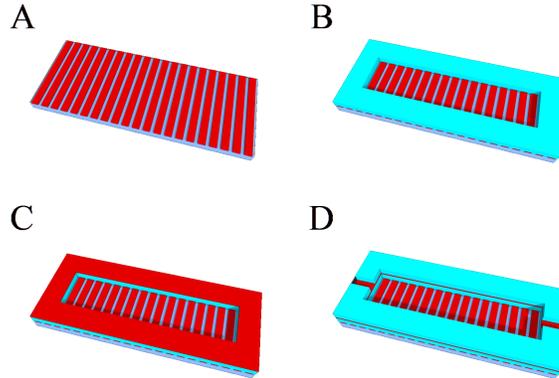


Figure 4.15. 3D representation of a stratified view of the well in design #8. A) IDEs for EIS are patterned on the bottom of the well; B) a $10\mu\text{m}$ structural layer is deposited, leaving a central well to expose the electrodes; C) the DEP electrode is deposited and patterned on top of the structural layer, with an identical hole; D) the second $10\mu\text{m}$ structural layer is deposited, creating microchannel and chamber geometries.

there is no possibility of mixing. In this situation, the top outlet will collect all the cells, and the bottom outlet will collect just sheet fluid. If, instead, the sorter is "on", a dielectrophoretic force will be exerted on cells, pushing them inside the sheet fluid. The "diagonal electrodes" sorter is activated with an AC voltage on the electrodes, that creates a gradient of E field in the middle of the electrodes that attracts cells, while the "liquid electrodes" sorter is activated with the same AC voltage, but applying $V+$ to the even electrodes and $V-$ to the odd electrodes, and works by pushing cells from one side of the channel to the other side (only electrodes on one side have to be activated). For details on the theory behind the working principles of DEP sorters, refer to literature. These two methods act in two complementary way to move cells from the top part of the channel to the bottom part, and if correctly calibrated, they could be able to separate cells on the basis of their dimensions and permittivity (see previous section for details on DEP force). Balancing the permittivity of the medium and the frequency of the applied voltage, it could be possible to move cells on the basis of their radius, keeping smaller cells in the top portion of the channel, and moving bigger cells (since the dependency is cubic) to the other side of the channel, collecting them in the other outlet.

After the sorter, the channel is then split in two parts. Two different chambers will gather the two different populations, studying them separately with both IFC and EIS, and then the two samples are collected via two different outlets (Fig. 4.17). The only difference between design #9 and #10, is that in the former the wells used are similar to what was done for design #7, while in the latter the wells used are

similar to what was done for design #8.

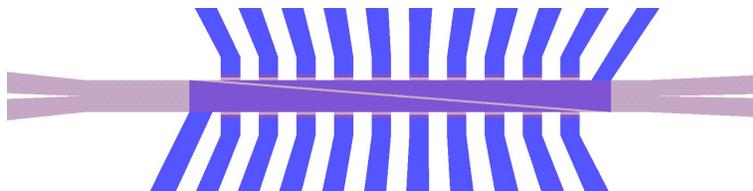


Figure 4.16. Screenshot from the layout editor software (Tanner L-Edit) of the sorter structure, created with two diagonal electrodes at the bottom of the channel and 10 liquid electrodes for each side of the channel

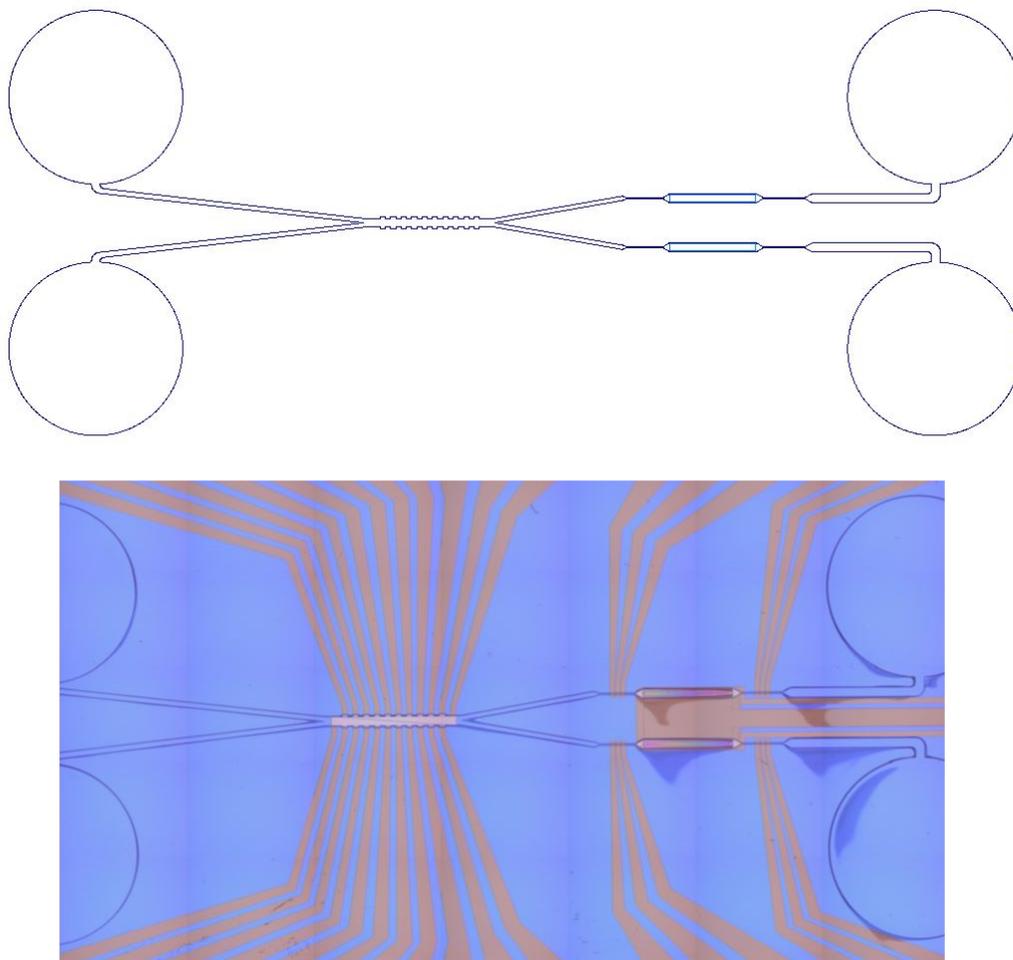


Figure 4.17. Top: screenshot from the layout editor software (Tanner L-Edit) of the microchannel structure, with the 2 inlets and 2 outlets, the sorter and the wells. Bottom: picture under optical microscope of the actual device after fabrication.

4.2 Materials

Several techniques can be used to realize a microfluidic device, e.g. PDMS casting, hot embossing or injection moulding of plastics, soft lithography etc. In this work, the chosen technique was standard Si wafer technology that, although presenting the drawback of being more expensive (because of the need of a cleanroom and several lithographic steps), would give us more freedom on the materials to be used, is very precise ($\sim 0.5\mu\text{m}$ minimum features) and is CMOS compatible, i.e. it would be theoretically possible to realize front-end electronic devices in silicon, and a back-end microfluidic chip on the same platform, with the same flowchart. This decision was taken regardless of the fact that a chip realized on silicon would lose transparency (needed for optical imaging of cells), because the aim of this project is indeed pushing the detection of cells and measuring techniques from the optical state-of-the-art way to a lens-free, label-free imaging based on impedance. The chip was therefore designed as if it was created on top of an already existing detection circuit, in a cleanroom environment and with microfabrication techniques, starting from 4-inch single-polished Si wafers. To simulate the impedance detection mechanism, IDEs are fabricated on the bottom of the microwells, insulated from the bulk Si thanks to a passivation layer. Then the microfluidic chip is realized, with two main structural layers, separated by another round of electrodes, used to perform IFC. This section wants to justify the selection of materials that have been used, highlighting their pros with respect to their alternatives, or the limits that have been found. A detailed view on the fabrication of the chips is given in chapter 5.

4.2.1 Passivation Layer

Since the first layer to be deposited would be a conductor, in order to pattern the first round of electrodes (IDEs for EIS), it is important to insulate those electrodes from the bulk (Si wafer), since its poor but not null conductivity would produce shorts and parasites. The initial idea was to create a silicon dioxide layer, but subsequently this idea has been discarded since also the structural of the device was to be realized in SiO_2 , therefore it was important to create a difference in material that would allow a selective etching. Silicon nitride was selected for this duty, given its high resistance to silicon oxide etching, and easiness of fabrication inside a cleanroom. Thickness of this layer is not important, since just few nm would perfectly insulate the electrodes from the substrate, and it was selected to be 200nm. The chosen deposition method was LPCVD, to obtain a very good conformity of the thin film and to process multiple wafers at the same time.

4.2.2 Electrodes

To choose which material to use as electrodes was driven by three main requisites: 1) high conductivity to reduce the losses; 2) high resistance against corrosion, and high biocompatibility, because the chip would work with the biological media or PBS solutions with $\text{pH} > 7$; 3) easy fabrication and availability in cleanroom, to avoid fabrication problems/delays. The usual and most common electrode material for biosensors is gold, but this first option was immediately discarded because it is not a cleanroom-friendly metal, and it is cause of several contamination problems in IC fabrication (see chapter 5 to have an insight on EKL cleanroom, where the device was fabricated).

A nice candidate to substitute gold was selected to be titanium, that provides a very good conductivity and perfect adhesion with substrates. To improve the biocompatibility and the resistance of the electrodes, they were coated with a layer of titanium nitride (TiN), a conductive ceramic material that has recently become popular to create biosensing electrodes for its incredible resistance to corrosion and biocompatibility [50], [51], [52], [53].

To increase the surface area and therefore increase the performances of the electrodes, it would be ideal making the surface of the electrode porous. It is reported in literature by L. T. Cunha et al in [54] that in order to do so, while depositing TiN through magnetron sputtering, the partial pressure of N_2 must be high, to produce films with a high percentage of nitrogen (see Fig. 4.18). After discussing with cleanroom staff, it resulted impossible to set the sputtering machine (TRIKON SIGMA) to produce such a condition, and the electrodes resulted smooth and sleek, almost mirror-finished. SEM pictures of the electrode surface are shown in Fig. 4.19, where no porosity is visible.

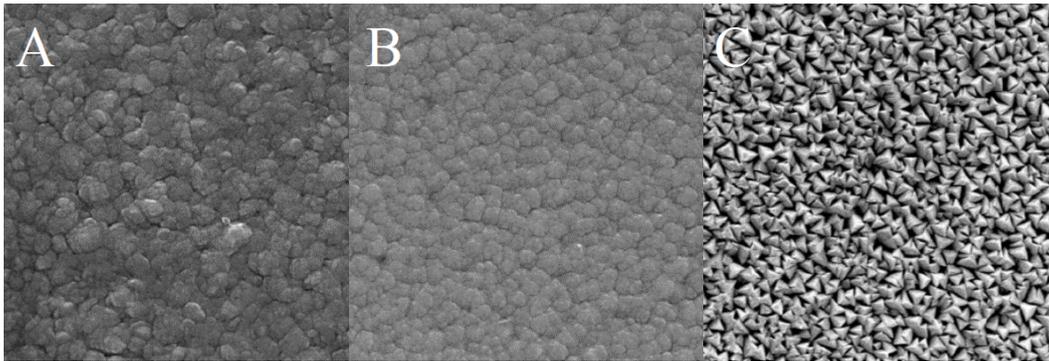


Figure 4.18. SEM pictures of TiN_x samples where the percentage of nitrogen is gradually increased. The letter x indicates the stoichiometry of the film, where for $x < 1$ the film is sub-stoichiometric and it is Ti-rich, while for $x > 1$ the film is over-stoichiometric and it is N-rich. A) sub-stoichiometric film with $x=0.56$; B) stoichiometric film; C) over-stoichiometric film with $x=1.34$ [54].

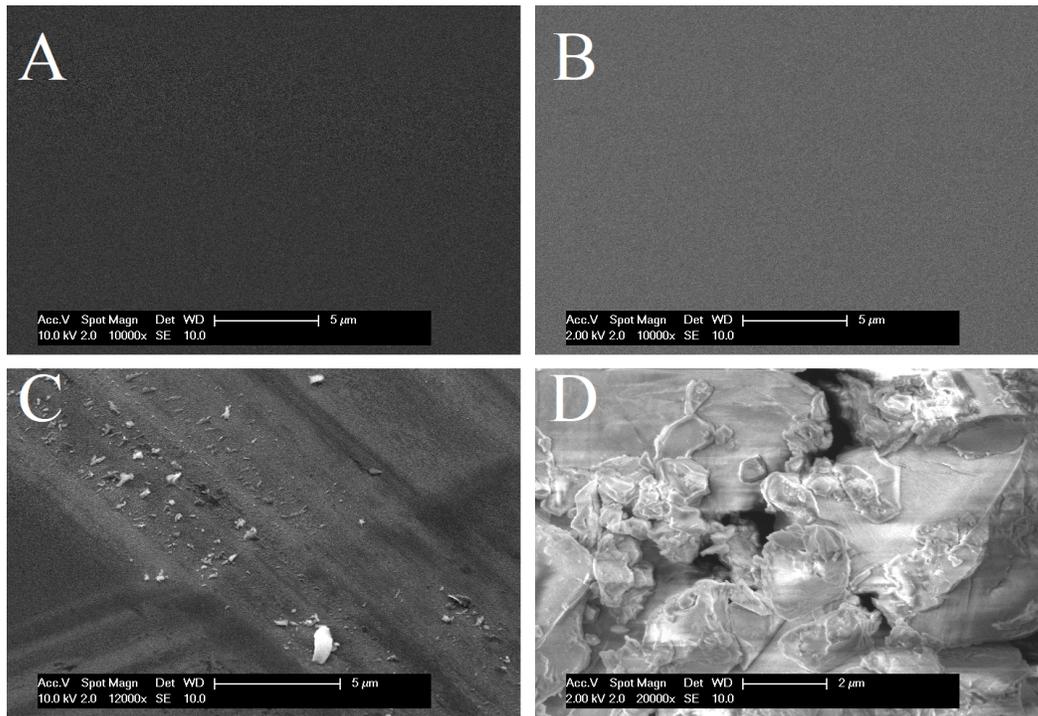


Figure 4.19. Pictures taken with electron microscope showing the perfect smoothness of the obtained TiN film. Different magnifications and different accelerating voltages show the same behaviour of the film, without any sort of porosity. A) clean area of the electrode, at an accelerating voltage of 10kV; B) clean area of the electrode, at an accelerating voltage of 2kV; C) area of the electrode where a scratch has been realized, in order to help focussing, at an accelerating voltage of 10kV, to notice the high resistance of the film, that is barely scratched and still sleek; D) area of the electrode with a scratch, at an accelerating voltage of 2kV (here the scratch was greater, but still the surface of the grains is not porous).

4.2.3 Structural Layers

Initially, the Lab-On-Chip was intended to be realized half in silicon dioxide and half with photosensitive polyimide. SiO_2 would provide mechanical strength to the microwells, and a good substrate layer for the IFC electrodes, then photoresist would have been spun on top of the wafers, and thanks to its self-planarizing property it would have created a sacrificial layer filling the geometries of the microchannels and microwells. The device would have been covered by polyimide, used as structural layer, and finally, the photoresist would have been etched away, leaving already sealed channels. A representation of this initial idea for flowchart is depicted in Fig. 4.20.

Later on, some problems arose, that forced us to make the decision of abandoning polyimide, and both the structural layer of the Lab-On-Chip have been realized in SiO_2 , that however couldn't provide sealing of the microfluidic chip (for the actual fabrication of the device, refer to chapter 5). The reasons why polyimide was discarded are related to problems during fabrication, since finding a way of using photoresist as sacrificial layer, i.e. creating a polyimide structure on top of it and later on removing the photoresist with acetone without damaging the polyimide, was not an easy task, given the long and narrow channel to be released. Moreover, due to a mere organization problem (nobody was working with polyimide since long time), the Fujifilm LTC9520 photosensitive polyimide to be used was expired, and requesting additional material would have been incompatible with the overall planning of the process. Some early results of structures created with polyimide are reported in Fig. from 4.21 to 4.23. Since with this solution the channel is not automatically sealed during fabrication, a different solution to seal it must be found. A series of proposals is given in section 6.3, when dealing with microfluidic interconnections.

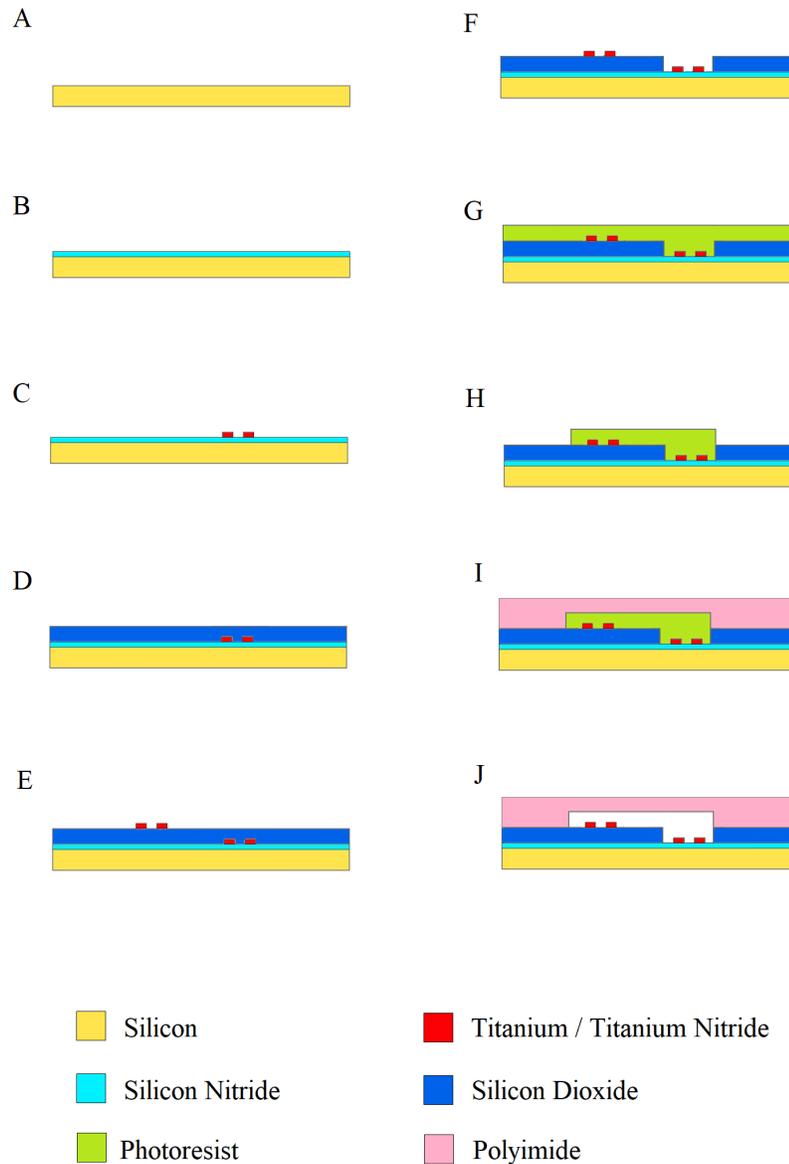


Figure 4.20. Fabrication steps for the realization of the device as it was initially intended, with photoresist as sacrificial layer and polyimide as structural layer. A) The starting material is a single side polished Si wafer; B) a first passivation layer of silicon nitride is deposited, to insulate the substrate; C) the first round of electrodes (the IDEs that will be inside the microwells) is patterned from a layer of titanium/titanium nitride; D) a $10\mu\text{m}$ thick silicon dioxide layer is deposited; E) the second round of electrodes (the flow cytometry electrodes that will be inside the microchannel) is patterned from a layer of titanium/titanium nitride; F) The microwells are opened etching the silicon dioxide; G) a thick ($10\mu\text{m}$) layer of photoresist is spun on top of the wafers, which fills also the microwells; H) the photoresist is lithographically patterned in the shape of the microfluidic circuit; I) polyimide is spun on top of the wafers, covering the photoresist shape; J) the wafers are submerged in acetone, dissolving the photoresist and leaving sealed microchannels made in polyimide.



Figure 4.21. Detail of fabrication problem using polyimide. The wafer was spun with polyimide, soft baked, exposed to UV light (EVG420 contact aligner), X-link baked, developed in HTRD2 and rinsed with RER600, cured in KOYO oven at 350°C for 60 min. Several wafers have been processed in this way, and all presented polyimide detachment problems, either in the developing phase or even after curing. Since other problems arose, that brought to the decision of removing the use of polyimide, causes have not been investigated, but they have to be searched in a too strong developing, weak bakes, or errors in exposure.

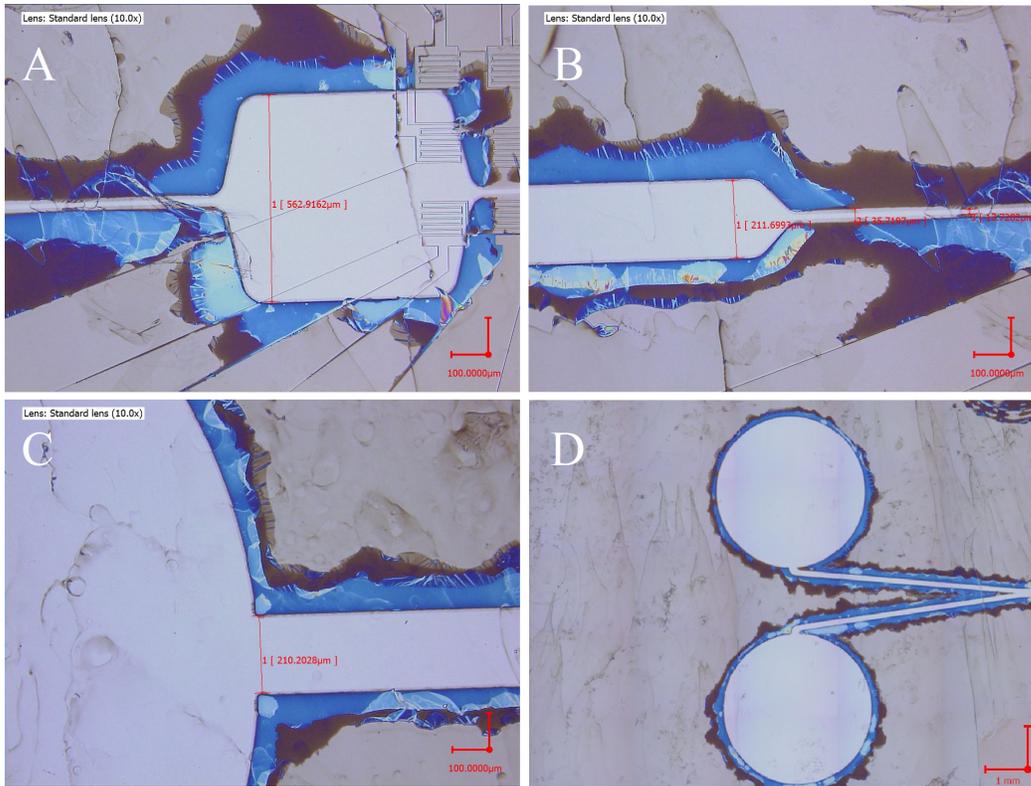


Figure 4.22. Pictures taken at optical microscope of polyimide structures, visibly deteriorated by wrong processing. Dimensions are larger than expected, which underline a too short exposure (since LTC9520 is a negative resist) or a too long development. A) detail of a chamber of design #1 that, beside an alignment problem, is totally ruined; B) detail of the microchannel of design #1, the $10\mu\text{m}$ are not respected; C) detail of the inlet of design #1; D) detail of the inlets of design #9.

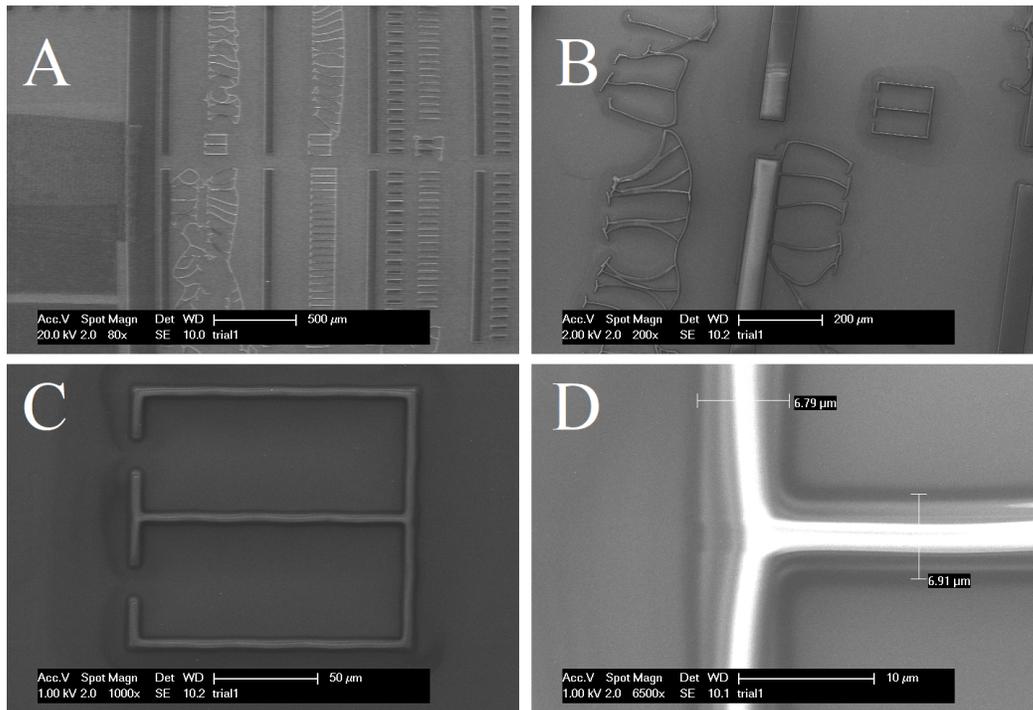


Figure 4.23. SEM micrographs of dummy polyimide structures patterned on Si wafer, to investigate detachment, seen at progressively greater magnifications (A is 80x, B is 200x, C is 1000x, D is 6500x). The ladder-style structures, not only have wrong dimensions (they should be $5\mu\text{m} \times 5\mu\text{m}$), but they detach easily from the substrate and float around the wafer.

4.3 Photomasks

After designing the geometries and choosing the materials to be used for fabrication, the masks can be drawn. The CAD layout software used was TANNER L-Edit from Mentor Graphics (Siemens). In order to realize the device, 4 masks have been designed, starting from a 5 x 5 inch² layout provided by EKL cleanroom. The initial layout provides the outline of the mask, alignment markers, vernier markers, and a 2 x 2 cm² die area (that has been horizontally splitted in half to double the number of dice per wafer) that is repeated 12 times inside the circular outline.

The minimum feature dimension depends strongly on the mask fabrication method, and each manufacturer gives precise specifications regarding precision of the process. The first idea was to fabricate masks with inkjet printing at 50'800 dpi from SELBA S.A. (single polymeric film of 30 x 40 cm², masks are aligned, printed and then the film is cut), that claims a precision of 6 μ m, but then for administrative reasons the chosen manufacturer was COMPUGRAPHICS, that produces masks on 5"x5"x0.09" quartz slides, with chromium as reflecting material. The precision offered is of 1.5 μ m, way better than film masks, but the price is also higher.

Given that, the CAD software was set with a manufacturing grid of 1.5 μ m, and the 10 designs were drawn in 2 x 1 cm² cells. Of the 24 available dice, 3 were used for design #1 to 4, while 2 were used for design #5 to 10, trying to distribute them in different areas of the wafer to increase variability, as shown in Fig 4.24 (if a systematic error occurs always on the same area of the wafer, having distributed designs helps in increasing the yeld).

It is important to always remember the material to be etched, the polarity of the photoresist of the lithography step associated, and the manufacturing options (brightfield/darkfield) when designing a mask, since a mistake at this level would produce the negative of the required mask. This was a problem in our specific case, because the last mask was designed for polyimide (negative polarity), and then the polyimide was removed in favour of silicon dioxide. To solve the problem the flowchart was modified and negative resist (instead of standard SPR 3012) was used.

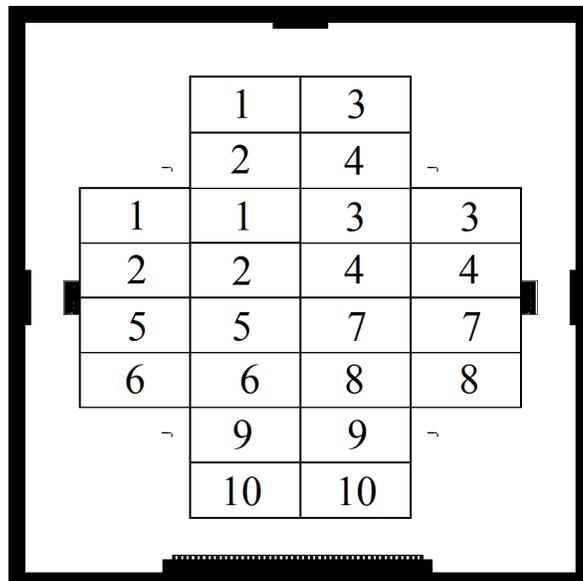


Figure 4.24. Representation of the layout of the 10 different designs on the masks. The small rectangular at the sides are the alignment markers, small dots next to the corners are part of vernier markers.

Chapter 5

Microfabrication

In order to satisfy the precision requirements of the device, and to comply with the need of creating a platform technology able to integrate microfluidics sensing and standard semiconductor technology, the whole fabrication has been carried out in a cleanroom class 100 with a CMOS-compatible process, on 4-inch silicon wafers. The first section of this chapter will deal with the Else Kooi Lab, the in-house cleanroom facility of TU Delft, giving an insight on the rules and instrumentations that have been used to realize the device; the second section will deal with the tests that have been created before starting the fabrication of the device; finally, section 5.3 will describe in details the main nodes of the flowchart, covering the issues that have arisen during the processing. All the flowcharts for the tests can be found in Appendix A, altogether with the last version of the main flowchart.

5.1 Else Kooi Lab Cleanroom



Figure 5.1. Else Kooi Lab logo

The Else Kooi Lab (formerly known as Dimes Technology Centre and now named

after Else Kooi, dutch chemist and inventor of LOCOS), is a cleanroom facility specialized in IC production, photonic devices, flexible electronics and MEMS technology. It comprises class 100 (ISO 5) and class 10'000 (ISO 7) areas, with dedicated sections for MEMS fabrication, special applications, bonding and packaging, measurements. The facility is hosted by TU Delft, and alongside its personal trained staff, it can count on the collaboration of university research groups, first of all the Electronic Components, Technology and Materials (ECTM) group. Not only senior researchers but also TU Delft master and PhD students can participate actively to the fabrication phase of a project, after getting the necessary training on the machinery and on the rules of the cleanroom. A brief description of the available machines is here provided, followed by a short insight of the do's and don'ts.

5.1.1 Equipment

EKL is divided in 3 main areas: class 100, class 10'000, and MEMS lab. Except for some of the post-processing tools, all the machines have the necessity to work with 4-inch wafers, and being production oriented there is usually the possibility to load standard 25-wafer carriers. The following is a non-exhaustive list of machines and technology that it is possible to use:

- High temperature furnaces: dry and wet oxidation, annealing, diffusion, LPCVD, nitrogen oven for curing;
- Plasma technology: RIE/DRIE of metals, polymers, ceramics and oxides, PECVD, plasma treatments with oxygen;
- Wet benches and fume hoods: chemicals for wet etching of metals and oxides, cleaning lines, polymer technology;
- Lithography: spinners and hotplates, automatic coating/developing station, contact aligner and wafer stepper;
- Measurements: optical, laser and electron microscopes, profilometer, ellipsometer, contact angle, stress-meter;
- Bonding and packaging: dicing saw, wire and wedge bonders, foil system, pick and place;
- Other: magnetron sputtering PVD, ALD, epitaxy, graphene CVD, wafer bonder, and much more.

5.1.2 Rules of Behaviour

Being exposed to dangerous materials and big machines, that usually work with gas pipes, under strong vacuum levels and/or with high voltages, it is of the foremost importance to know how to work inside a cleanroom, to not generate any health issue for yourself and for others. Moreover, maintaining cleaning levels so high requires an enormous effort, and it is mandatory to avoid any behaviour that could possibly damage other's work by contaminating the cleanroom. First of all, it is necessary for everybody who wants to work inside EKL to follow a safety course, which also comprises of a cleanroom tour to learn the gowning procedure and to locate the position of all the emergency exits, fire extinguishers, emergency buttons, diphoterine/hexafluorine kits. Then, the training on the machinery could begin, which lasts one week or more, on the basis of the particular needs of the trainee. At the end of the training, the user is allowed to autonomously process its wafer inside the cleanroom, and a mentor (a more experienced user) is assigned to him in order to help him in the creation of the first flowchart. If additional training is needed, the user can always request for it through a web portal, and the teaching staff will organize training sessions.

Some of the rules to be always respected are: the use of working glasses whenever dealing with chemicals (especially during wet etching with HF and cleaning with high temperature HNO_3); buddy system, i.e. at least one person must know what you are doing, checking regularly that no hazards happened, every time you work on a wet bench or you are working outside the 8:00-18:00 shift; distinction between "green metals" (that are considered to be less dangerous in IC manufacturing, e.g. titanium, aluminium, molybdenum) and "red metals" (very dangerous for IC manufacturing, e.g. gold, copper, nickel), with the requirement that every wafer that carries red metals should be considered "contaminated", and should be processed differently (different baths, different chucks and carriers, avoid use of some machines); always having an approved flowchart prior to entering the cleanroom (a flowchart that has been checked by cleanroom staff and marked with a Run Number).

5.2 Tests and Trials

The particular precision required to fabricate micro/nano devices is particularly prone to errors, especially when the processes aren't planned with care. Even the simplest step of the flowchart could create problems on the final device if its output is uncontrolled, since the variability of microfabrication processes depends on a huge number of parameters, which must be analysed in advance and managed with care. After coming up with a flowchart for the realization of a device, many additional tests arise, each one of them requiring its own flowchart. EKL policy is to mark

these flowcharts with a "P Number", i.e. an equivalent of the Run Number used in a "real" flowchart. Prior to the complete run of the actual flowchart, all the tests should be performed, whose outcomes will have relevance for the main flowchart (that will therefore be modified accordingly).

This section is to list and explain the tests that have been created to investigate critical steps of the main flowchart. The related P flowcharts are attached in Appendix A, together with the main flowchart. A number of minor tests have been performed on dummy wafers, without the need of a P flowchart, and are not listed here. Since the choice of materials and processes for the realization of the device changed halfway, some of the tests became unnecessary and have not been performed. They are reported here for the sake of completeness, but without conclusion.

5.2.1 Uncured Polyimide Interaction with Acetone

Initially, the device was intended to be fabricated not only with silicon dioxide, but also with polyimide. The choice was driven by the idea of having a self planarizing material able to cover a sacrificial layer of photoresist, that would be subsequently etched by acetone, leaving a polyimide structure with an internal cavity (the channel of the device). The idea was soon discarded for two reasons: the unexpected slowness of dealing with polymers in EKL, which threatened the success of the project, and the high (although not verified) probability that the dimensions of the etching apertures would have been not enough to completely etch the photoresist, leaving the channel clogged and the device unusable. This test was designed to study the behaviour of polyimide when put in contact with acetone *before* being cured: the polyimide is insoluble in acetone if cured, but curing at high temperature would cause the photoresist to burn, decreasing its solubility in acetone and clogging the channel. Just a trial has been performed before changing the flowchart to avoid the use of photoresist, which showed that a $5\mu\text{m}$ layer of polyimide, exposed to a 1 min proximity soft bake at 115°C (conditions at which the photoresist would have been subjected) is still strongly attached by acetone, being not enough cured (Fig. 5.2).

5.2.2 Polyimide Interaction with Positive Photoresist

This test was created to further investigate the interactions between a sacrificial layer made of Photoresist (SPR 3012 by MicroChem) and a structural layer made of polyimide (LTC 9520 by Fujifilm). The process theoretically involved the deposition and patterning of a thick layer of positive resist, to define the channel geometry, which had to be covered by a thick layer of polyimide, used as a lid and patterned to create the inlet/outlet and the opening pads for the electrodes. Then the photoresist

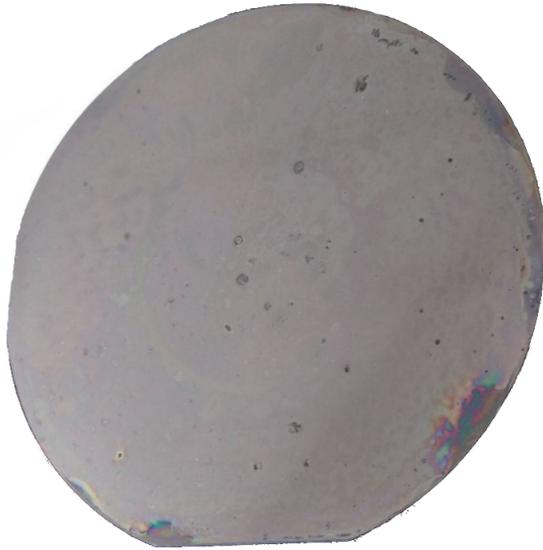


Figure 5.2. Uncured polyimide after acetone bath. It is possible to see how the polyimide almost completely got dissolved in the acetone

inside the channel would be etched with acetone. The steps of the test are shown in Fig. 5.3. Because of the change in the flowchart, this test has not been performed.

5.2.3 Thick PECVD Oxide Stress Measurement

Depositing thick layers of silicon dioxide with PECVD could sometimes be problematic since the temperature involved is definitely lower with respect to standard CVD. This could create layers that have a noticeably higher level of stress (in case of silicon dioxide the stress is compressive). The deposited layer must be stress-free to avoid bending, or even breaking the wafer, since a bended wafer is not recognised by machines, and cannot be processed anymore. A stressed layer could also generate microfractures, interfering with the adhesion of the following layers and with the sealing of the device. Measuring the stress of a wafer before and after a long deposition let us investigate the properties of the thick ($10\mu\text{m}$) oxide film used in our device. The deposition of silicon dioxide has been performed with a NOVELLUS CONCEPT 1 with silane (SiH_4) and nitrous oxide (N_2O) as precursor gases, at a temperature of 400°C , while the stress measurements have been performed with a Tencor Flexus 2320 laser stress meter. Table 5.1 summarizes the results: the Radius of Curvature of the wafer, i.e. the radius of the hypothetical sphere which best approximates the curvature of the wafer, significantly decreases, and the Bow (difference in height between border and centre of the wafer) increases. Nevertheless,

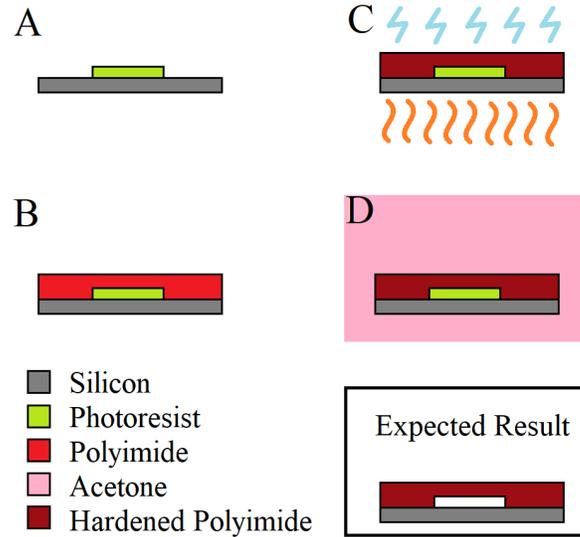


Figure 5.3. Steps of the test supposed to investigate polyimide/photoresist interaction. A) a pattern of positive photoresist is created on top of a silicon wafer with standard photolithographic techniques; B) the wafer is covered with polyimide; C) a variable combination of UV light, heat and time is applied to the wafer; D) the wafer is suberged in acetone. When the combination of parameters applied could produce a polyimide structure resistant enough to withstand the acetone bath needed to dissolve the photoresist, without hardening the photoresist too much, then the test could be considered concluded.

the extracted values have been presented to EKL technicians, which compared them with limit values, and stated that no problem would arise in further processing the wafer.

	Si wafer	Si wafer + 10 μ m SiO ₂
Radius of Curvature (m)	450	103
Bow(μm)	-2.42	-8.23

Table 5.1. Stress measurements before/after the deposition of 10 μ m SiO₂

5.2.4 Etching of Titanium Nitride in BHF Bath

The decision of Titanium/Titanium Nitride as the electrode material was taken for three main reason: the high conductivity of the titanium core, the high resistance against corrosion and biocompatibility of the titanium nitride shell, and the EKL cleanroom availability of both, to avoid annoying slowdowns in production. Initially, the flowchart contemplated the use of a wet etchant (BHF, a mixture of hydrofluoric

acid in a buffering agent) to etch the last part of the silicon dioxide, as the selectivity of HF in etching silicon dioxide and titanium nitride is supposed to be different and the use of a RIE machine could damage the electrodes underneath. To test this selectivity a test flowchart was created, in order to investigate the etching rate of a titanium nitride film inside BHF, since the only data available regarding titanium nitride in BHF stated that *"40nm of titanium nitride deposited at 50°C has been tested in BHF 1:7. After 5 minutes no attack of the layer was observed. Layers deposited at 350°C (standard) are expected to have better quality. Effects of longer exposure to BHF 1:7 are not known"*. Eventually, the BHF was abandoned in favour of the use of a two-steps recipe of the RIE machine (DRYTEK TRIODE 384T with C₂F₆ and CHF₃ gases, first step 300W, second step 100W) that solved the problem anyway, without the risk of the typical underetch of wet etching.

5.2.5 RIE Selectivity of Titanium Nitride over Silicon Nitride

Titanium nitride and silicon nitride are two hard ceramic materials, with different electrical properties. Titanium nitride is conductive, while silicon nitride is an insulator. In our process, silicon nitride was used to passivate the bulk Si wafer and avoid shorts between electrodes, and the titanium nitride is used in combination with titanium in order to obtain electrodes which have good conductivity, excellent biocompatibility and resistance to corrosion. During the etching of the titanium nitride, the silicon nitride underneath could be damaged, since the recipe used by the RIE machine to etch titanium nitride could also damage silicon nitride, leading to shorts. This test was performed to understand how fast the silicon nitride is etched with that recipe, which was intended for titanium nitride, to avoid overetching of the silicon nitride protection layer during the "real" process. The test was performed depositing 300nm of silicon nitride with LPCVD on a silicon wafer, and measuring the layer before and after the etching recipe. The measuring equipment was a LEITZ MPV-SP laser microscope, able to measure silicon nitride on top of silicon because of their different diffraction index. The etching machine was a TRIKON OMEGA 201, recipe with HBr and Cl₂ intended to etch 300nm of titanium nitride (80s bulk etch + 25s overetch). The actual thickness of the deposited layer of silicon nitride before etching was measured to be 267nm ± 0.5nm. After the etch, we could notice that the thickness of the silicon nitride decreased significantly, and that the etch rate of the machine is greater in the centre and lower near the borders of the wafer (Fig. 5.4). The result of this experiment showed that the etch rate of silicon nitride, that is calculated to be approx. 150 nm/min at the centre and 120 nm/min at the border, is not so much lower with respect to the etch rate of titanium nitride (180-200 nm/min), with an estimated selectivity of 2:3. For this reason, and for the

reason that the etch rate is not constant on the surface of the wafer, the recipe was manually shortened, to be sure to avoid the overetch of silicon nitride.

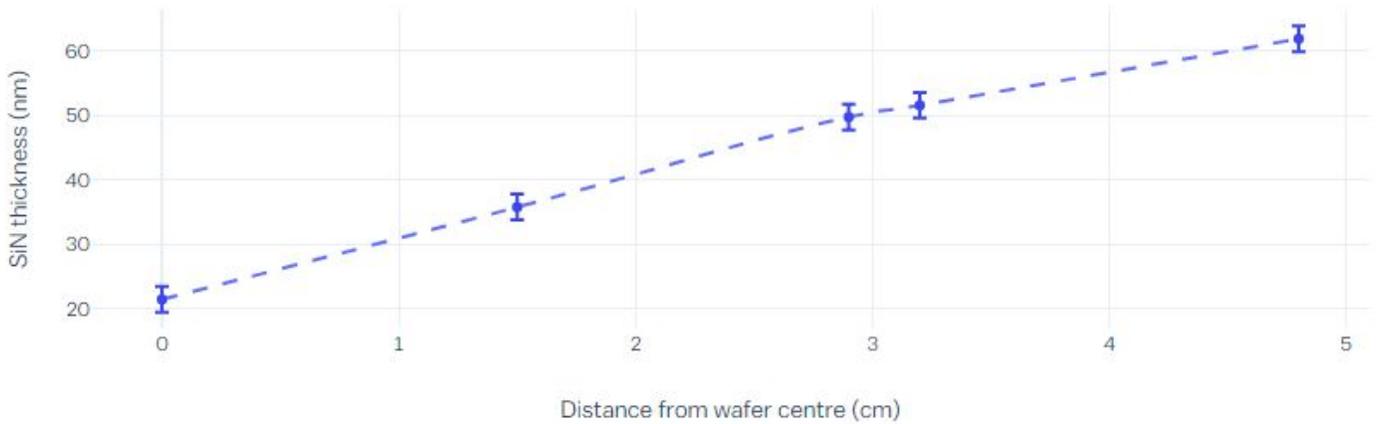


Figure 5.4. Graph showing the resulting thickness of silicon nitride after the etching step, with respect to the distance from the centre of the wafer

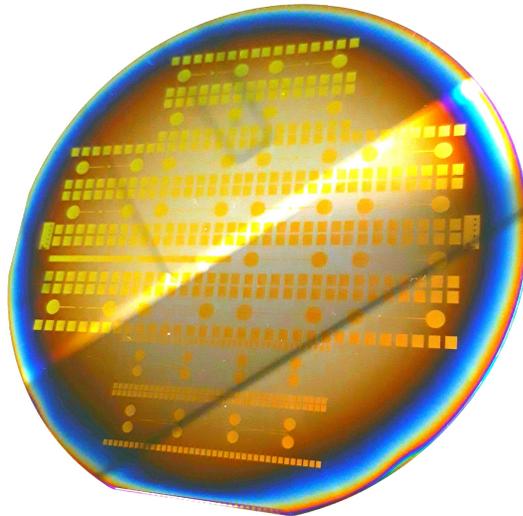


Figure 5.5. Wafer used to test RIE etching of silicon nitride. Gold-coloured circular and squared patterns are control areas where photoresist protected the etch of the silicon nitride, and where the thickness wasn't altered. To be noticed the changing colour of the etched silicon nitride, caused by the different thickness of the layer, already a mark of the different etching rate between the centre and the borders.

5.3 Workflow

In this section the flowchart used for the realization of the device (which can be found in Appendix A) is explained step by step. Initially, the flowchart contemplated the use of polyimide to create a cover for the Lab-on-Chip, but after the choice of abandoning the use of polymers (mainly driven by timing issues) the flowchart have been changed. In its final version, the structural layers for both the wells and the channel are realized with PECVD silicon dioxide, as further explained in this section. Fig. 5.6 shows the fabrication steps to obtain a double depth, multi electrode device, without the need of using polymers to create the structural layers.

5.3.1 Bulk Passivation

Before realizing the electrodes at the bottom of the device (the ones that will be placed inside the microwells), it is important to insulate the substrate, since the cristaline silicon of which wafers are made is conductive and can create shorts between the electrodes. This is done by covering with a thin (approx. 200nm) layer of silicon nitride the whole wafer, by LPCVD at 700°C for about 30 min. Wafers, after the deposition, will turn their colour from the typical grey of the Si to a more gold/brownish one (depending on the thickness of the layer the colour could tend to blue, yellow or green). To obtain informations about the thickness of the layer, a LEICA laser microscope that is able to measure thin films thickness by measuring the refracted light at the interface between two materials. In this case the measurement shown that the silicon nitride thickness was around 197pm0.5nm. This is the "step 0" of the process, and shouldn't be considered as part of the fabrication since it became necessary just because of our choice of starting material (Si wafers), and would have been avoided using another substrate (e.g. SiO₂ covered wafers or glass wafers). This is also the only non-CMOS compatible step of the flowchart, since the temperature goes above the diffusion temperature of doped regions and the melting temperature of the metal lines, but again, it won't be included in a flowchart where the initial material is already insulating.

5.3.2 Microwell Electrodes

The first real step of the fabrication consists in depositing the metal layer and patterning it in order to create the interdigitated electrodes for the EIS. This is done in three main steps: 1) sputtering of the metal layer; 2) photolithography to define areas to be etched; 3) reactive ion etching of the unwanted metal.

The first step was performed with a TRIKON SIGMA magnetron sputtering machine, at 350°C with a two-phase process: in the first phase the titanium target is sputtered in an argon (inert) atmosphere for about 25 sec, to create a 40nm

layer of titanium, while in the second phase the titanium target is sputtered in a nitrogen atmosphere for nearly 5 min, creating a 200nm layer of titanium nitride because of the chemical interaction between the sputtered atoms of Ti and the low pressure N₂ gas. The correct way to utilize the machine is therefore to first clean the target (which could still be dirty of titanium nitride/oxide from the previous user) with a fake deposition on a dummy wafer, then to perform the two-phase recipe, and eventually clean the target again with another dummy wafer to prepare the machine for the next process wafer. This means that every process wafer must be preceded by a dummy wafer, thus increasing the time of this step by the double.

The second step, i.e. the photolithography, was done in a yellow room (to avoid unwanted exposures) with two semi-automated machines: the first one is an EVG120 automatic coater/developer, and consists of a robotic arm routinely placing wafers either on top of a spinner (where peristaltic pumps dispense the photoresist/developer) or inside a series of hotplates, the second one is an EVG420 contact aligner, where the photoresist is exposed through UV light. In this step first the wafers were inserted in the EVG120 to be coated with 1.4 μ m of SPR 3012 positive photoresist and soft baked at 115°C for 90 sec, then they were exposed with the appropriate mask under the light of the contact aligner for 7 sec (lamp intensity of 15mW/cm²) at a distance of 40 μ m, and then again inserted into the EVG120 for a post-exposure bake, a standard 90sec development with alkaline solution and a hard bake. The whole process is performed to obtain a patterned photoresist layer on top of the metal layer, to protect it from the next step.

Finally, the unwanted metal can be etched, patterning the electrodes in an interdigitated fashion (IDE). The procedure was performed in a TRIKON OMEGA 201 reactive ion etching machine, using a recipe with HBr and Cl₂ intended to etch titanium nitride but suitable also for pure Ti. As shown by the tests, this recipe is also able to etch silicon nitride, and the endpoint detection doesn't work at the interface between titanium/titanium nitride and silicon nitride, so it had to be manually stopped after 1 min 30 sec to avoid overetch of the silicon nitride passivation layer. The masking photoresist was removed with a TEPLA 300 plasma stripper (O₂ gas at a plasma power of 1kW). To measure the thickness of the electrodes a double measurement was used: first, a DEKTAK 150 profilometer was used to manually measure the step between the unetched and etched regions, and then the LEICA laser microscope was used to refine the profilometer measurement (in case some of the silicon nitride was etched). The measurement shown the expected thickness of 238 \pm 5nm

5.3.3 First Structural Layer

After electrode patterning, a thick intermediate layer of silicon dioxide was deposited on top of the wafers, which in the final steps of the process will be opened in

correspondence of the IDEs and of the contact pads. This layer was deposited with a NOVELLUS CONCEPT 1 plasma enhanced CVD machine, using a recipe with silane (SiH_4) and nitrous oxide (N_2O) as precursor gases, at a temperature of 400°C . A PECVD technique was chosen because it allows the fast deposition of thick layers of oxides, at low temperature, with a reasonable quality. The deposition time was first calculated on the basis of the most recent SiO_2 deposition (since the machine has a logbook where it is necessary to record the performance of each deposition), then tested on a dummy wafer. The deposition rate for silicon oxide, with a gas pressure of 2200 mT and a high frequency power of 1kW has been found to be slightly higher than $350\text{nm}/\text{min}$, which made the time needed to deposit $10\mu\text{m}$ approx. 28 min. Fig. 5.7 shows a wafer after the first electrodes and the subsequent oxide deposition. As it is possible to notice, the whole wafer changes colour after the process, losing the characteristic yellow-gold finish and becoming greyish, due to the SiO_2 layer. Unfortunately, the measurement of this layer couldn't be performed directly with the LEICA, given that there was no possibility of measuring silicon dioxide on top of silicon nitride or titanium nitride, but the measurement has been performed on a dummy wafer which have been inserted in the same batch and processed at the same time inside the machine, revealing a thickness of $\sim 9800\text{nm}$.

5.3.4 Microchannel Electrodes

After the oxide deposition, another metallization step was performed, in order to create a second electrode layer $10\mu\text{m}$ above the first layer. The steps followed are identical to the ones already mentioned in section 5.3.2, using the correct mask for the lithography step, and are not reported here. Fig. 5.8 and 5.9 are a collection of pictures taken with an optical microscope equipped with CCD camera, showing the results of the two lithographic steps needed to realize the electrodes. The difference in colours for the electrodes is caused by a different diffraction of the light under the intermediate layer of silicon oxide, and because top electrodes are still covered by photoresist (brownish electrodes are the microwell electrodes and are imaged below the $10\mu\text{m}$ of oxide, pink electrodes are the microchannel electrodes and are exposed).

5.3.5 Second Structural Layer

To insulate the microchannel electrodes, another layer of $10\mu\text{m}$ is deposited on top of the wafers, that will be subsequently etched to expose them, and to create the microfluidic channel geometry. Since the same method of section 5.3.3 has been followed, it is not reported here. The result of this step produces wafers that again have changed colour, from grey to blue/purple, because of the different thickness of the overall deposited layer (approx. $20\mu\text{m}$ of silicon dioxide), and with no exposed electrodes/pads. In this case the indirect measurement revealed a silicon oxide layer

of $\sim 9750\text{nm}$, making the total thickness of $\sim 19'550\text{nm}$. The next and last step is to reach the electrodes and the contact pads by means of a reactive ion etching technique, to give anisotropy to the walls of the microfluidic device.

5.3.6 Electrode Openings

The final step for the fabrication of the device, before going in the MEMS lab for the dicing of the individual chips, is to etch the unwanted SiO_2 to open the contact pads and expose the electrodes, and to create the geometries for the microchannel/microwells. To etch the $\sim 19'550\text{nm}$ of silicon dioxide, at two different depths, we performed a lithographic step twice, with two different masks, the first to etch the channel geometries for the first $\sim 9750\text{nm}$, reaching the flow cytometry electrodes and their pads, and the second to etch the remaining $\sim 9800\text{nm}$ inside the wells. These two lithographic steps were performed similarly to section 5.3.2, but with an important difference: in this case the thickness of the photoresist spun by the EVG120 was selected to be $3.1\mu\text{m}$ instead of $1.4\mu\text{m}$, in order to withstand a longer etching. Given the greater thickness of the photoresist, also the exposure was to be longer, to increase the energy dose, and the exposure time was increased from 7sec to 20sec. The post-exposure bake was then performed manually on a hot plate for 60sec at 115°C in contact mode, and the development is unvaried. The two etching steps were performed in a DRYTEK TRIODE 384T reactive ion etching machine, with a recipe using C_2F_6 and CHF_3 gases (180mT of pressure), in a "soft landing" modality, meaning that it consists of two parts: the first part at an RF power of 300W, for a faster etching rate of $\sim 600\text{nm}/\text{min}$, and the second part at an RF power of 100W, that etches at a slower speed of $\sim 200\text{nm}/\text{min}$ and tries to be less aggressive with the electrodes on the substrate. The variable parameters for part #1 and part #2, for both the etching steps, can be found in table 5.2. The choice of time is done to use the first part as a bulk etch, to etch the most of the silicon dioxide, and the second part as a softer and slower etch, to remove the last micron of oxide and to slightly overetch, since even the thinnest layer of oxide on top of the electrodes would cause a drop of the sensitivity. To avoid a too strong overetch, the second part of the recipe was always performed in multiple steps, for 4 minutes first and then checking the electrodes under a microscope and with a multimeter to see if all the oxide was gone, and if this was not the case (Fig. 5.10) the wafers would go again in the DRYTEK for another etching (same recipe with part #1 lasting 0 min and part #2 lasting 1 min). When the first etch produced exposed electrodes and pads, the photoresist was stripped (TEPLA oxygen plasma at 1000W for 3 minutes) and the second lithography was performed, with the other mask, repeating the same procedure for the etch, until the microwell electrodes were exposed. Then again the photoresist was stripped and the wafers were ready to be diced in single chips. Fig. 5.11 and 5.12 show the results of the two etching steps under the optical microscope,

while 5.13 and 5.14 are taken with a SEM (PHILIPS XL 50 Field Emission Gun SEM). A important thing to be highlighted: since initially the top structural layer (microchannel) was intended to be realized with photosensitive polyimide (negative resist), the last mask has been designed inverted. This imposed us to use a negative resist for the first etching. No other changes were made.

		Power (W)	Etch Rate (nm/min)	Time (min)	Total Etch (nm)
First Etch	Part #1	300	~600	14	~8400
	Part #2	100	~200	8	~1600
					~10'000
Second Etch	Part #1	300	~600	14	~8400
	Part #2	100	~200	9	~1800
					~10'200

Table 5.2. Collection of parameters for the two etching steps to be performed on the DRYTEK reactive ion etcher.

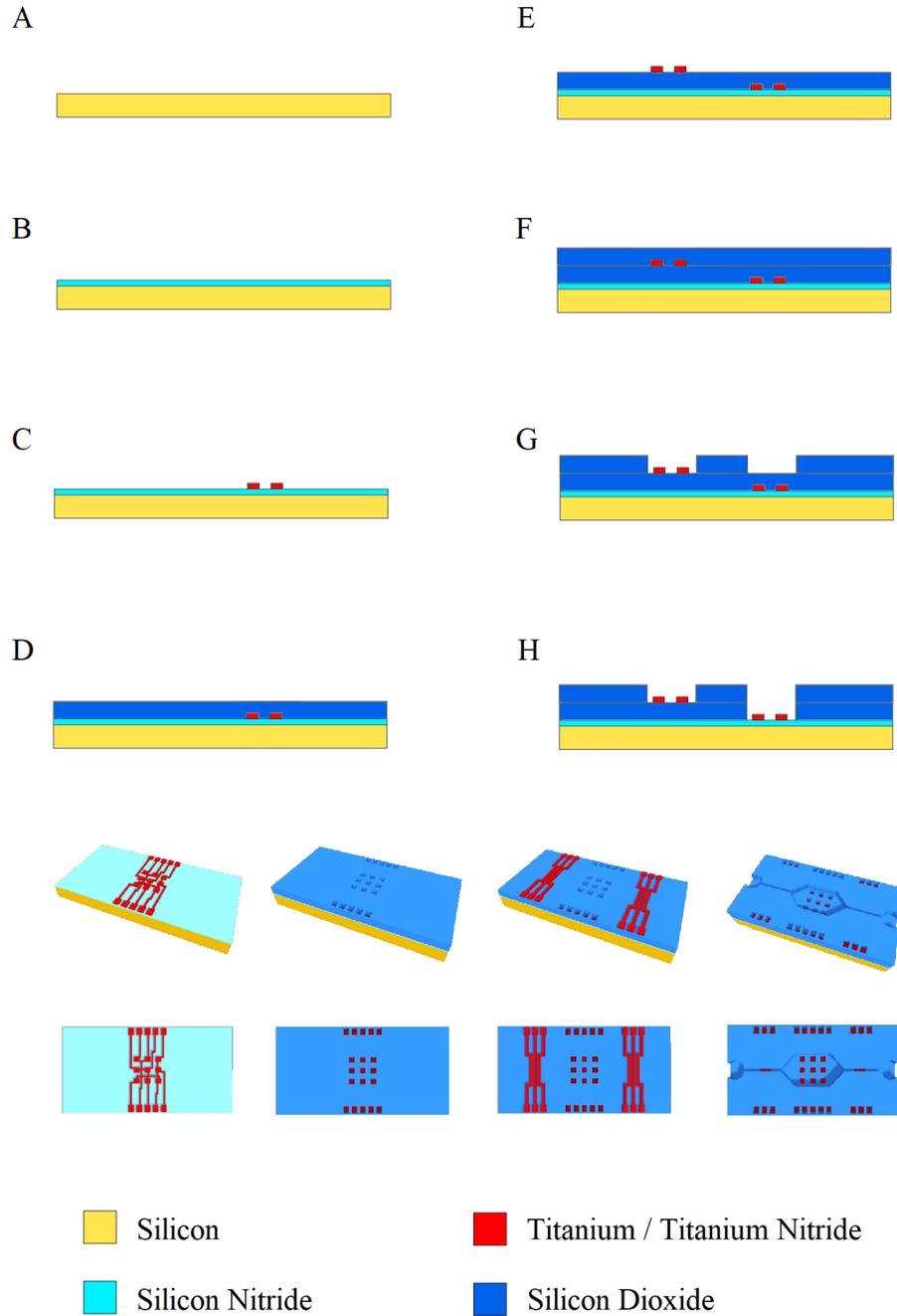


Figure 5.6. Fabrication steps for the realization of the device. A) The starting material is a single side polished Si wafer; B) a first passivation layer of silicon nitride is deposited, to insulate the substrate; C) the first round of electrodes (the IDEs that will be inside the microwells) is patterned from a layer of titanium/titanium nitride; D) a $10\mu\text{m}$ thick silicon dioxide layer is deposited; E) the second round of electrodes (the flow cytometry electrodes that will be inside the microchannel) is patterned from a layer of titanium/titanium nitride; F) another $10\mu\text{m}$ thick silicon dioxide layer is deposited; G) a first etching step is performed, to expose the microchannel electrodes and their pads; H) a second etching step is performed, to expose the microwell electrodes and their pads. On the bottom: 3D representation of the 4 layers that make up the chip

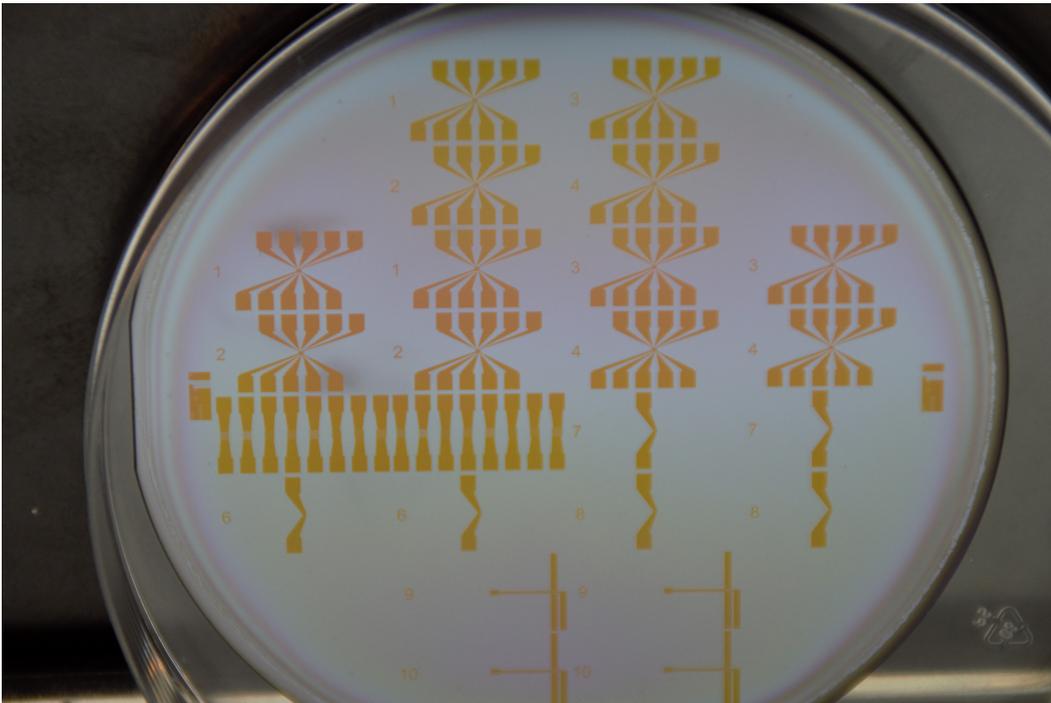


Figure 5.7. Wafer after the first two steps of the process, i.e. the metal deposition/patterning and the oxide deposition.

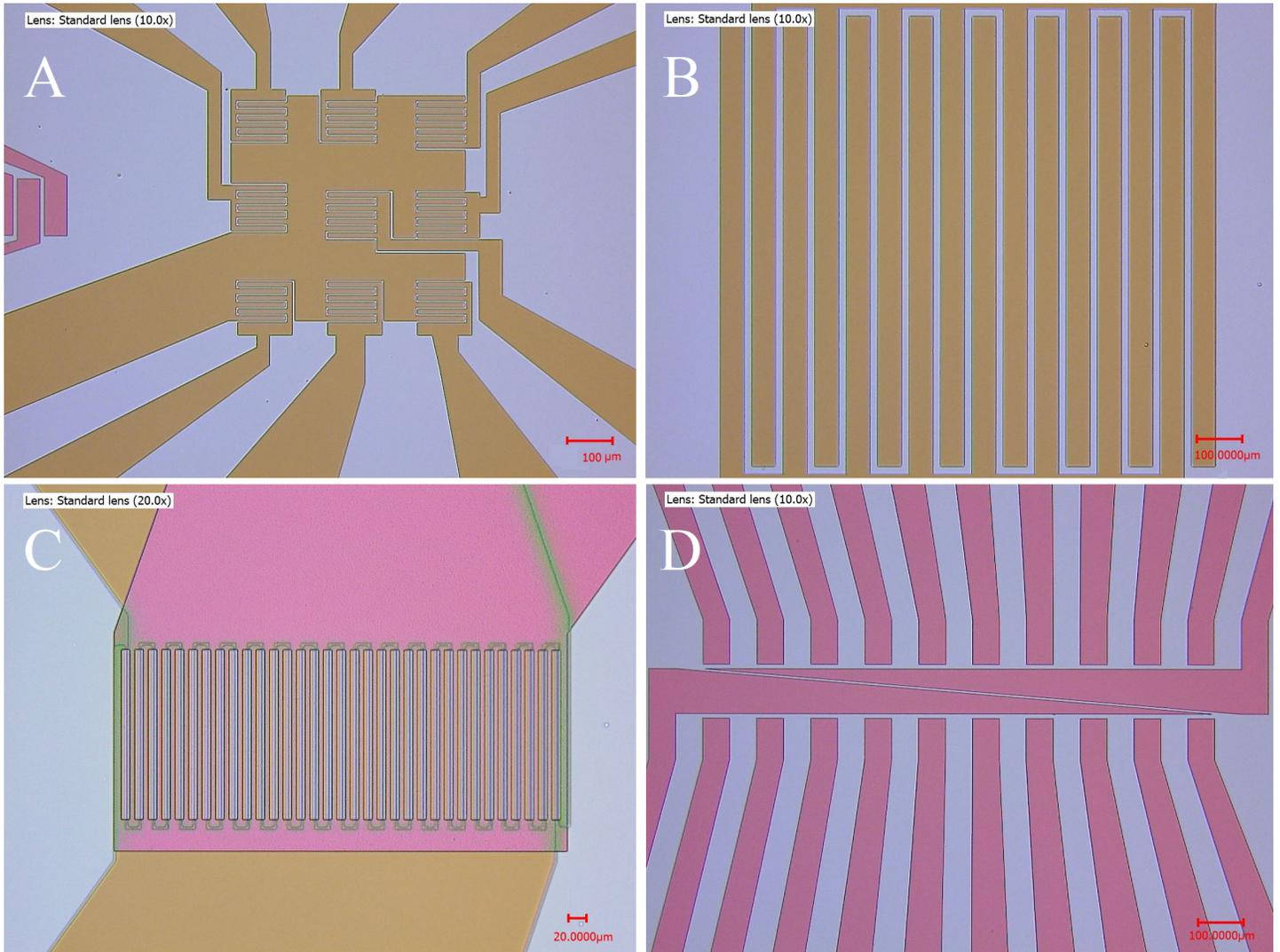


Figure 5.8. Pictures taken with optical microscope of the two rounds of electrodes, separated by $10\mu\text{m}$ of silicon oxide. A) Design #1, zoom on central electrode structure (IDEs + common ground) and part of left-side flow cytometry electrodes; B) design #5, zoom on one of the test IDE structure; C) design #7, zoom on the central microwell structure, with the brown bottom IDEs and the pink top DEP electrode; D) design #9, zoom on the DEP sorter structure.

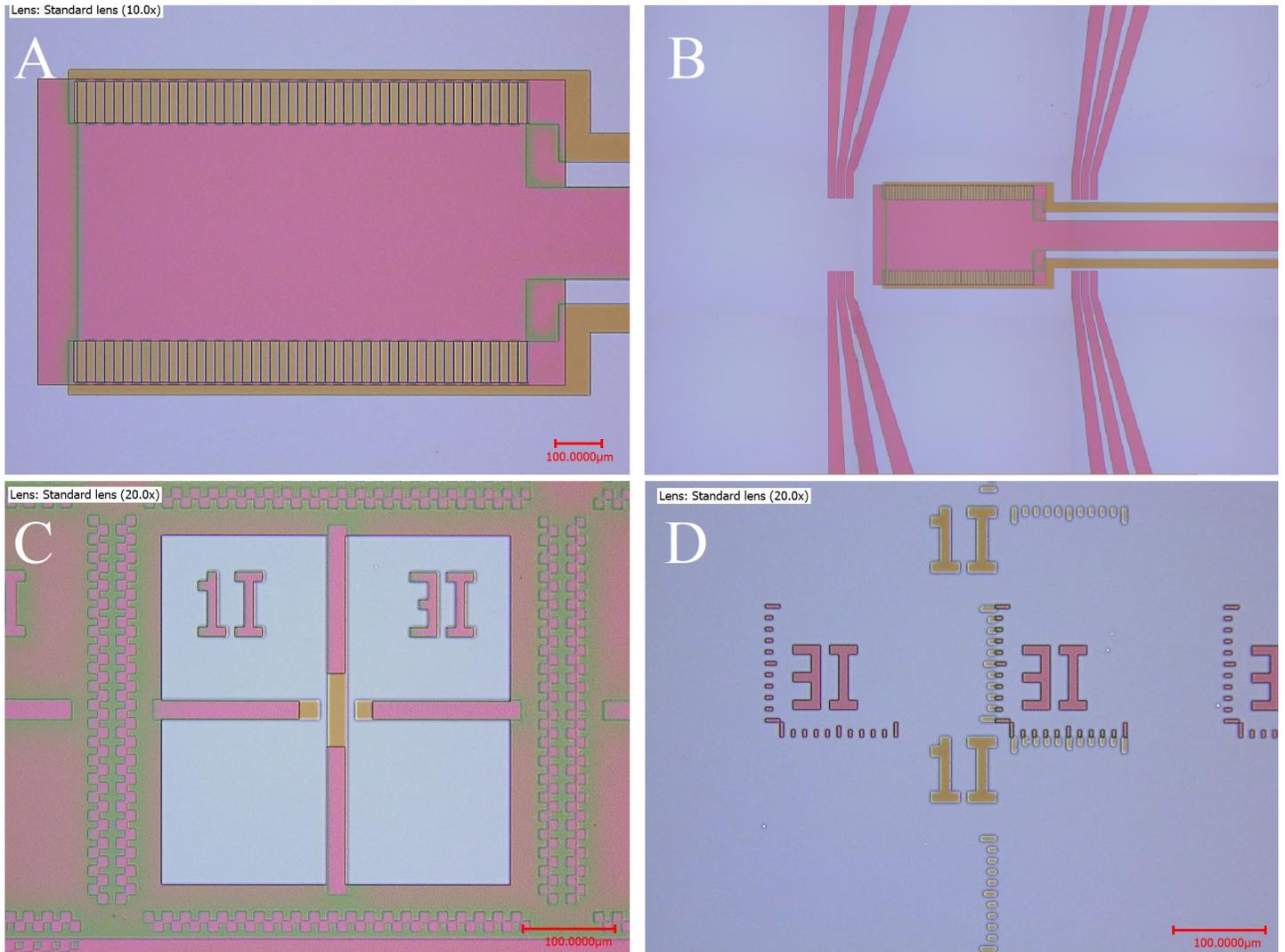


Figure 5.9. Pictures taken with optical microscope of the two rounds of electrodes, separated by $10\mu\text{m}$ of silicon oxide. A) Design #9, zoom on the two microwell structures, each one with IDE structure but with the same common ground, hidden by the pink top DEP electrode; B) design #9, zoom out on the whole microwell structure, with flow cytometry electrodes for both microwells; C) detail of alignment markers between mask FIRSELECTRODES and mask SECONDELECTRODES, it is possible to notice a slight misalignment; D) detail of vernier markers used to quantify x and y displacement in alignment (in this case it is -40nm on x-axis).

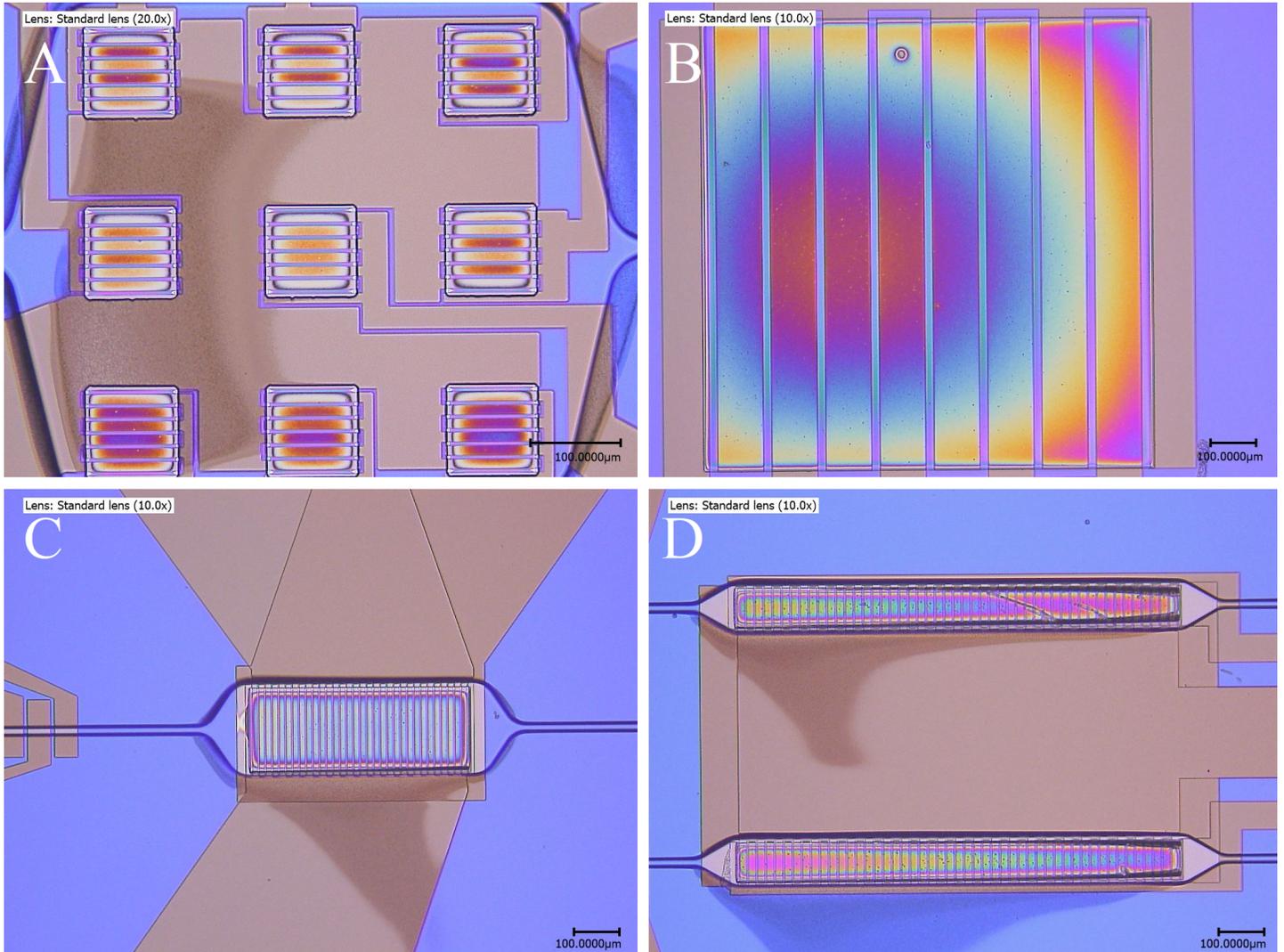


Figure 5.10. Examples of not completely etched structures. The wafer would go again inside the RIE machine for another minute of soft land etching. A) design #4, detail of the central chamber, none of the 9 wells has been etched completely; B) design #5, zoom on the IDEs, the rainbow-like colours are caused by a thin layer of silicon dioxide of different thickness, since the etching rate is stronger in the middle of the well, it shows us that the etching is not complete; C) design #8, zoom on the well, the etch is almost complete but the borders of are still to be etched; D) design #9, zoom on the two wells, clearly still to be etched.

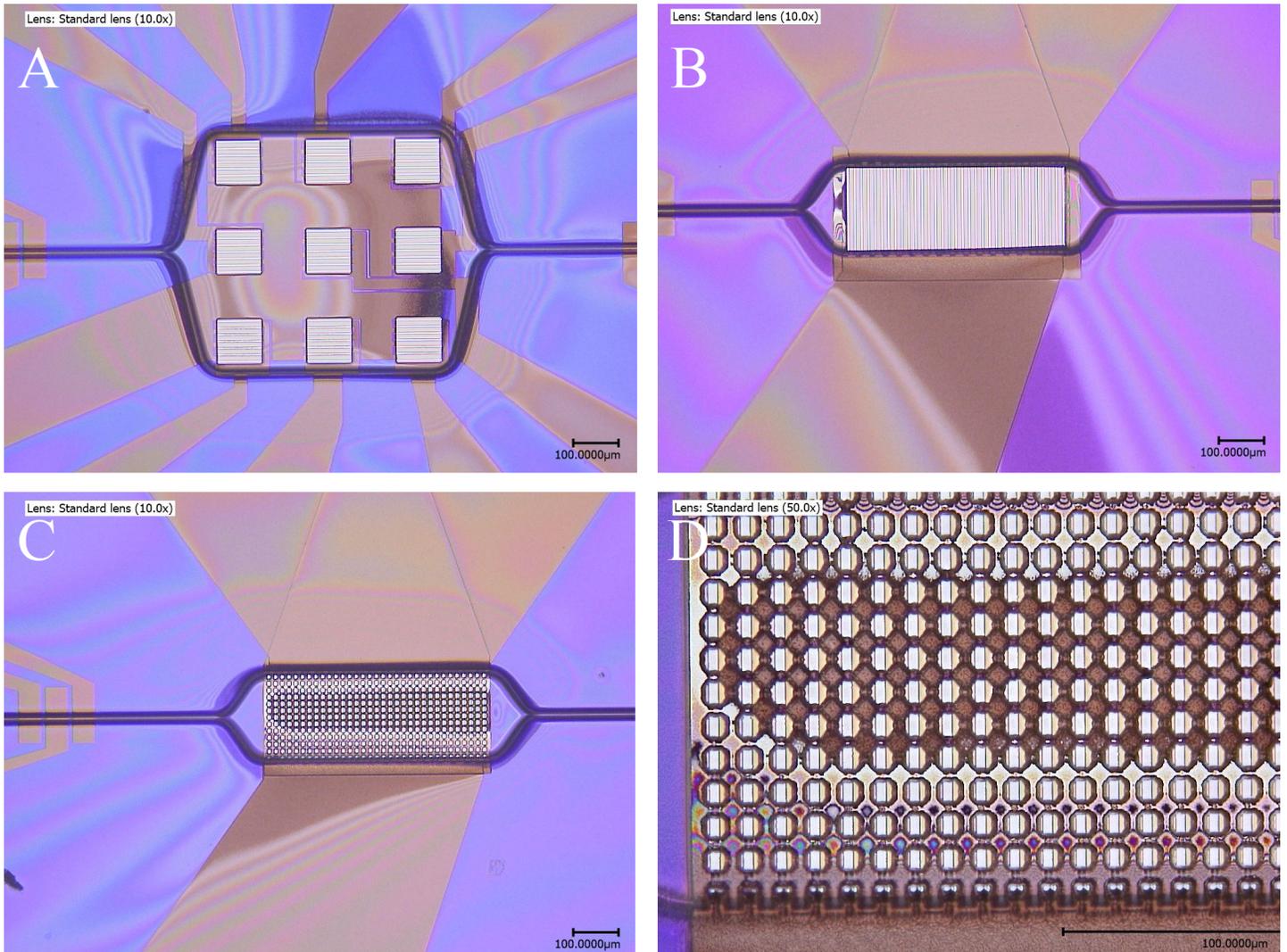


Figure 5.11. Pictures of the final devices under optical microscope. A) design #1, central chamber with the 9 wells, with perfectly exposed electrodes; B) design #8, chamber with completely etched well; C) and D) design #6, chamber with singularly etched square wells.

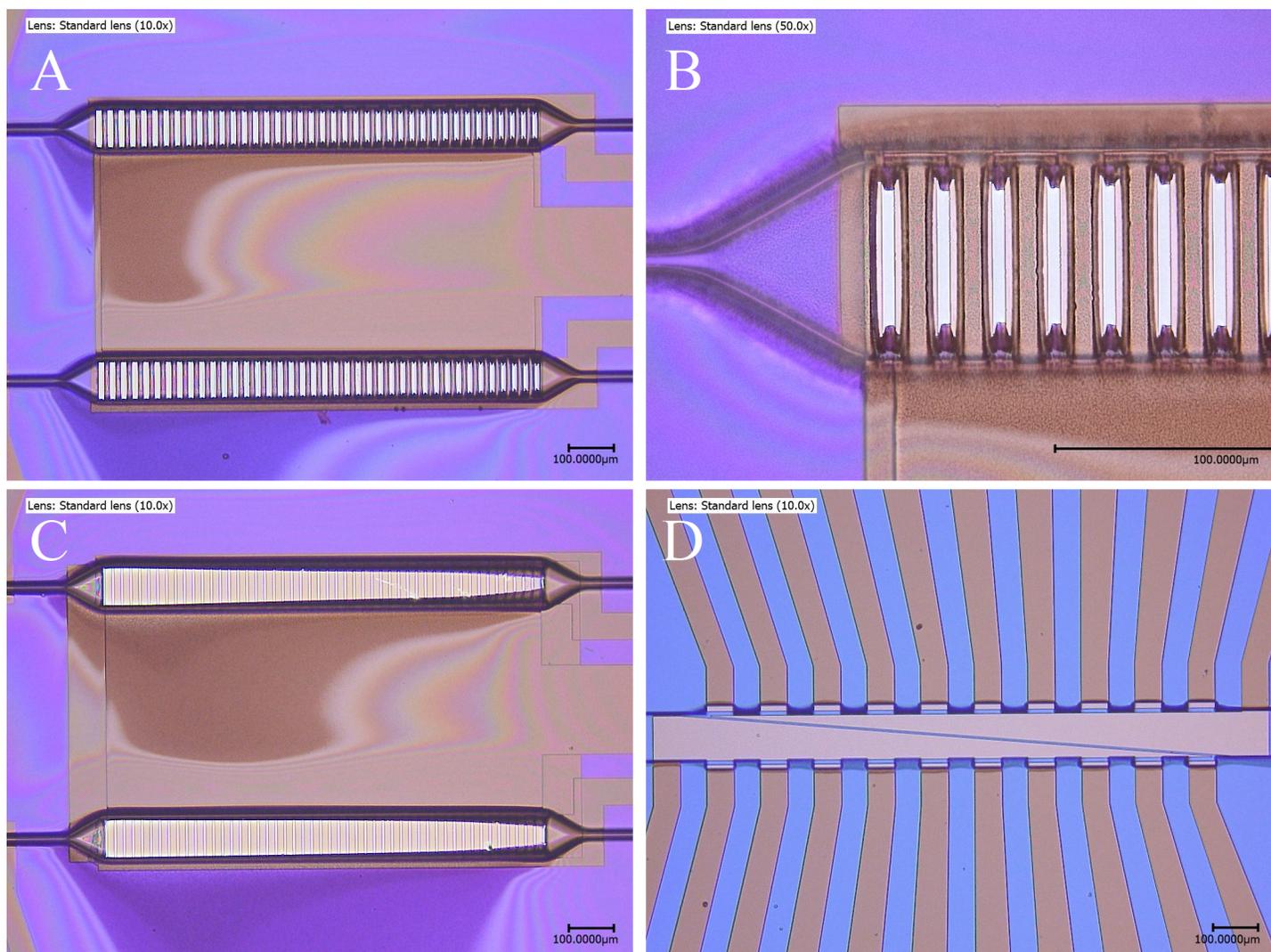


Figure 5.12. Pictures of the final devices under optical microscope. A) and B) design #10, rectangular wells etched inside the two chambers; C) design #9, chambers with etched well; D) dielectrophoretic sorter with "liquid electrodes".

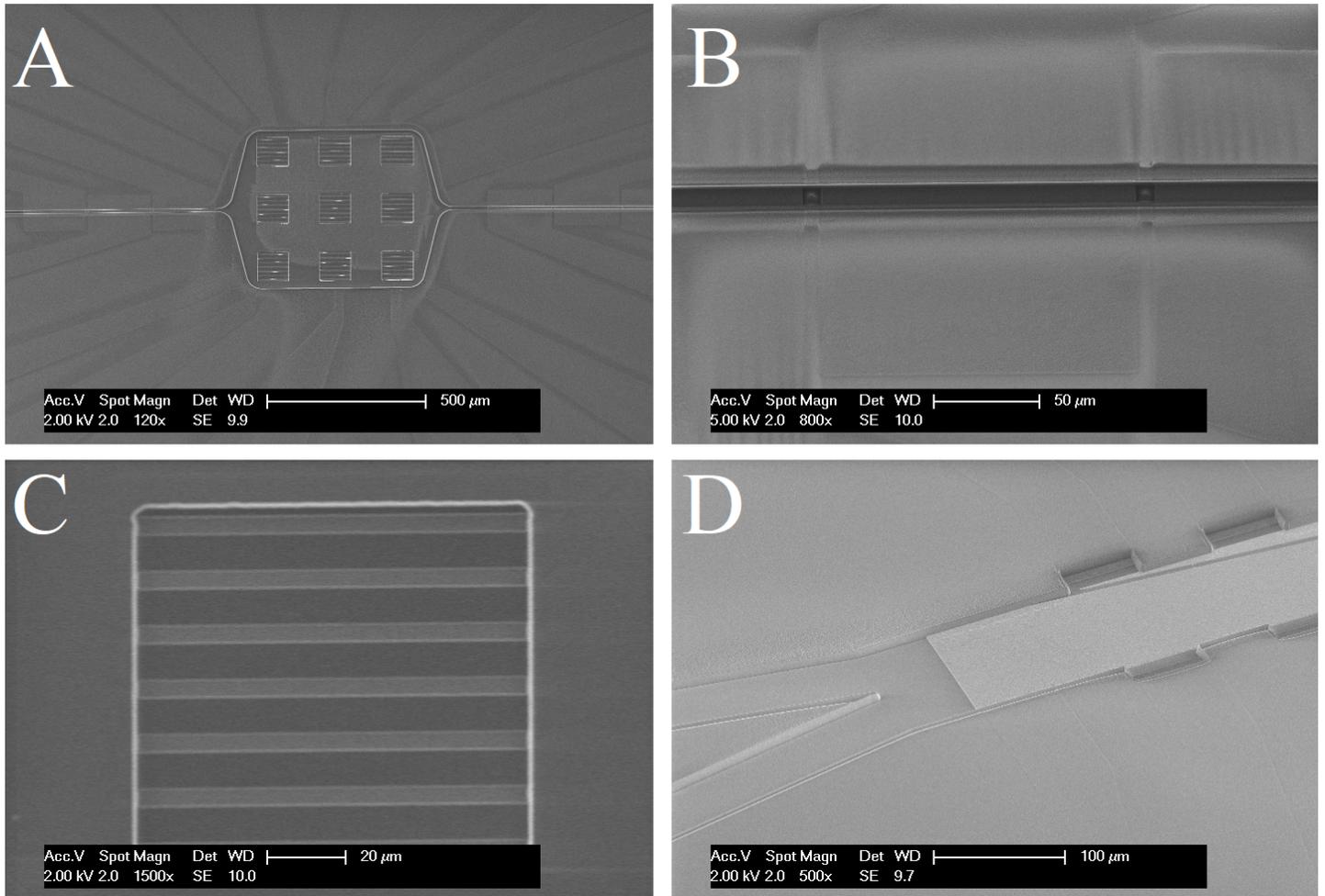


Figure 5.13. Pictures of the final devices under electron microscope. A) design #3, central chamber with 9 wells; B) design #4, particular of the channel (45deg tilted), flow cytometry electrodes covered by silicon dioxide, producing "hills" next to the channel; C) design #1, particular of a nicely etched microwell; D) dielectrophoretic sorter, particular of the two inlets (45deg tilted).

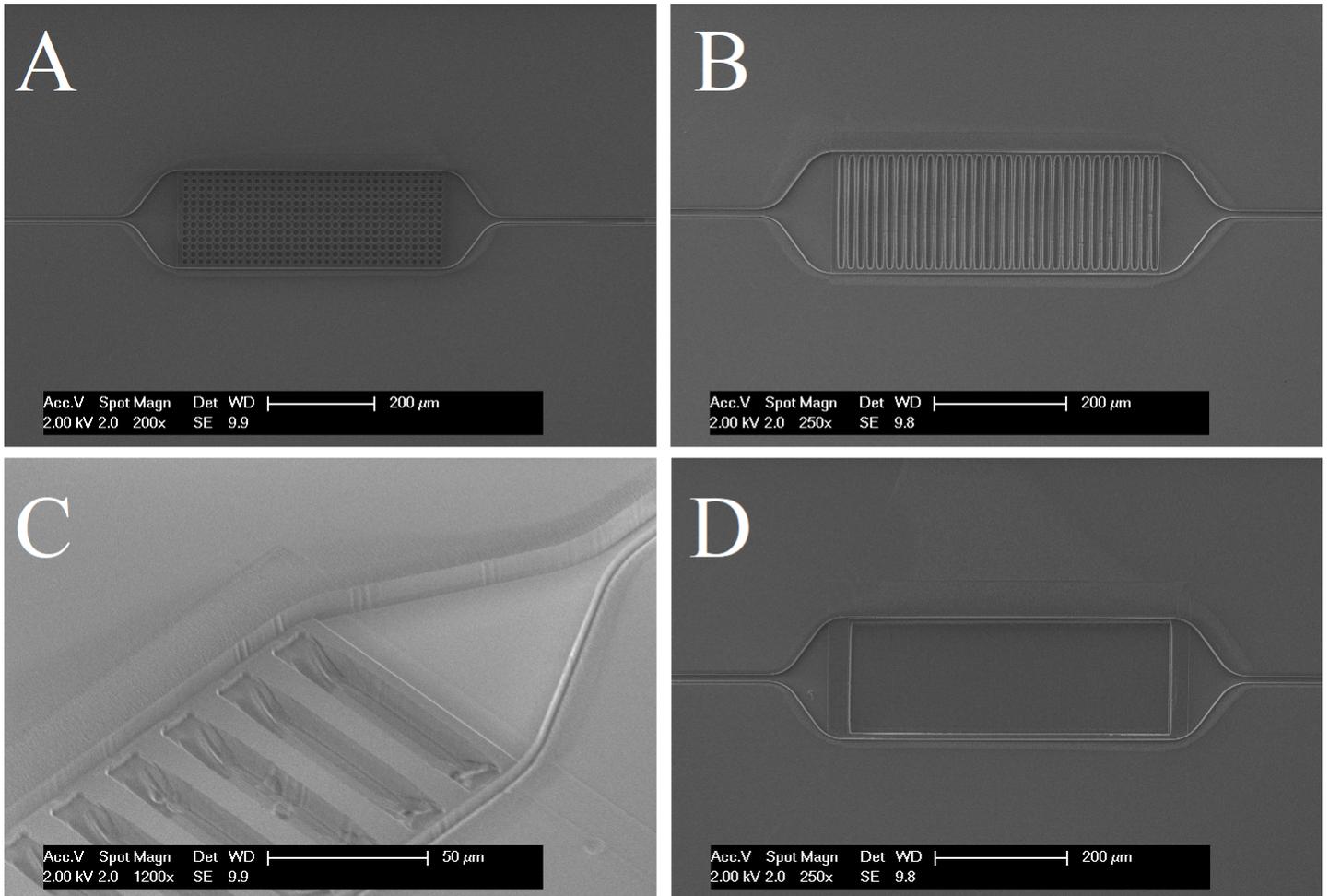


Figure 5.14. Pictures of the final devices under electron microscope. A) design #6, central chamber with wells; B) design #7, central chamber with wells; C) design #7, detail on silicon dioxide etching inside the chamber (45deg tilted); D) design #8, central chamber with well.

Chapter 6

System Integration

Despite being the most time consuming part, the realization of the chip in the cleanroom would be useless without implementing it in a system. Indeed, it wouldn't be possible to perform any measurement with the chip as it is, and a complementary system comprising electronics and microfluidics is needed. In this chapter the choices taken to connect the chip to the external world are described, with a final insight on what would still be needed in order to carry out a full experiment. Section 6.1 deals with the design of the PCB needed to connect the chip with an external electronic board for readout, section 6.2 describes the post-cleanroom processing of the wafers, from dicing to bonding, and section 6.3 gives some hints on possible choice of microfluidics interconnections, that time constraints didn't allow us to realize.

6.1 PCB Design

The necessity of designing a custom PCB was driven by the need of having an easy and standardize way to connect the chip to discrete component electronics, by means of a breadboard or similar fast prototyping solutions, to test the chip and its performances. The first solution, that was soldering 0.1-inch pin headers directly on top of the pads (that were designed with the same spacing for this reason), turned out to be unworkable, for the reason that solder tin didn't attach properly to the titanium nitride pads of the chip. The alternative was designing a simple PCB as an adaptor from the "chip" world (titanium nitride pads) to the "standard electronics" world (pin headers). The chip would then be wire bonded to the PCB, and pin headers would be soldered to the PCB instead of soldering them directly to the chip. This solution, apparently less straightforward than a standard Dual In-Line ceramic package (solution already available for all the chip produced by EKL or external source), was preferred, since it can be considered more customizable,

giving more freedom in realizing the microfluidic connections on top of the chip.

The PCB were designed in DesignSpark PCB 8.1 (given the simplicity of the project no schematic was realized), first creating a padstack for the new component (the chip), then routing the new component to standard 0.1-inch pinholes, and finally designing the geometries of the board. Two versions of the chip were realized, since chip designs #1 to #8 have a 16 pads pinout, while designs #9 and #10 have a 38 pads pinout (Fig. from 6.1 to 6.4 show details of the two PCBs). The gerber files generated comprised top/bottom copper layer, top/bottom soldermask, top/bottom silkscreen, outline, drill data.

The chosen PCB manufacturer was EuroCircuit, ten 16-pin PCBs and five 38-pin PCBs were ordered. The option chosen were the standard ones, i.e. double layer PCB with green soldermask, white silkscreen, plated holes, lead-free finish (this last choice turned out to be non-optimal, as further explained in section 6.2.2). Due to time constraints, another order was placed at PCBWay (faster delivery option), of just ten pieces of the 16-pin PCB, with the same manufacturing options, except for a blue soldermask in order to distinguish them from the others. PCBs from both manufacturers turned out to be perfectly made, and no problems arose due to PCB manufacturing.

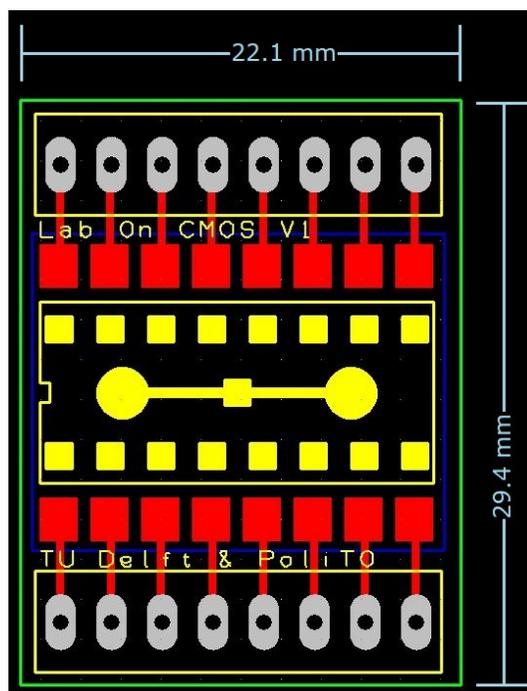


Figure 6.1. Design view of the 16-pin PCB in DesignSpark. Legend: Yellow is Top Silkscreen, Dark Blue is Bottom Silkscreen, Red is Top Copper, Grey are Vias for pin headers, Green is Outline.

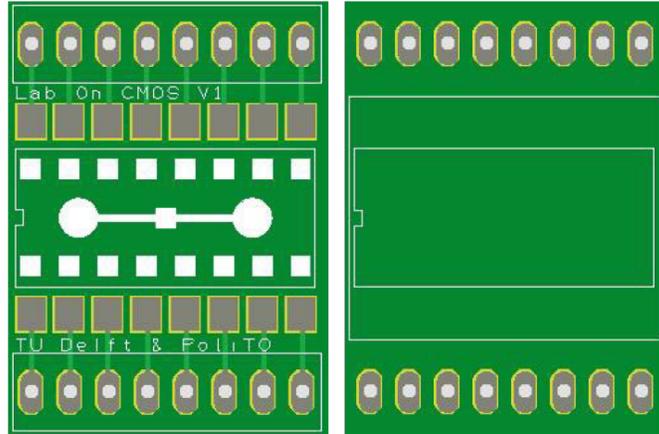


Figure 6.2. Rendering of the final 16-pin board (left top side and right bottom side) from EuroCircuit Gerber Checker.

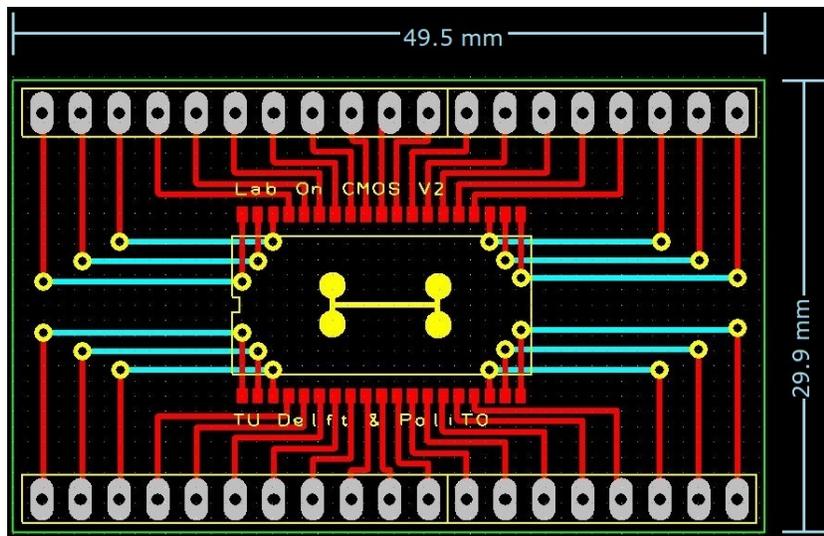


Figure 6.3. Design view of the 16-pin PCB in DesignSpark. Legend: Yellow is Top Silkscreen, Dark Blue is Bottom Silkscreen, Red is Top Copper, Light Blue is Bottom Copper, Grey are Vias for pin headers, Green is Outline.

6.2 Bonding and Packaging

After finishing cleanroom process, the wafers were ready to be diced in single chips, to be bonded to the PCBs. The next sections describe the system level packaging of the chips, i.e. the steps in between cleanroom processing and testing.

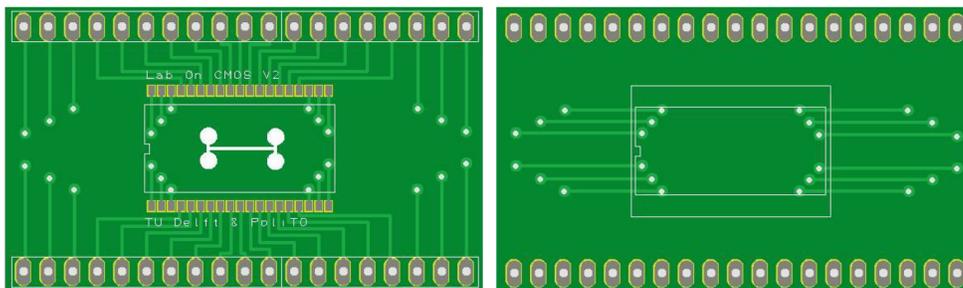


Figure 6.4. Rendering of the final 38-pin board (left top side and right bottom side) from EuroCircuit Gerber Checker.

6.2.1 Wafer Dicing

Dicing of the wafers was done with an automated procedure thanks to a DAD321 disco saw. The machine was programmed to cut the wafers vertically with a spacing of 2cm, and horizontally with a spacing of 1cm, starting from the centre of the wafer, and obtaining 2x1 cm² chips. The diced wafers were then cleaned with an SPS wafer cleaner, and glued to antistatic plastic foil for easy handling (Fig. 6.5). Wafers were then checked under optical microscope and conductivity measurements were performed in order to select the working chips (Fig. 6.6), then single chips were separated from the plastic foil (Fig. 6.7), and 2-3 chips for each design were glued with standard epoxy on top of the PCBs, ready for wiring (Fig. 6.8)

6.2.2 Wire Bonding

The initial solution for wiring the chips to the pads of the PCBs, was to use gold wire thermal bonding, that consists in a machine dispensing a 25 μ m golden wire through a nozzle, applying heat as the point of the nozzle touches the pad, melting the gold of the wire together with the material of the pad. Unfortunately, it wasn't possible to wire bond the titanium nitride pads of the chips, since the hard ceramic material made it impossible for the gold wire to stick. To solve this problem we used wedge bonding, also called thermosonic bonding, which uses a 32 μ m aluminium wire and applies not only heat but also ultrasound vibrations when the nozzle touches the pad, so that the wire can stick more easily. This time there were no problems in sticking the wire to the titanium nitride pads of the chips, but the main problem was that the choice of pads we used for the PCBs (lead-free finish without gold, nickel or other "bonding-friendly" material) made it impossible to wire them. Eventually, a solution was found via increasing the power of the bonding, thus penetrating the lead-free finish of the pads and directly bonding on the copper below. The machine used was a ACCELONIX wedge bonder, parameters for bonding are collected in table 6.1. After bonding, the area between the PCB pads and the chip pads was manually

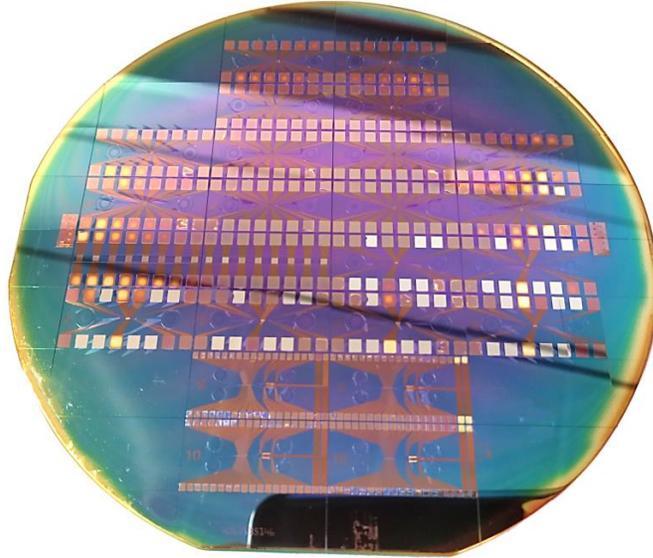


Figure 6.5. Wafer that has been diced with DAD321 disco saw and glued to antistatic plastic foil.

covered with transparent and insulating medium density epoxy glue, carefully trying not to cover any area of the channel or the inlet/outlet, to not damage the device.

Bond 1 (chip)	Ultrasonic Power (mW)	320
	Time (ms)	300
	Force (mN)	300
Bond 2 (PCB)	Ultrasonic Power (mW)	400
	Time (ms)	400
	Force (mN)	500
	Loop Height (μm)	1200
	Work Height (μm)	4900

Table 6.1. Bonding parameters used on the ACCELONIX wedge bonder. It can be noticed that parameters for Bond 2 are significantly greater than parameters for Bond 1, this is caused by the fact that it was impossible to bond the aluminium wire to PCB pads and it was necessary to penetrate the surface material and bond directly with the copper underneath.

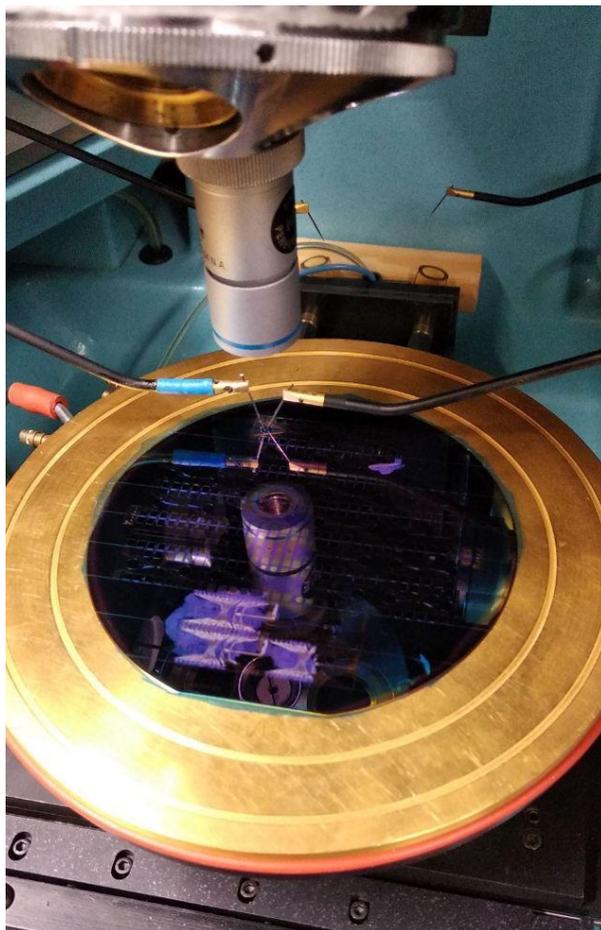


Figure 6.6. Electrical conductivity measurement of titanium nitride tracks, the probe station was connected to a multimeter.

6.3 Microfluidic Interconnections

In order to seal the Lab-On-Chip and connect the system to a microfluidic circuit, a number of solutions exist [55], [56] and have been investigated, although time constraints allowed us to test just a simplified one, which turned out to not seal the device perfectly.

The classic method to seal open channels in a Lab-On-Chip consists in pouring PDMS into a mould, curing it, realizing inlet/outlet holes into the PDMS brick, and then fixing it on top of the Lab-On-Chip via plasma treatment (Fig. 6.9A). This method, despite being straightforward for everybody working on Lab-On-Chip, resulted difficult to be realized, since EKL wasn't equipped to realize Lab-On-Chip and would have required additional time.

An even more effective way to seal the chips would have been wafer bonding:

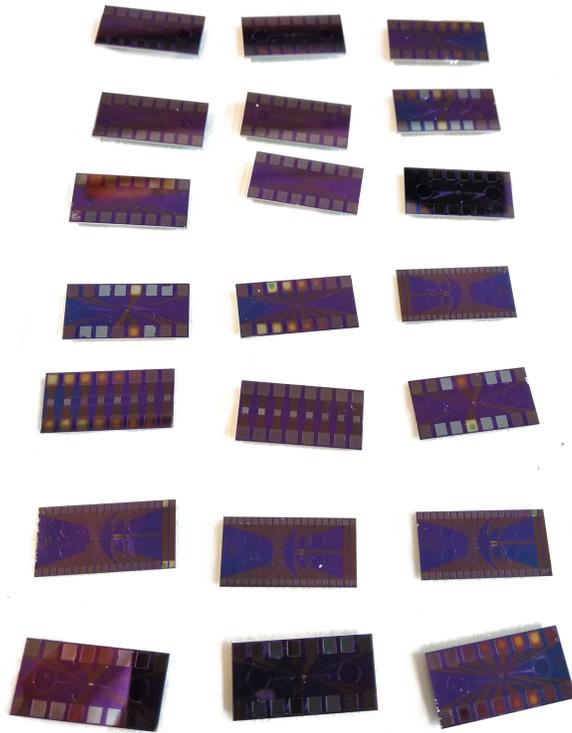


Figure 6.7. Series of chips singularly separated from one wafer.

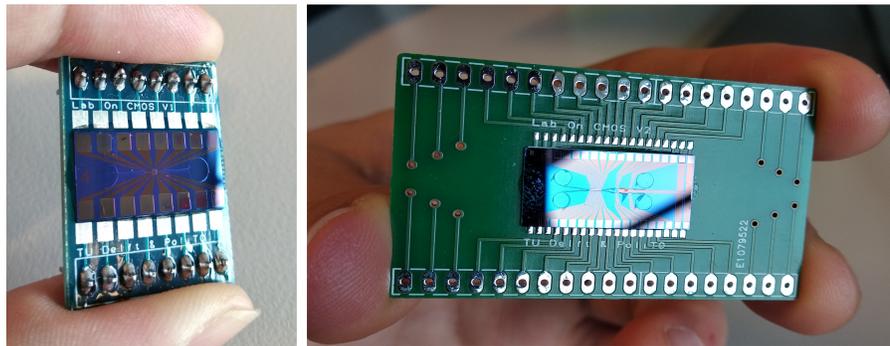


Figure 6.8. Two chips glued to their PCBs. Left, chip with design #1 connected to 16-pin PCB; right, chip with design #9, connected to 38-pin PCB.

after wafer processing, and prior to wafer dicing, glass/silicon wafers, with holes corresponding to inlets/outlets and contact pads, could have been bonded (by anodic bonding or adhesion bonding) to processed wafers, sealing the chips, and then dicing already sealed Lab-On-Chips (Fig. 6.9B). The reason this method was discarded is that the choice of materials couldn't allow us to use anodic bonding, while the

narrowness of the channel made us think that the use of whatever glue would have clogged it.

A third way to create a lid for the chips was to use already made coverslips to cover the exposed area of the channel (Fig. 6.9C). This method have been tested with silicone-covered plastic and glass coverslips. The silicone layer (to be put in contact with the top of the chip) was supposed to make a firm electrostatic bond with the chip, but two problem arose: if glass coverslips were used, there was no possibilities of drilling inlet/outlet and contact pads; if plastic coverslips were used, the drilling operation produced bad finishes, and the adhesion was poor. A plastic tube was glued on top of a drilled plastic coverslip, and subsequently fixed on top of the Lab-On-Chip, to test sealing, and pink coloured water was used to optically inspection any leaking: unfortunately the results showed that no pressure could be applied without water detaching the lid from the chip.

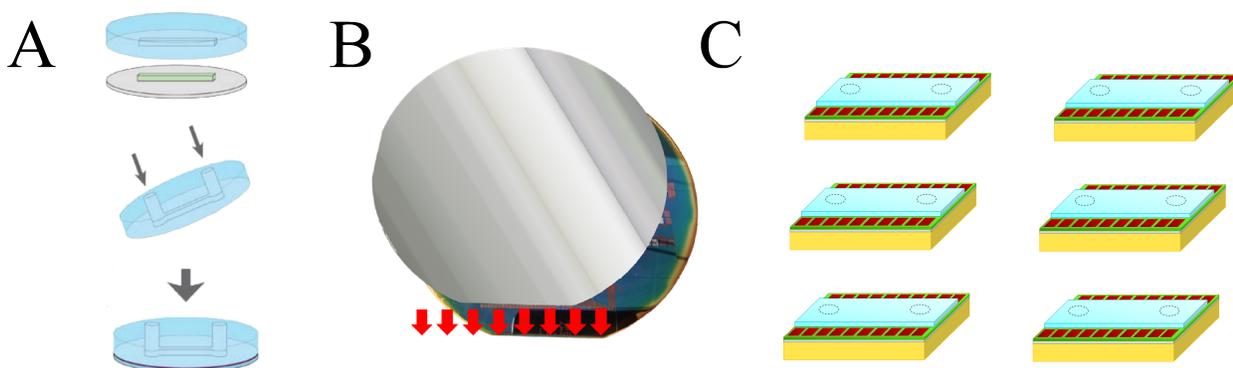


Figure 6.9. Three investigated methods to seal the microchannel of the Lab-On-Chip. A) PDMS is mould in the required shape, inlet/outlet are drilled, and this new PDMS lid is fixed to the chip thanks to a plasma treatment; B) full wafer bonding, where silicon/glass wafer are bonded to processed wafers thanks to electrostatic forces (anodically) or chemical bounds (glue); C) single-chip bonding, where coverslips are applied to individual chips after wafer dicing.

Chapter 7

Measurements

After realizing the complete device, a number of measurements and testing procedures have to be carried out in order to validate the idea. In our specific case, not being able to finish the realization of the final device, measurements have been limited to a simple electrical and electrochemical characterization. This chapter reviews the testing procedures that have effectively been performed at chip level, while measurements at system level weren't feasible and are collected in section 8.1.

7.1 Preliminary Measurements

The first conductivity measurements were performed inside the cleanroom class 100, as explained in section 5.3.6: during the RIE of the silicon dioxide it was important to keep conductivity monitored, since the etching couldn't stop before removing all the SiO_2 from the top of the electrodes, but a strong etching could damage the titanium nitride of the electrodes, because of the ion bombardment. As already mentioned, the etching was performed at a lower power, and in several 1-minute steps. In between every etching step, a conductivity measurement was performed on a 2-point probe station, equipped with an OLYMPUS optical microscope and connected to a bench multimeter to automatically measure conductivity. In every measurement, one of the probe was connected to an electrode, and the other to the electrode's pad. When the measurement showed a significant drop in resistance (from $\sim 100\text{-}1000\text{M}\Omega$ to $\sim 100\text{-}1000\text{k}\Omega$), the etching could be considered complete. NB: the conductivity measurements had to be performed on multiple spots (i.e. on different chips) every time, since the etching performed under the TRIKON OMEGA appeared to be non uniform. In fact, chips closer to the centre of the wafer were etched faster than chips at the border of the wafer (non uniform etching profile). The decision of waiting until all the chips (also the ones at the border of the wafer) were completely etched, risking to overetch the chips at the centre, didn't produce

any significant drawback, and all the chips appeared to be working.

7.2 2-Point Probe

After processing, diced wafers were brought to the Measurement Lab, where conductivity measurements were performed again on every chip, to select the working ones, as already stated in section 6.2.1. The conductivity was measured on a CASCADE MICROTECH probe station, with 6 micromanipulators for the probes (just two were used for conductivity measurements) and golden chuck. Out of the 96 chips from the 4 processed wafer (two wafers from the initial batch of six got "sacrificed" to test particularly critical recipes), 62 chips resulted to be defect-free, after both optical inspection under microscope and electrical conductance measurement, 27 chips resulted to have fabrication defects (missing pads, badly etched IDEs, etc) and were put apart for further inspection, 7 were completely unusable (broken or seriously damaged, e.g. see Fig 7.1). A representation of the yield from each wafer is depicted in Fig. 7.2. As already mentioned, 2-3 chips for each design were selected and bonded to the PCBs.

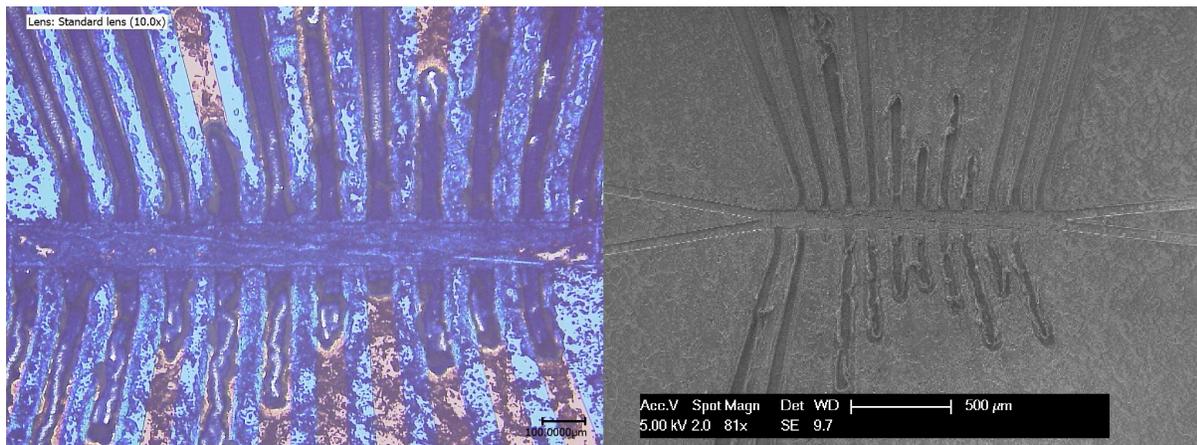


Figure 7.1. Pictures taken under KEYENCE optical microscope (left) and with SEM (right) of a dielectrophoretic sorter from design #9, but from a seriously damaged chip. In this case the problem was caused by the stripping of the very thick and heavily burned layer of photoresist after the long etching phase under the DRYTEK, that caused metal tracks to detach from the substrate.

7.3 EIS Measurements

To validate the electrochemical model of the IDEs, Electrochemical Impedance Spectroscopy measurements were performed on working chips, using a AUTOLAB

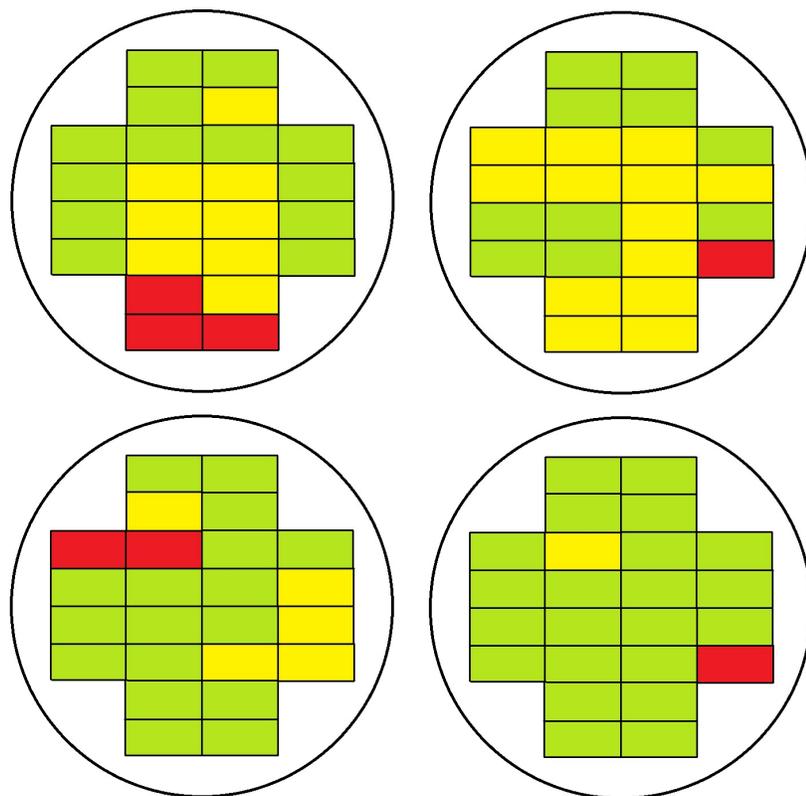


Figure 7.2. Representation of the yield for each of the 4 processed wafers. Legend: Green corresponds to perfectly working chips, Yellow corresponds to partially damaged chips, Red corresponds to completely broken chips.

METROHM potentiostat. To give statistical relevance to the measurements, many chips were supposed to be measured, but the problems arose during the bonding phase allowed us to have just one completely bonded and working device, so all the EIS measurements here reported have been performed on that device. All the measurements were taken with a 2-terminal configuration (working electrode connected to sensing electrode, reference electrode connected to counter electrode), with 0V DC and 100mV AC signal, from 10Hz to 100kHz. Fig. from 7.4 to 7.6 show the magnitude/phase vs frequency graphs of the IDEs of 3 microwells of the device, obtained connecting one terminal of the potentiostat to the common ground, and the other terminal to the corresponding IDE. The measurements were taken first with dry IDEs, then with the microwells wet in PBS (Gibco pH 7.2 by ThermoFisher Scientific). It is possible to notice that the behaviour is similar in all the 3 measurements, and compliant with the expected results: dry electrodes have a very high impedance that decreases with the increasing of frequency, and a nearly constant phase at -90° ,

while wet electrodes present a much lower magnitude (about 1/3 of dry electrodes), and a phase drop at 50-100kHz. The behaviour is capacitive as expected, but in both dry and wet cases more elements have to be taken in consideration in order to explain 2nd order poles (e.g. the bump at 2-3kHz for dry electrodes and 1kHz for wet electrodes).

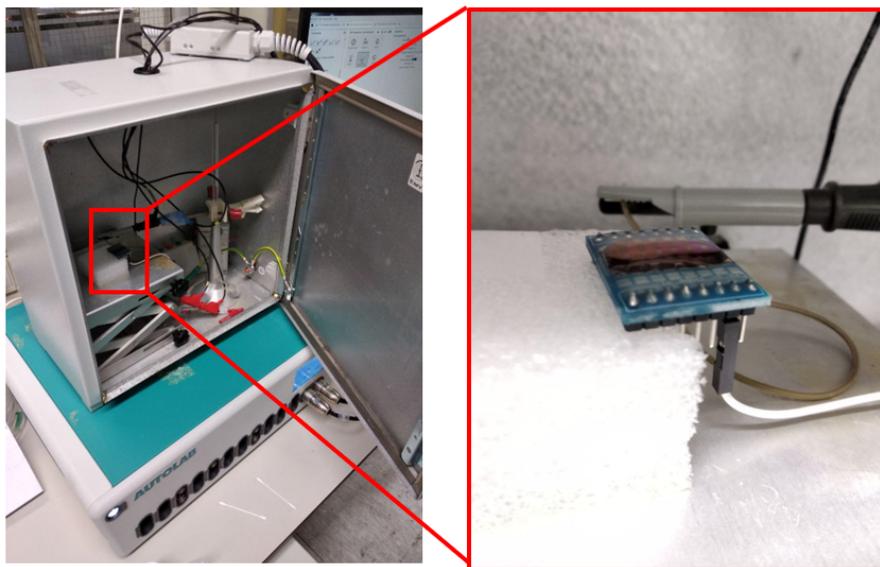


Figure 7.3. Setup used for the EIS measurements of the chip (left) and detail of the device connected to the potentiostat terminals.

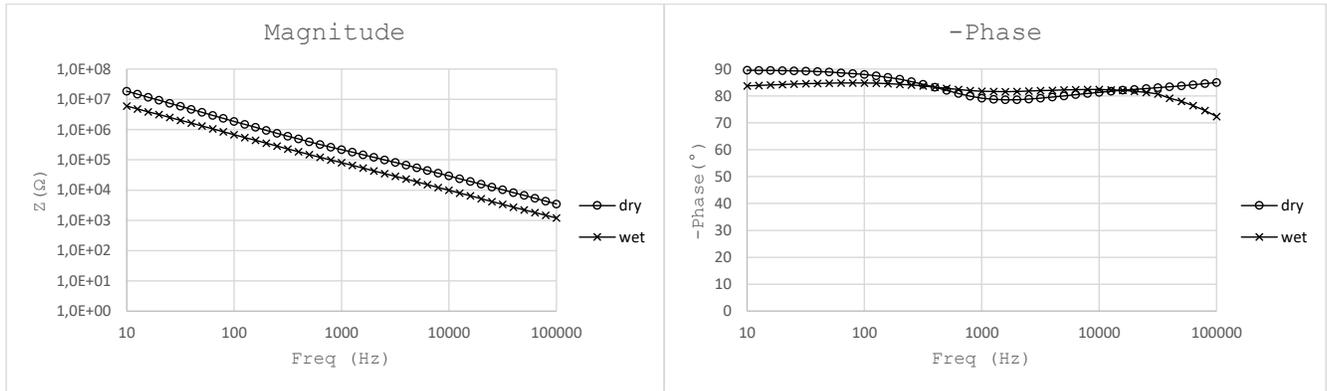


Figure 7.4. Graphs showing Magnitude vs Frequency (left) and -Phase vs Frequency (right) of the first microwell measured, both dry and wet in PBS.

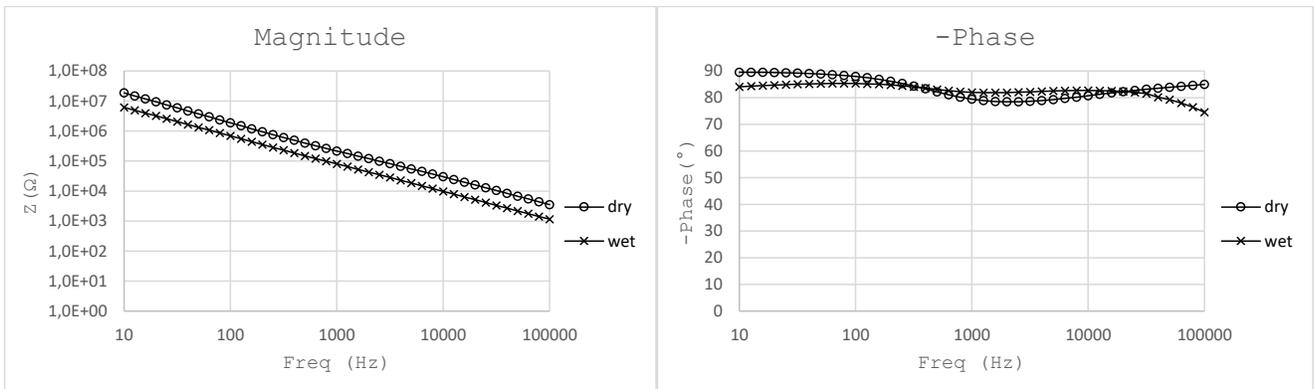


Figure 7.5. Graphs showing Magnitude vs Frequency (left) and -Phase vs Frequency (right) of the second microwell measured, both dry and wet in PBS.

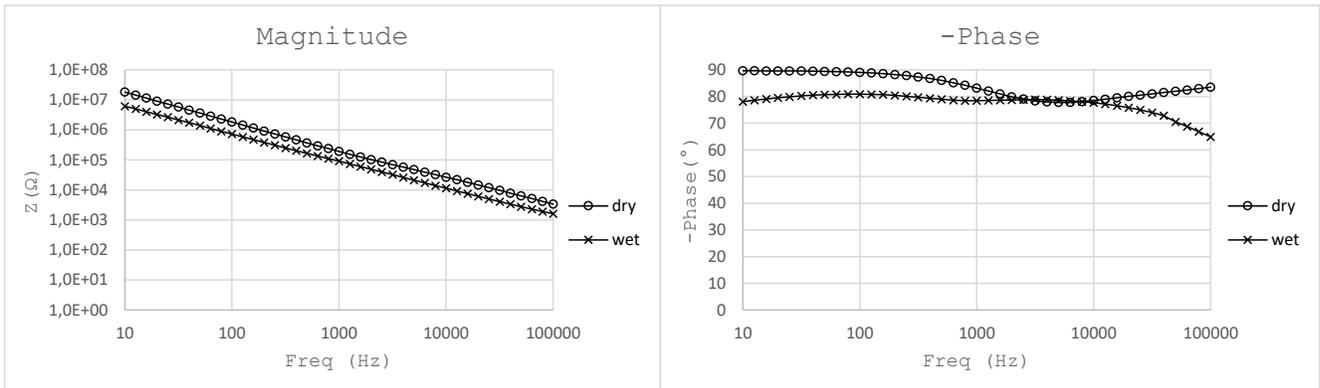


Figure 7.6. Graphs showing Magnitude vs Frequency (left) and -Phase vs Frequency (right) of the third microwell measured, both dry and wet in PBS.

Chapter 8

Conclusions

As a conclusion of this thesis, it is important to highlight the obtained results, to take stock of the situation and to propose possible outcomes of this work. Timing constraints have put limitations on the number of experiments realized, and even if the overall picture looks promising, still a lot of work has to be done before obtaining the final result, i.e. a single-cell impedance cytometer with both high throughput and long term analysis capabilities.

As main result, a novel Lab-On-Chip device for multi-sensing operations has been realized, and the following objectives have been reached:

- The chip has been designed, comprising of channels for Impedance Flow Cytometry (IFC) and wells with Interdigitated Electrodes (IDEs) for Electrochemical Impedance Spectroscopy (EIS). Photolithographic masks have been designed for production of the chip on 4-inch silicon wafers;
- Several designs of the chip have been theorized and realized in different areas of the wafers, with the same fabrication process, in order to characterize the device and test several parameters (e.g. IDEs length, width). A novel dielectrophoretic cage design was proposed, simulated and realized, not relying on a top counter electrode (e.g. ITO glass on top of the chip). One design proposes the integration of a dielectrophoretic sorter, adding actuation capabilities to the chip;
- The wafers were processed and chips were realized in cleanroom class 100. The flowchart used for the fabrication of the chips was written to be fully CMOS compatible, for a future co-integration with integrated readout, and fully biocompatible;
- A PCB was designed and fabricated, and used to connect the chip with the

external world. Standard 0.1 inch pin headers were soldered to the PCBs, and the chip was correctly bonded to the PCB using ultrasonic bonding;

- An Electrochemical Impedance Spectroscopy analysis has been performed with both dry and wet electrodes, showing the behaviour of titanium nitride electrodes in air and in PBS solution.

During the 8 months dedicated to the project, many things didn't go as planned, and just the fabrication of the device (plus a short glimpse on the measurements) have been performed. Here the lacks of the project are listed:

- The initial idea of using photoresist to realize a sacrificial structure on top of which polyimide would create a bridge, sealing the Lab-On-Chip, has been discarded, because of fabrication problems using polyimide;
- The device has been realized with exposed channel and wells, but to complete the microfluidic circuit further processing is needed. Some ideas to close the Lab-On-Chip and plug it to syringe pumps were proposed, but they were not put into practice because of timing constraints;
- The PCB was manufactured with the wrong pad finishing, not suitable for wire bonding, which further slowed down the processing. Eventually, just two chips were wirebonded to a PCB;
- The fabrication of the device took more time than what it was planned, and less to no time was dedicated to measurements. Just EIS analysis on dry/wet electrodes has been performed, on the few chips that were available.

8.1 Future Work

In order to consider this project complete, a few more things have to be done. From the manufacturing side, a lid has to be produced, to close the channels, and to ensure sealing. Using the common approach, the lid would be created casting PDMS in a custom mould, realizing inlet/outlet connections, and fixing it to the silicon oxide chip after a plasma treatment. Sealing tests have to be run in order to validate the manufacturing procedure. From the testing and measurement side, EIS analysis should be performed again, on a significant number of devices to guarantee statistically reliable data and to test the different geometrical parameters, with dry electrodes, PBS, and PBS+microbeads (polystyrene or silicone dielectric beads of 6-8 μm of diameter) to simulate the presence of cells and show the change in the impedance spectrum.

To characterize DEP cages, two tests can be performed: first one, injecting PBS+microbeads and measuring how much the flux speed can be increased if cages are on, with respect to when cages are off, before cells are sucked away from the wells; second one, performin an EIS analysis when beads are collected with DEP, with respect to when they are collected just in a gravitational way. To characterize the DEP sorter, various frequencies should be tested to observe a migration of beads from one side of the channel to the other side.

The next step toward the co-implementation of CMOS and microfluidics would be the design of an integrated analog readout circuit and its realization on silicon wafers (EKL cleanroom proposes a proprietary $1\mu\text{m}$ BiCMOS, 7 masks technology for IC design), prior to the back-end microfluidic channels/wells. This combination would constitute a chip able to perform fast, automated, high precision, lens-free, single cell imaging.

8.2 Final Considerations

This project successfully worked as a proof of concept to demonstrate the co-integration of microfluidics and CMOS processing, leading the way toward a next generation of microfluidic devices (by some defined as Lab-On-CMOS/Bio-CMOS), i.e. a true combination of electronics and biology, aimed at exploiting engineering know-how of microelectronics and nanotechnologies to realize platforms for a better diagnosis/treatment.

This device, despite not complete, is already a step forward to a more precise and reliable cell sensing, that uses impedance information to reconstruct biological characteristics of cells. The impedance sensing technique proved to be an excellent candidate for label-free, automatic, precise sensing operation, and a paradigm for Lab-On-CMOS technology development.

Appendix A

Flowcharts



Lab-On-Chip for Electrical Cytometry

Version: 2

Valid from: 1 September 2018

Made by: Federico Bedini

Run number: EC2300

Process engineer: Federico Bedini

Mentor: Tom Scholtes

Start date processing: 1 October 2018

Estimated end date: 1 December 2018

Contamination: None

Labs: CR100

EKL(Else Kooi Laboratory)
DELFT UNIVERSITY OF TECHNOLOGY
Address : Feldmannweg 17, 2628 CT Delft, The Netherlands
P.O. Box : 5053, 2600 GB Delft, The Netherlands
Phone : +31 - (0)15 – 2783868
Fax : +31 - (0)15 – 2622163
Website : <http://ekl.tudelft.nl/EKL/Home.php>

Lab-On-Chip for Electrical Cytometry V2 – RUN NUMBER: EC2300

Detailed information about possible contamination: **NONE**

Place/Clean Rooms used in process:

- Write the sequence of used labs from start to finish.
- Which (Non-standard) materials or process steps
- Process step number
- What kind of process or machine was used?
- The other materials or wafers that contain non-green metals that are also processed in this machine

Example

Lab/ Clean Room	Non-standard materials	Process step	Machine- process	Other materials used in machine

If there are custom steps in a standard process or possible cross contamination materials are used:

Write down the

- Step number
- Material
- Machine/tool where the process is done
- Pre and past process step numbers that are used to prevent cross contamination.

Example

Step number	Material	Machine/Tool/lab	Process steps to prevent cross contamination

Lab-On-Chip for Electrical Cytometry V2 – RUN NUMBER: EC2300

GENERAL RULES

CLEANROOM BEHAVIOUR

- Always follow the "**Security and Behaviour**" rules when working in the EKL laboratories.
- Always handle wafers with care during processing. Use cleanroom gloves and work as clean as possible!!
- Use cleanroom gloves when working with vacuum equipment. Do not touch the inside or carriers with bare hands.
- Always check equipment and process conditions before starting a process. Do **NOT** make unauthorized changes!
- Directly notify the responsible staff member(s) when there are problems with equipment (like malfunction or contamination). Put the system down in the Phoenix reservation system, and turn the equipment status sign from **UP** or **Usable** to **DOWN**.
- DO NOT TRY TO REPAIR OR CLEAN EQUIPMENT YOURSELF**, and **NEVER** try to refresh a contaminated etch or cleaning bath! Only authorized staff members are allowed to do this.

PCC RULES

- All substrates, layers and chemicals which are not CMOS compatible are considered to be "**NON-STANDARD**" materials, and may be contaminating.
- The use of "non-standard" materials for processing in the class100 and SAL cleanroom must **ALWAYS BE EVALUATED AND APPROVED** by your mentor and in agreement with the PCC document.
- Wafers that are contaminated may **NEVER** be processed in any of the equipment without permission of the Equipment owner. Special precautions may have to be taken, like the use of a special substrate holder or container.
- Check the PCC "Rules & Instructions" - available on the "[EKL intranet webpage](#)" - for more details.

CLASS 100 RULES

CLEANING OF WAFERS

After several hours (4 hours max) of storage wafers must always be cleaned before performing a **COATING, FURNACE, EPITAXY** or **DEPOSITION** step.

Use the correct cleaning procedure:

- Tepla stripper ⇒ for removal of implanted or plasma etched photoresist
- Acetone ⇒ for removal of photoresist that is not implanted or plasma etched
- HNO₃ 99% (Si) ⇒ for IC compatible wafers which do not need a HNO₃ 69.5% step
- HNO₃ 99% (Al) ⇒ for wafers which are or have been in contact with one of the following metals: like Al, Al(1%Si), Ge, Ti, Zr
- HNO₃ 99% (Si) + HNO₃ 69.5% (Si) ⇒ for all other IC compatible wafers

- Note:**
- The above described cleaning procedures are only valid for IC compatible wafers with "standard" materials on them. **In all other situations follow the PCC rules (Previously to be discussed with the mentor).**
 - Wafers do not have to be cleaned **after** a furnace, epitaxy or deposition step if the next process step will be performed immediately, unless the wafers are covered with particles.

FURNACE RESTRICTIONS

Wafers that are covered with photoresist or a metal layer may **NEVER** be processed in any of the furnaces. This also applies for wafers from which a metal layer has been removed by etching. Only alloying in tube C4 is allowed for wafers with an aluminium layer.

MEASUREMENTS

Always perform all the measurement and inspection steps, and **write down the results in your journal and in the result tables that can be found at some of the equipment!!** The results are used to check the condition of the processes and/or equipment.

It is possible to use the following Class 100 equipment to measure directly onto your (IC compatible) process wafers:

- The Leitz MPV-SP, the WOOLLAM and the SAGAX. These systems are used for thickness measurements of transparent layers. The measurements are non-destructive and without contact to the wafer surface.
- The Dektak 8 surface profilometer. This system is used for step height measurements. In this case a needle will physically scan over the wafer surface (contact measurement), which can be destructive for structures.
- The XL50 SEM. It can be used for inspection of your wafers and for width, depth or thickness measurements.

Note: After certain measurements cleaning of your wafers may be required for further processing.

An extra wafer must be processed when other measurement methods will be used (like sheet resistance and junction depth measurements). These wafers cannot be used for further processing.

Lab-On-Chip for Electrical Cytometry V2 – RUN NUMBER: EC2300

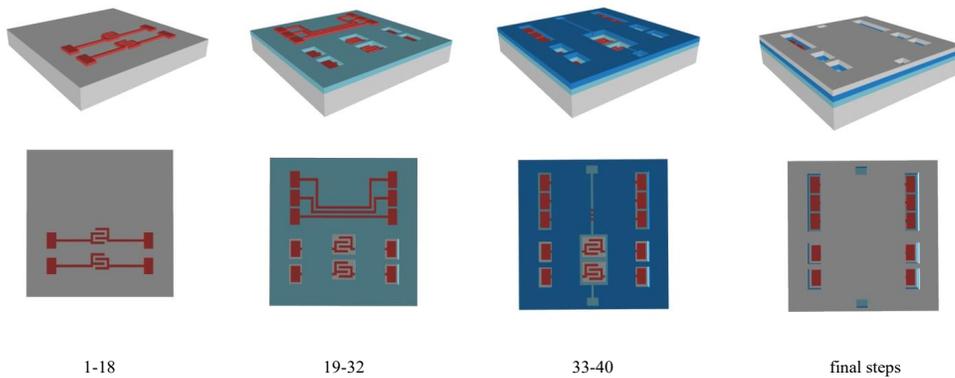
STARTING MATERIAL

Use **SILICON WAFERS, SINGLE SIDE POLISHED**

Type:	p/B (p-type, boron)
Orientation:	<100>
Resistivity:	2-5 Ω cm
Thickness:	525 \pm 15 μ m
Diameter:	100 mm
Number of wafer:	6

Background: Kind of process description about the device.

This project aims at the realization of a Lab-On-Chip device with the double function of performing impedance flow cytometry and electrical impedance spectroscopy, two similar (but conceptually different) measurement of the impedance of cells, to characterize them. First, cells will pass in a 10x10 micrometer channel, some electrodes at the bottom will sense the transit of the cells (theoretically one at a time), then cells will arrive in a chamber with several wells, in which groups of cells will fall and will be analyzed by interdigitated electrodes. The challenge of this project is to realize two different sensing layers, at two different depths, each with its own round of electrodes, and to seal the device with a lid. Possibilities include the use of two different wafers bonded together, or the use of a photoresist sacrificial layer to sustain a polyimide cover layer.



Lab-On-Chip for Electrical Cytometry V2 – RUN NUMBER: EC2300

ALIGNMENT MARKERS ON WAFERS

1. COATING

EVG 120: program “Co – 3012 – zero layer”

- HDMS primer
- Spin coating SPR3012 positive resist
- Soft bake 95°C for 90 seconds
- Edge bead removal

2. ALIGNMENT/EXPOSURE

ASML PAS 5500: Stepper – program: “FWAM”

- Energy Dose: auto
- Focus: 0

3. DEVELOPING

EVG 120: program “Dev – SP”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

4. INSPECTION

Microscope inspection, no resist is allowed

5. WAFER NUMBERING

Glass pen – WAFER NUMBER 1 – 6

6. PLASMA ETCHING: Etching the alignment markers on the wafer

TRIKON OMEGA 201: sequence “URK_NPD” (20°C platen)

- Breakthrough: CF4/O2, 5 mTorr, 10 seconds
- Bulk etch: Cl2/HBr, 60 mTorr, 40 seconds

7. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O2 plasma, **program 1** (1000 watts, endpoint detection, 2 min overetching)

ETCH STOP/PASSIVATION LAYER OF SILICON NITRIDE

8. CLEANING: organics (HNO3 99%) and metals (HNO3 69.5%, 110°C)

- 10 minutes “HNO3 99% (Si) room temperature”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- 10 minutes “HNO3 69.5% 110C (Si)”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with RED DOT

9. LPCVD DEPOSITION: 200 nm SiN

FURNACE E2: Silicon Nitride. Program “StdSiN” (Variable time, calculate on the basis of avg deposition time)

Lab-On-Chip for Electrical Cytometry V2 – RUN NUMBER: EC2300

10. MEASUREMENT: SiN thickness

LEITZ MPV-SP: program “**lpcvd loSiN >50nm on Si**”

FIRST ROUND OF ELECTRODES

11. CLEANING: organics (HNO3 99%) and metals (HNO3 69.5%, 110°C)

- 10 minutes “**HNO3 99% (Si) room temperature**”. Carrier with RED DOT
- Rinse in Quick Dump Rinsers, standard program until resistivity is 5 Mohm
- 10 minutes “**HNO3 69.5% 110C (Si)**”. Carrier with RED DOT
- Rinse in Quick Dump Rinsers, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with RED DOT

12. METALLIZATION: stack of 40nm Ti and 200 nm TiN

TRIKON SIGMA 204 sputter coater. Recipe “**Ti40_TiN200_350C**”

- IMMEDIATELY AFTER CLEANING
- 1 dummy wafer before batch with recipe “**Trg_cln_Ti_350C**”
- 1 dummy wafer between every batch wafer with recipe “**Ti_in_between_350C**”

13. COATING

EVG 120: program “**Co – 3012 – 1,4um**”

- HDMS primer
- Spin coating SPR3012 positive resist
- Soft bake 95°C for 90 seconds
- Edge bead removal

14. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “**MASK1_FIRSTELECTRODES**”

- Energy Dose: 7sec, 15mW/cm²
- Focus: 0

15. DEVELOPING

EVG 120: program “**Dev – SP**”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

16. INSPECTION

Microscope inspection, no resist is allowed

17. PLASMA ETCHING: Etching TiN USE A TEST WAFER TO MEASURE ETCHING TIME

TRIKON OMEGA 201: sequence “**TiN300nm**” (25°C platen)

- Bulk etch: Cl₂/HBr, 60 mTorr, 80 seconds with Endpoint Detection (falling edge)
- Overetch: Cl₂/HBr, 60 mTorr, 25 seconds

NB: Endpoint Detection not reliable, use dummy wafer to measure etching, and manual stop recipe

18. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O₂ plasma, **program 1** (1000 watts, endpoint detection, 2 min overetching)

Lab-On-Chip for Electrical Cytometry V2 – RUN NUMBER: EC2300

SILICON OXIDE DEPOSITION (WELLS)

19. CLEANING: organics (HNO₃ 99%) GREEN METALS CLEANING LINE

- 10 minutes “**HNO₃ 99% (Si) room temperature**”. Carrier with YELLOW/GREEN DOT
- Rinse in Quick Dump Rinsers, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with BLACK DOT

20. PECVD DEPOSITION: 10um SiO₂

NOVELLUS CONCEPT ONE: recipe “**xxx_siostd**” (Variable time, on the basis of avg deposition time)

- IMMEDIATELY AFTER CLEANING
- USE A TEST WAFER TO KNOW EXACT DEPOSITION TIME

21. MEASUREMENT: SiO₂ thickness

LEITZ MPV-SP: program “**SiO₂ on Si**” on the test wafer

SECOND ROUND OF ELECTRODES

22. CLEANING: organics (HNO₃ 99%) GREEN METALS CLEANING LINE

- 10 minutes “**HNO₃ 99% (Si) room temperature**”. Carrier with YELLOW/GREEN DOT
- Rinse in Quick Dump Rinsers, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with BLACK DOT

23. METALLIZATION: stack of 40nm Ti and 200 nm TiN

TRIKON SIGMA 204 sputter coater. Recipe “**Ti40_TiN200_350C**”

- IMMEDIATELY AFTER CLEANING
- 1 dummy wafer before batch with recipe “**Trg_cln_Ti_350C**”
- 1 dummy wafer between every batch wafer with recipe “**Ti_in_between_350C**”

24. COATING

EVG 120: program “**Co – 3012 – 1,4um**”

- HDMS primer
- Spin coating SPR3012 positive resist
- Soft bake 95°C for 90 seconds
- Edge bead removal

25. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “**MASK3_SECONDELECTRODES**”

- Energy Dose: 7sec, 15mW/cm²
- Focus: 0

26. DEVELOPING

EVG 120: program “**Dev – SP**”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

Lab-On-Chip for Electrical Cytometry V2 – RUN NUMBER: EC2300

27. INSPECTION

Microscope inspection, no resist is allowed

28. PLASMA ETCHING: Etching TiN USE A TEST WAFER TO MEASURE ETCHING TIME

TRIKON OMEGA 201: sequence “**TiN300nm**” (25°C platen)

- Bulk etch: Cl₂/HBr, 60 mTorr, 80 seconds with Endpoint Detection (falling edge)
- Overetch: Cl₂/HBr, 60 mTorr, 25 seconds

NB: Endpoint Detection not reliable, use dummy wafer to measure etching, and manual stop recipe

29. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O₂ plasma, **program 1** (1000 watts, endpoint detection, 2 min overetching)

SILICON OXIDE DEPOSITION (CHANNEL)

30. CLEANING: organics (HNO₃ 99%) **GREEN METALS CLEANING LINE**

- 10 minutes “**HNO₃ 99% (Si) room temperature**”. Carrier with YELLOW/GREEN DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with BLACK DOT

31. PECVD DEPOSITION: 10um SiO₂

NOVELLUS CONCEPT ONE: recipe “**xxx_siostd**” (Variable time, on the basis of avg deposition time)

- IMMEDIATELY AFTER CLEANING
- USE A TEST WAFER TO KNOW EXACT DEPOSITION TIME

32. MEASUREMENT: SiO₂ thickness THIS MEASUREMENT IS NOT FEASIBLE WITH LEITZ

LEITZ MPV-SP: program “**SiO₂ on Si**” on the test wafer

ETCHING OF THE SILICON OXIDE (FIRST STEP)

33. CLEANING: organics (HNO₃ 99%) **GREEN METALS CLEANING LINE**

- 10 minutes “**HNO₃ 99% (Si) room temperature**”. Carrier with YELLOW/GREEN DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with BLACK DOT

34. COATING

EVG 120: program “**Co – 3027 – 3.1um**” COATING WITH THICK RESIST

- HDMS primer
- Spin coating AZ3027 positive resist
- Soft bake 95°C for 90 seconds
- Edge bead removal

35. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “**MASK4_MICROCHANNEL**”

- Energy Dose: 20s, 15mW/cm²
- Focus: 0

Lab-On-Chip for Electrical Cytometry V2 – RUN NUMBER: EC2300

36. DEVELOPING

EVG 120: program “Dev – SP”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

37. INSPECTION

Microscope inspection, no resist is allowed

38. PLASMA ETCHING: Etching away SiO₂ to realize channel and chamber geometries

DRYTEK TRIODE 384T: recipe “OXD_SFT_LND”

Standard SiO₂ etching, with a second step at 1/3 of the power

- Bulk etch: C2F₆/CHF₃, 180 mTorr, 300 W, **xxx seconds (around 9 min)**
- Soft Land: C2F₆/CHF₃, 180 mTorr, 100 W, **xxx seconds (around 12 min)**

39. INSPECTION, ELECTRICAL MEASUREMENT, PROFILE CHECK

- **MICROSCOPE** inspection, no SiO₂ is allowed on channel electrodes
- **OHMETRE:** 2-needle measurement. Checking conductivity of channel electrodes (SiO₂ completely etched)
- **DEKTAK 9 PROFILOMETRE:** checking chamber and channel depth (should be 10µm)

40. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O₂ plasma, **program 1** (1000 watts, endpoint detection, 2 min overetching)

ETCHING OF THE SILICON OXIDE (SECOND STEP)

41. CLEANING: organics (HNO₃ 99%) **GREEN METALS CLEANING LINE**

- 10 minutes “**HNO₃ 99% (Si) room temperature**”. Carrier with YELLOW/GREEN DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with BLACK DOT

42. COATING

EVG 120: program “Co – 3027 – 3.1µm” COATING WITH THICK RESIST

- HDMS primer
- Spin coating AZ3027 positive resist
- Soft bake 95°C for 90 seconds
- Edge bead removal

43. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “**MASK2_MICROWELLS**”

- Energy Dose: 20s, 15mW/cm²
- Focus: 0

44. DEVELOPING

EVG 120: program “Dev – SP”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

Lab-On-Chip for Electrical Cytometry V2 – RUN NUMBER: EC2300

45. INSPECTION

Microscope inspection, no resist is allowed

46. PLASMA ETCHING: Etching away SiO₂ from inside chamber to realize wells

DRYTEK TRIODE 384T: recipe “**OXD_SFT_LND**”

Standard SiO₂ etching, with a second step at 1/3 of the power

- Bulk etch: C2F₆/CHF₃, 180 mTorr, 300 W, **xxx seconds (around 9 min)**
- Soft Land: C2F₆/CHF₃, 180 mTorr, 100 W, **xxx seconds (around 12 min)**

47. INSPECTION, ELECTRICAL MEASUREMENT, PROFILE CHECK

- **MICROSCOPE** inspection, no SiO₂ is allowed on well electrodes
- **OHMETRE:** 2-needle measurement. Checking conductivity of well electrodes (SiO₂ completely etched)
- **DEKTAK 9 PROFILOMETRE:** checking wells depth (should be 10µm)

48. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O₂ plasma, **program 1** (1000 watts, endpoint detection, 2 min overetching)

FINAL STEPS (OUTSIDE CLASS 100)

49. DICING

MEMS LAB dicing saw, 2cm spacing horizontal cuts, 1cm spacing vertical cuts

50. APPLYING THE LID TO SEAL THE DEVICE

Different options

1. Anodic bonding (or gluing) of a glass wafer on top, prior to dicing
2. Glass cover for smartphone? The tempered glass screen protector → tried, doesn't work
3. PDMS cover: dummy wafer as substrate, or even directly on chip



Uncured Polyimide Interaction with Acetone

Version: 1

Valid from: 1 September 2018

Made by: Federico Bedini

Run number: P3370

Process engineer: Federico Bedini

Mentor: Tom Scholtes

Start date processing: 1 September 2018

Estimated end date: 1 November 2018

Contamination: None

Labs: CR100

EKL(Else Kooi Laboratory)
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Fax : +31 - (0)15 - 2622163
Website : <http://ekl.tudelft.nl/EKL/Home.php>

Uncured Polyimide Interaction with Acetone– P3370

STARTING MATERIAL

Use **SILICON WAFERS, SINGLE SIDE POLISHED**

Type:	p/B (p-type, boron)
Orientation:	<100>
Resistivity:	2-5 Ω cm
Thickness:	525 \pm 15 μ m
Diameter:	100 mm
Number of wafer:	2

Background: Kind of process description about the device.

An important portion of the device will be realized with polyimide, a polymer whose properties are suitable for the realization of Lab-On-Chip devices. In our case, a negative photosensitive polyimide will be used. However, it is important to define the parameters for the cure, deposition, exposure and development of thick layers of polyimide, to obtain a thick, uniform layer. The behavior of the polyimide in acetone is studied (before cure). Another test is done to study the behaviour of several layers of polyimide one on top of the other, to understand how thickness is varied (if it expands or if it shrinks).

Uncured Polyimide Interaction with Acetone– P3370

ALIGNMENT MARKERS ON WAFERS

1. COATING

EVG 120: program “Co – 3012 – zero layer”

- HDMS primer
- Spin coating SPR3012 positive resist
- Soft bake 95°C for 90 seconds
- Edge bead removal

2. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “MASK0_MARKERS”

3. DEVELOPING

EVG 120: program “Dev – SP”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

4. INSPECTION

Microscope inspection, no resist is allowed

5. WAFER NUMBERING

Glass pen – WAFER NUMBER P1 – P2

6. PLASMA ETCHING: Etching the alignment markers on the wafer

TRIKON OMEGA 201: sequence “URK_NPD” (20°C platen)

- Breakthrough: CF4/O2, 5 mTorr, 10 seconds
- Bulk etch: Cl2/HBr, 60 mTorr, 40 seconds

7. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O2 plasma, **program 1** (1000 watts, endpoint detection, 2 min overetching)

POLYIMIDE

8. CLEANING: organics (HNO3 99%) and metals (HNO3 69.5%, 110°C)

- 10 minutes “HNO3 99% (Si) room temperature”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- 10 minutes “HNO3 69.5% 110C (Si)”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- Avenger Ultra-Pure rinse/dryer, standard program. Carrier with RED DOT

9. COATING

BREWER MANUAL SPINNER (polymer lab)

- 1st step:
- 2nd step:
- 3rd step:
- 4th step:
- ...

Uncured Polyimide Interaction with Acetone– P3370

10. SOFT BAKE

BREWER HOT PLATE (polymer lab)

- 1st step:
- 2nd step:
- 3rd step:
- 4th step:
- ...

11. MEASUREMENT: Polyimide thickness

DEKTAK?

12. COATING

BREWER MANUAL SPINNER (polymer lab)

- 1st step:
- 2nd step:
- 3rd step:
- 4th step:
- ...

13. SOFT BAKE

BREWER HOT PLATE (polymer lab)

- 1st step:
- 2nd step:
- 3rd step:
- 4th step:
- ...

14. MEASUREMENT: Polyimide thickness after second coating

DEKTAK?

15. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “MASK5_INLETOUTLET”

16. CROSSLINK BAKE

BREWER HOT PLATE (polymer lab)

- 1st step:
- 2nd step:
- 3rd step:
- 4th step:
- ...

17. DEVELOPMENT

MANUAL DEVELOPMENT: HTRD2 polymer lab FUMEHOOD and BREWER HOTPLATE

- 1st step: xxx
- 2nd step: xxx
- 3rd step: xxx
- 4th step: xxx
- ...

Uncured Polyimide Interaction with Acetone– P3370

18. MEASUREMENT: Polyimide thickness after development (reference before acetone)

DEKTAK?

19. ACETONE BATH

FUMEHOOD in polymer lab. **xxx minutes.**

20. INSPECTION

Did the acetone reacted with the polyimide? Did the polyimide detach from the surface?

21. MEASUREMENT: Polyimide thickness after acetone. Decreased thickness or not?

DEKTAK?

22. POLYIMIDE CURE

KOYO OVEN: recipe from previous results on thickness

23. MEASUREMENT: Polyimide thickness after cure (reference before acetone)

DEKTAK?

Doubts:

- How many time we coat and bake? How thickness is influenced?
- How much thickness is decreased after cure? (should be 45%)
- Acetone damages polyimide before cure?

Results: all the parameters to work with photosensitive polyimide will be obtained, thickness of the resulting film will be obtained, adhesion problems will be investigated. The initial wafer won't (shouldn't) be damaged by the process, it is possible to reuse it several times, even for the following problems.



Polyimide Interaction with Positive Photoresist

Version: 1

Valid from: 1 September 2018

Made by: Federico Bedini

Run number: P3371

Process engineer: Federico Bedini

Mentor: Tom Scholtes

Start date processing: 1 September 2018

Estimated end date: 1 November 2018

Contamination: None

Labs: CR100

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Polyimide Interaction with Positive Photoresist – P3371

STARTING MATERIAL

Use **SILICON WAFERS, SINGLE SIDE POLISHED**

Type:	p/B (p-type, boron)
Orientation:	<100>
Resistivity:	2-5 Ω cm
Thickness:	525 \pm 15 μ m
Diameter:	100 mm
Number of wafer:	2

Background: Kind of process description about the device.

In the last steps of the flowchart, we will need to work both with the polyimide (negative photoresist) and with a positive resist, to define a sacrificial structure below the polyimide. The process will involve the deposition and patterning of a thick layer of positive resist, to define the channel geometry, which will be covered by a thick layer of polyimide, that will be used as a lid, and will be patterned to create the inlet/outlet and the pads for the electrodes. Then the photoresist inside the channel will be etched away with acetone. The three main uncertainties related to this process are: 1) will the polyimide adhere well on the substrate, without bubbles, without mixing to the photoresist, without damaging or hardening too much the photoresist? 2) will the acetone bath also damage the polyimide? will it effectively remove the photoresist without damaging the overall design? 3) will features be respected during the photo steps? is it a problem to UV cure everything several times? how does the photoresist react during the development of the polyimide?

Polyimide Interaction with Positive Photoresist – P3371

ALIGNMENT MARKERS ON WAFERS

1. COATING

EVG 120: program “Co – 3012 – zero layer”

- HDMS primer
- Spin coating SPR3012 positive resist
- Soft bake 95°C for 90 seconds
- Edge bead removal

2. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “MASK0_MARKERS”

3. DEVELOPING

EVG 120: program “Dev – SP”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

4. INSPECTION

Microscope inspection, no resist is allowed

5. WAFER NUMBERING

Glass pen – WAFER NUMBER P3 – P4

6. PLASMA ETCHING: Etching the alignment markers on the wafer

TRIKON OMEGA 201: sequence “URK_NPD” (20°C platen)

- Breakthrough: CF4/O2, 5 mTorr, 10 seconds
- Bulk etch: Cl2/HBr, 60 mTorr, 40 seconds

7. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O2 plasma, **program 1** (1000 watts, endpoint detection, 2 min overetching)

PHOTORESIST

8. CLEANING: organics (HNO3 99%) and metals (HNO3 69.5%, 110°C)

- 10 minutes “HNO3 99% (Si) room temperature”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- 10 minutes “HNO3 69.5% 110C (Si)”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- Avenger Ultra-Pure rinse/dryer, standard program. Carrier with RED DOT

9. COATING

EVG 120: program “xxx” COATING WITH THICK RESIST (4um) SYRINCH?

- 1st step: xxx
- 2nd step: xxx
- 3rd step: xxx
- 4th step: xxx
- ...

Polyimide Interaction with Positive Photoresist – P3371

10. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “MASK4_MICROCHANNEL”

11. DEVELOPMENT

MANUAL DEVELOPMENT polymer lab FUMEHOOD and BREWER HOTPLATE

- 1st step: xxx
- 2nd step: xxx
- 3rd step: xxx
- 4th step: xxx
- ...

12. MEASUREMENT: Photoresist thickness

DEKTAK?

POLYIMIDE

13. COATING (Polyimide precursor)

BREWER MANUAL SPINNER (polymer lab)

- 1st step:
- 2nd step:
- 3rd step:
- 4th step:
- ...

14. SOFT BAKE

BREWER HOT PLATE (polymer lab)

- 1st step:
- 2nd step:
- 3rd step:
- 4th step:
- ...

15. REPEAT COATING AND BAKING on the basis of previous results

16. MEASUREMENT: Polyimide thickness

DEKTAK?

17. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “MASK5_INLETOUTLET”

18. CROSSLINK BAKE

BREWER HOT PLATE (polymer lab)

- 1st step:
- 2nd step:
- 3rd step:
- 4th step:
- ...

Polyimide Interaction with Positive Photoresist – P3371

19. DEVELOPMENT

MANUAL DEVELOPMENT: **HTRD2** polymer lab FUMEHOOD and BREWER HOTPLATE

- 1st step: xxx
- 2nd step: xxx
- 3rd step: xxx
- 4th step: xxx
- ...

20. ACETONE BATH

FUMEHOOD in polymer lab. **xxx minutes**.

21. INSPECTION

Did the acetone removed all the photoresist?

22. POLYIMIDE CURE

KOYO OVEN: recipe from previous results on thickness

Results: problems will arise, as the channel is 10x10 um, so maybe the acetone won't go inside the chip. Pump? Vibrations? Other techniques? Or maybe the photoresist will be so hard after all those bakes, that it won't be removed by acetone. In that case we could either try to lower time/temp of the bakes (and see if it's not a problem to have a softer polyimide before the acetone bath), then remove the photoresist, then do the hard bake without the photoresist, or we can also decide to go for another process (e.g. another carrier wafer with patterned polyimide, to bond it upside down on top of our wafer).



Thick PECVD Oxide Stress Measurement

Version: 1

Valid from: 1 September 2018

Made by: Federico Bedini

Run number: P3372

Process engineer: Federico Bedini

Mentor: Tom Scholtes

Start date processing: 1 September 2018

Estimated end date: 1 November 2018

Contamination: None

Labs: CR100

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Thick PECVD Oxide Stress Measurement – P3372

STARTING MATERIAL

Use **SILICON WAFERS, SINGLE SIDE POLISHED**

Type:	p/B (p-type, boron)
Orientation:	<100>
Resistivity:	2-5 Ω cm
Thickness:	525 \pm 15 μ m
Diameter:	100 mm
Number of wafer:	2

Background: Kind of process description about the device.

Description: the problem will arise if the deposition of Silicon Dioxide with the NOVELLUS PECVD machine is not stress-free. The deposited layer must be stress-free to avoid the bending of the wafer (or the breaking of a glass wafer), but also to avoid cracks in the SiO₂ itself. A bended wafer is not recognised by the machines, and cannot be processed anymore, while cracks in the oxide will interfere with the adhesion of the following layers and with the sealing of the device, nevertheless they will weaken the microchannel, which is not desirable as the system will be pressurized. Measuring the stress of a wafer before and after a long deposition will let us investigate the properties of this thick (>10 μ m) oxide film used as a passivation layer. Also the etching of this thick layer will be investigated, and to reduce the isotropy of the wells an half DRY half WET etching is performed.

Thick PECVD Oxide Stress Measurement – P3372

ALIGNMENT MARKERS ON WAFERS

1. COATING

EVG 120: program “Co – 3012 – zero layer”

- HDMS primer
- Spin coating SPR3012 positive resist
- Soft bake 95°C for 90 seconds
- Edge bead removal

2. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “MASK0_MARKERS”

3. DEVELOPING

EVG 120: program “Dev – SP”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

4. INSPECTION

Microscope inspection, no resist is allowed

5. WAFER NUMBERING

Glass pen – WAFER NUMBER P5 – P6

6. PLASMA ETCHING: Etching the alignment markers on the wafer

TRIKON OMEGA 201: sequence “URK_NPD” (20°C platen)

- Breakthrough: CF4/O₂, 5 mTorr, 10 seconds
- Bulk etch: Cl₂/HBr, 60 mTorr, 40 seconds

7. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O₂ plasma, **program 1** (1000 watts, endpoint detection, 2 min overetching)

SILICON OXIDE DEPOSITION

8. CLEANING: organics (HNO₃ 99%) and metals (HNO₃ 69.5%, 110°C)

- 10 minutes “HNO₃ 99% (Si) room temperature”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- 10 minutes “HNO₃ 69.5% 110C (Si)”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- Avenger Ultra-Pure rinse/dryer, standard program. Carrier with RED DOT

9. MEASUREMENT: SiO₂ stress, reference

TENCOR FLEXUS

10. PECVD DEPOSITION: 10um SiO₂

NOVELLUS CONCEPT ONE: recipe “xxx_siostd” (Variable time, on the basis of avg deposition time)
Eventually the deposition can be repeated two times, to obtain desired thickness

Thick PECVD Oxide Stress Measurement – P3372

11. MEASUREMENT: SiO₂ thickness

LEITZ MPV-SP: program “xxx”

12. MEASUREMENT: SiO₂ stress

TENCOR FLEXUS

ETCHING OF THE SILICON OXIDE

13. CLEANING: organics (HNO₃ 99%) and metals (HNO₃ 69.5%, 110°C)

- 10 minutes “**HNO₃ 99% (Si) room temperature**”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- 10 minutes “**HNO₃ 69.5% 110C (Si)**”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with RED DOT

14. COATING

EVG 120: program “xxx” COATING WITH THICK RESIST (4um)

- HDMS primer
- Spin coating SPR3012 positive resist
- Soft bake xxx
- Edge bead removal

15. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “**MASK3_MICROWELLS**”

16. DEVELOPING

EVG 120: program “**Dev – SP**”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

17. INSPECTION

Microscope inspection, no resist is allowed

18. PLASMA ETCHING: Etching away HALF of the SiO₂

DRYTEK TRIODE 384T: recipe “**STDOXIDE**”

- Bulk etch: C2F₆/CHF₃, 180 mTorr, 300 W, **xxx seconds**

19. MEASUREMENT: SiO₂ thickness IN THE WELLS

LEITZ MPV-SP: program “xxx”

20. WET ETCHING: Etching away OTHER HALF of the SiO₂

- 1 minute “**H₂O/Triton X-100**”. Carrier with BLUE DOT
- xxx minutes “**BHF 1:7**” (to be calculated on the basis of step 29). Carrier with BLUE DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with BLUE DOT

Thick PECVD Oxide Stress Measurement – P3372

21. MEASUREMENT: SiO₂ thickness IN THE WELLS

LEITZ MPV-SP: program “xxx” I DON’T WANT ANY SiO₂ RESIDUE

22. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O₂ plasma, **program 1** (1000 watts, endpoint detection, 2 min overetching)

Results: if everything went well, we obtain a wafer which is not bended, that is covered by a 10um layer of SiO₂, which is in turn patterned with wells. We could study under a microscope the dimensions of the wells, to understand if the underetch is too extended or if it is acceptable, if features are respected, if long etching creates problem to the photoresist.



Etching of Titanium Nitride in BHF Bath

Version: 1

Valid from: 1 September 2018

Made by: Federico Bedini

Run number: P3373

Process engineer: Federico Bedini

Mentor: Tom Scholtes

Start date processing: 1 September 2018

Estimated end date: 1 November 2018

Contamination: None

Labs: CR100

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Etching of Titanium Nitride in BHF Bath– P3373

STARTING MATERIAL

Use **SILICON WAFERS, SINGLE SIDE POLISHED**

Type:	p/B (p-type, boron)
Orientation:	<100>
Resistivity:	2-5 Ω cm
Thickness:	525 \pm 15 μ m
Diameter:	100 mm
Number of wafer:	2

Background: Kind of process description about the device.

Titanium Nitride is a ceramic, biocompatible material that has recently become popular as a substitute for gold in the production of electrodes. It has good mechanical and electrical qualities, and it is cleanroom compatible. From previous data we know that:

“40 nm TiN deposited at 50C has been tested in BHF 1:7. After 5 minutes no attack of the layer was observed. Layers deposited at 350C (standard) are expected to have better quality. Effects of longer exposure to BHF 1:7 are not known”.

As our process requires longer etching times under the BHF, further tests are needed.

Etching of Titanium Nitride in BHF Bath– P3373

1. WAFER NUMBERING

Glass pen – WAFER NUMBER **P7 – P8**

2. METALLIZATION: xxx nm TiN

TRIKON SIGMA 204 sputter coater. Recipe: “xxx”.

3. MEASUREMENT: TiN sheet resistance (reference)

4 POINT PROBE

4. BHF BATH

- 1 minute “**H2O/Triton X-100**”, Carrier with BLUE DOT
- xxx minutes “**BHF 1:7**” (to be calculated on the basis of step 29). Carrier with BLUE DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with BLUE DOT

5. MEASUREMENT: TiN sheet resistance

4 POINT PROBE

Results: the sheet resistance of the TiN film shouldn't change. If it increases, that means that the layer has decreased in thickness, which is not desirable.



RIE Selectivity of Titanium Nitride over Silicon Nitride

Version: 1

Valid from: 1 September 2018

Made by: Federico Bedini

Run number: P3374

Process engineer: Federico Bedini

Mentor: Tom Scholtes

Start date processing: 1 September 2018

Estimated end date: 1 November 2018

Contamination: None

Labs: CR100

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RIE Selectivity of Titanium Nitride over Silicon Nitride– P3374

STARTING MATERIAL

Use **SILICON WAFERS, SINGLE SIDE POLISHED**

Type:	p/B (p-type, boron)
Orientation:	<100>
Resistivity:	2-5 Ω cm
Thickness:	525 \pm 15 μ m
Diameter:	100 mm
Number of wafer:	2

Background: Kind of process description about the device.

Description: Titanium Nitride and Silicon Nitride are two hard ceramic materials, with different electrical properties. Titanium Nitride is considered conductive, while Silicon Nitride is definitely an insulator. In the process, Silicon Nitride is used to passivate the bulk Si wafer from the electrodes, and the Titanium Nitride is used in combination with Titanium in order to obtain electrodes which have good conductivity and excellent biocompatibility and resistance to corrosion. During the etching of the Titanium Nitride, the Silicon Nitride underneath could be damaged, since the recipe used by the RIE machine (TRIKON OMEGA used with HBr and Cl₂) to etch Titanium Nitride, also could damage Silicon Nitride, leading to shorts. This test is performed to understand how good the selectivity is between Titanium Nitride and Silicon Nitride, to avoid overetching of the Silicon Nitride protection layer.

RIE Selectivity of Titanium Nitride over Silicon Nitride– P3374

ALIGNMENT MARKERS ON WAFERS

1. COATING

EVG 120: program “Co – 3012 – zero layer”

- HDMS primer
- Spin coating SPR3012 positive resist
- Soft bake 95°C for 90 seconds
- Edge bead removal

2. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “MASK0_MARKERS”

3. DEVELOPING

EVG 120: program “Dev – SP”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

4. INSPECTION

Microscope inspection, no resist is allowed

5. WAFER NUMBERING

Glass pen – WAFER NUMBER P9 – P10

6. PLASMA ETCHING: Etching the alignment markers on the wafer

TRIKON OMEGA 201: sequence “URK_NPD” (20°C platen)

- Breakthrough: CF4/O2, 5 mTorr, 10 seconds
- Bulk etch: Cl2/HBr, 60 mTorr, 40 seconds

7. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O2 plasma, program 1 (1000 watts, endpoint detection, 2 min overetching)

ETCH STOP/PASSIVATION LAYER OF SILICON NITRIDE

8. CLEANING: organics (HNO3 99%) and metals (HNO3 69.5%, 110°C)

- 10 minutes “HNO3 99% (Si) room temperature”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- 10 minutes “HNO3 69.5% 110C (Si)”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- Avenger Ultra-Pure rinse/dryer, standard program. Carrier with RED DOT

9. LPCVD DEPOSITION: 200 nm SiN

FURNACE E2: Silicon Nitride. Program “StdSiN” (Variable time, calculate on the basis of avg deposition time)

10. MEASUREMENT: SiN thickness

LEITZ MPV-SP: program “lpcvd loSiN >50nm on Si”

RIE Selectivity of Titanium Nitride over Silicon Nitride– P3374

METALLIZATION

11. CLEANING: organics (HNO₃ 99%) and metals (HNO₃ 69.5%, 110°C)

- 10 minutes “**HNO₃ 99% (Si) room temperature**”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- 10 minutes “**HNO₃ 69.5% 110C (Si)**”. Carrier with RED DOT
- Rinse in Quick Dump Rinser, standard program until resistivity is 5 Mohm
- **Avenger Ultra-Pure** rinse/dryer, standard program. Carrier with RED DOT

12. METALLIZATION: stack of 40nm Ti and 200 nm TiN

TRIKON SIGMA 204 sputter coater. Recipe “**Ti40_TiN200_350C**”

- IMMEDIATELY AFTER CLEANING
- 1 dummy wafer before batch with recipe “**Trg_cln_Ti_350C**”
- 1 dummy wafer between every batch wafer with recipe “**Ti_in_between_350C**”

ETCHING

13. COATING

EVG 120: program “**Co – 3012 – 1,4um**”

- HDMS primer
- Spin coating SPR3012 positive resist
- Soft bake 95°C for 90 seconds
- Edge bead removal

14. ALIGNMENT/EXPOSURE

EVG 420: Contact Aligner – mask: “**MASK1_FIRSTELECTRODES**”

- Energy Dose: 7sec, 15mW/cm²
- Focus: 0

15. DEVELOPING

EVG 120: program “**Dev – SP**”

- Post exposure bake 115°C for 90 seconds
- Developing with MF322, single puddle process
- Hard bake 100°C for 90 seconds

16. INSPECTION

Microscope inspection, no resist is allowed

17. PLASMA ETCHING: Etching TiN

TRIKON OMEGA 201: sequence “**TiN300nm**” (25°C platen)

- Bulk etch: Cl₂/HBr, 60 mTorr, 80 seconds with Endpoint Detection (falling edge)
- Overetch: Cl₂/HBr, 60 mTorr, 25 seconds

MANUAL STOP OF RECIPE AT DIFFERENT TIME, TO SEE WHEN THE TiN IS COMPLETELY ETCHED AND WHEN THE SiN STARTS TO BE ETCHED, SINCE THERE IS NO ENDPOINT BETWEEN TiN / SiN

18. PHOTORESIST LAYER STRIPPING

TEPLA PLASMA 300: O₂ plasma, **program 1** (1000 watts, endpoint detection, 2 min overetching)

Appendix B

Photomasks

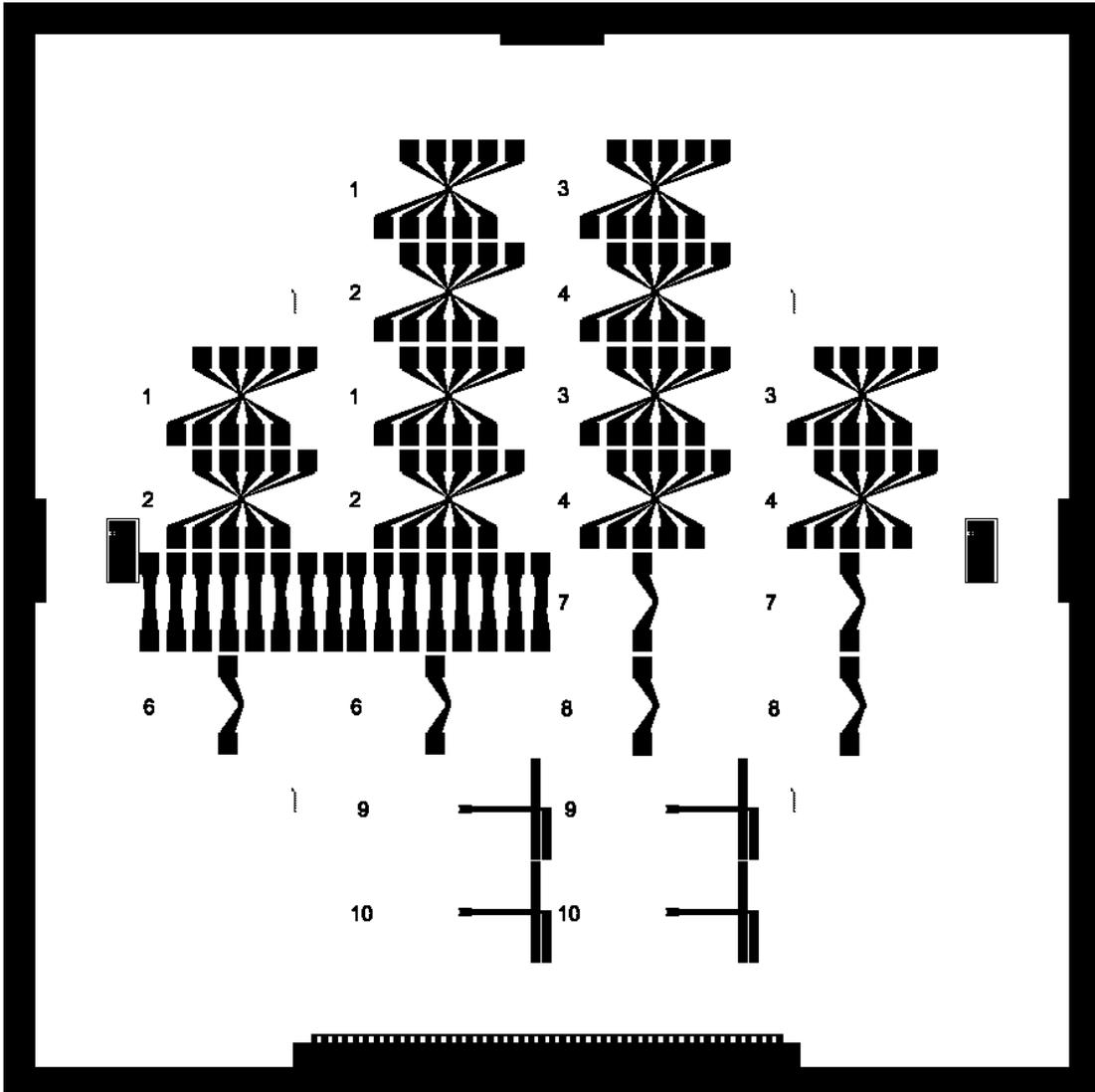


Figure B.1. Mask 1: First Electrodes

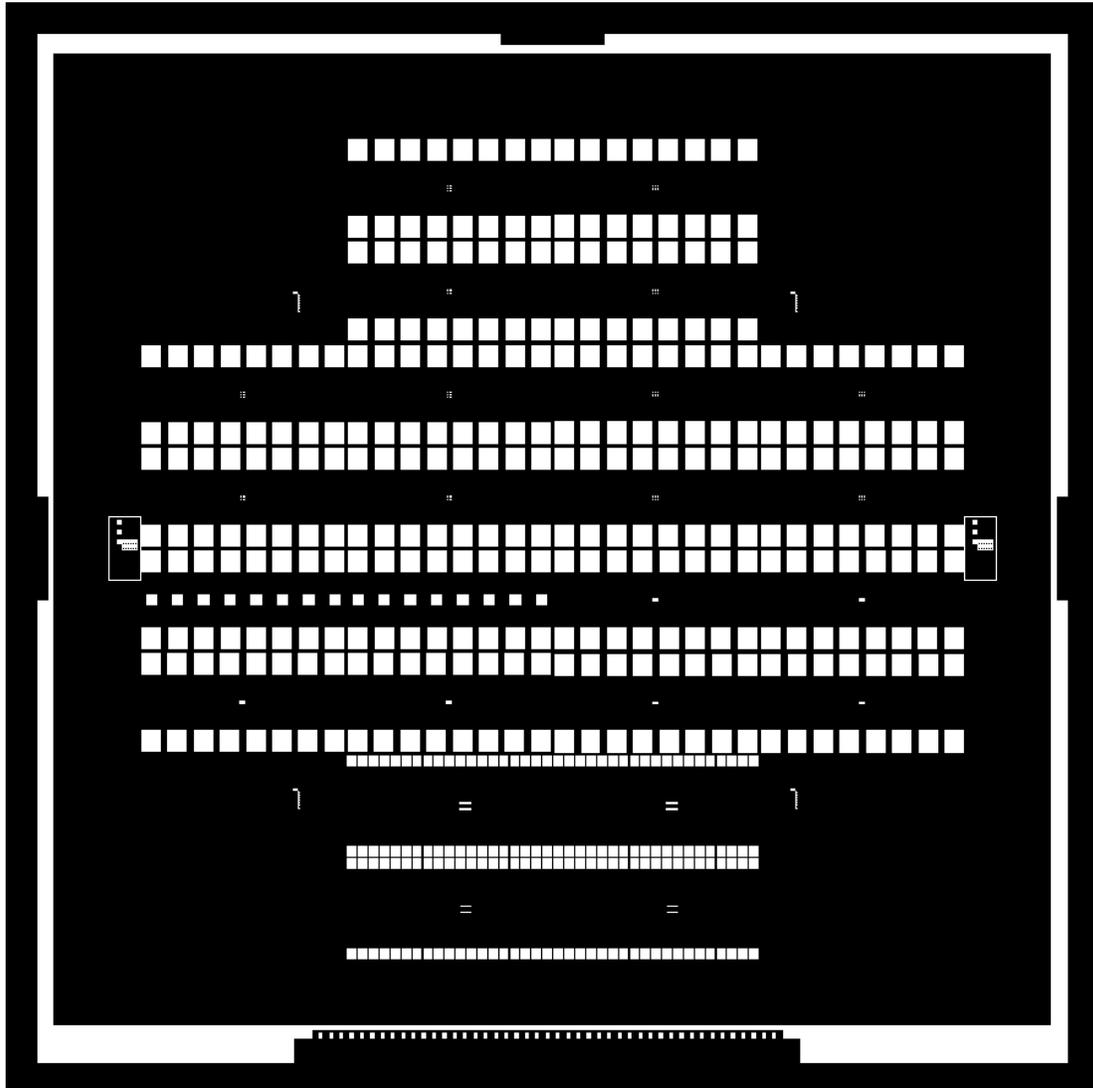


Figure B.2. Mask 2: Microwells

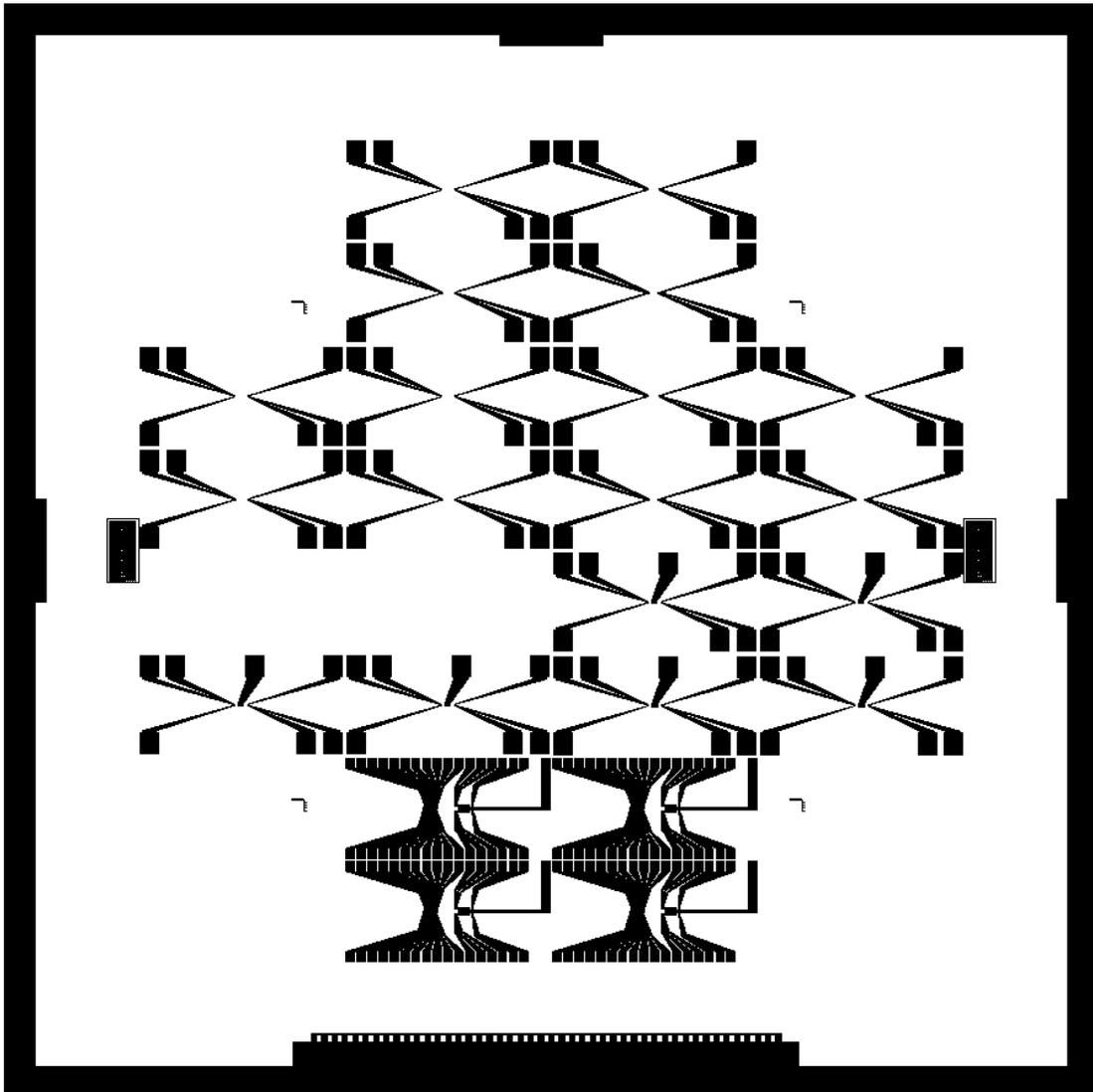


Figure B.3. Mask 3: Second Electrodes

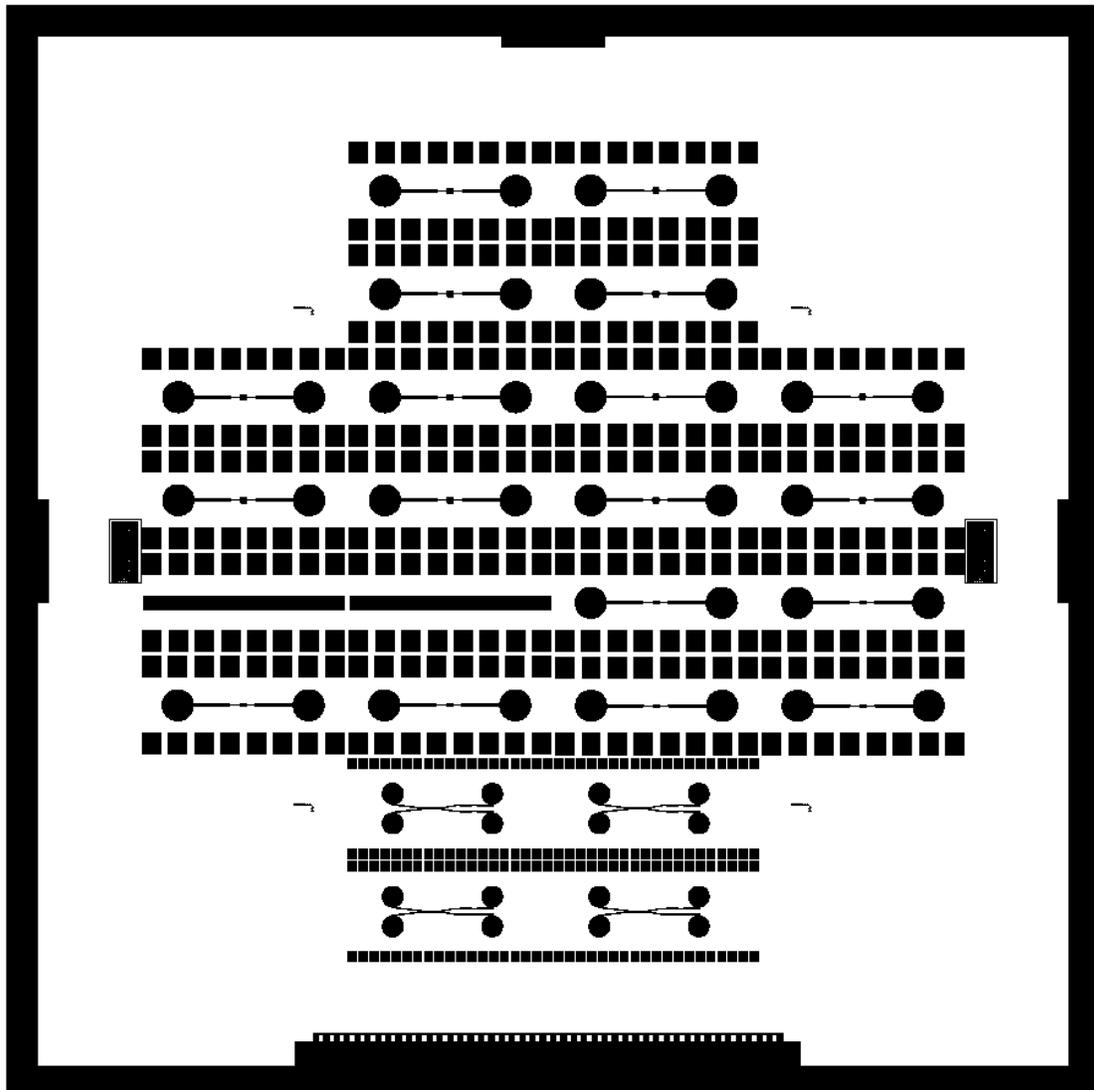


Figure B.4. Mask 4: Microchannel

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