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Evaluation of a new Si/SiGe Heterojunction Bipolar Transistor architecture in the 55 nm BiCMOS technology

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Sommario

BiCMOS055 di STMicroelectronics, una tecnologia BiCMOS nel nodo 55 nm, dimostra prestazioni senza eguali nei circuiti RF ed é la scelta per applicazioni allo stato dell'arte. BiCMOS055X intende migliorare queste capacità introducento la nuova architettura EXBIC per transistors bipolari. La nuova struttura presenta una epitassia del collettore intrinseco che permette di controllare precisamente la giunzione base-collettore e di intervenire liberamente sul collettore estrinseco impiantato nel substrato.

Oggetto di questo lavoro, la riduzione della capacità parassita base-collettore è ottenuta aggiungendo alla struttura un Super Shallow Trench Isolation (SSTI) e tramite lo studio di tecniche di drogaggio specifiche. La possibilità di poter integrare direttamente le proposte é studiata tramite l'ausilio di simulazioni TCAD ed esperimenti su Silicio. Si presentano diverse soluzioni e si forniscono ipotesi per una futura riproduzione su Silicio. Una nuova tecnica di drogaggio tramite co-impiantazione sviluppata appositamente per questi scopi ha dimostrato risultati interessanti ma necessita di una comprensione più profonda.

Abstract

BiCMOS055 from STMicroelectronics, a BiCMOS technology in the 55 nm node, shows unrivalled performances in RF circuits and is the choice for cutting-edge applications. BiCMOS055X aims to improve these capabilities by introducing the new EXBIC architecture for bipolar transistors. The new structure features an epitaxy of the intrinsic collector that allows to precisely control the base-collector junction properties and to play freely with the extrinsic collector implanted in the bulk.

Subject of this work, the reduction of parasitic base-collector capacitance is achieved by adding to the layout a Super Shallow Trench Isolation (SSTI) and by the study of specific doping techniques. The possibility to directly integrate the propositions is studied by the help of TCAD simulations and experiments on Silicon. Different solutions are presented and suggestions are given for future reproduction on Silicon. A new doping co-implantation technique introduced for this purpose is shown to have interesting results but needs deeper understanding.

The Erasmus+ program, funded by the European Union, defines the international spirit of interaction between Europeans and made this experience possible.

This work is part of a Double Degree exchange program between Politecnico di Torino and Grenoble INP - PHELMA. With the intention to offer a novel interesting and enriching experience abroad, prof. Davide Bucci (PHELMA) and prof. Fabrizio Pirri (PoliTo) have managed to reproduce for Nanotechnologies students what already exists for other fields of studies.

STMicroelectonics is a leader franco-italian enterprise amongst the biggest microelectronics world players with a strong focus in Research & Development. Participating in different european research projects such as TARANTO, it well represents the synergy between Italy and France in Europe.

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STMicroelectronics, known also as ST, was born in 1987 by the fusion of SGS Microelettronica and Thompson Semiconducteurs. It is the Europe's largest semiconductor chipmaker on revenue and a prominent player in the world semiconductor industry. Company's motto "life augmented" represents the mission of the group: wherever semiconductor technology can improve everyday life, ST is present.

The site of Crolles is one of the most important facilities of the company and hosts two production plants, namely Crolles 1 (200 mm) and Crolles 2 (300 mm), where more than 4000 employees participate in production and Research & Development activities. More than 17000 wafers per week are produced in this site bringing to the clients technologies like CMOS, Analog and Radio Frequency or image sensors.

Among all the groups involved in Research & Development, The Mixed Signal and BiCMOS team is the one in charge for the creation of different technologies involved essentially in high-frequency operations. Many people work in the team and intervene in the development of new technologies during different stages of its evolution, from the initial moments of the architecture design to the late industrialization process optimization. The objective is to offer to the final client a complete product that is ready to be used by circuit designers and be transferred to the main production line.

A strong interactivity between people with different backgrounds is necessary in order to approach the complex problems that arise during the development of new microelectronic technologies. All these competences are mixed in the Process Integration group, which is responsible for the early stages of development, when all the steps required for the creation of a new device need to be put together.

This environment has been hosting the progression of the present work under the supervision of Mr. Pascal Chevalier. The cooperation of many different engineers and experts has been relevant not only for the technical aspect of this work but also for the understanding of the complex environment behind a leading enterprise. Learning programs have been offered along the time, demonstrating a clear interest in the development of personal skills.

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Glossary

[Kinetic] Monte Carlo ([K]MC) Statistical simulation algorithms intended to reproduce a phenomenon from a probability distribution of the events. Kinetic Monte Carlo is normally associated to a more complex physic and statistic model. 14, 23

Ab-initio simulation Ab-initio simulations are computational methods based on quantum mechanics and relying only on physical constants. The absence of empirical parameters allows to easily simulate unknown structures but requires high calculation efforts and a strong physical model. 41

Algorithm Procedure for solving a mathematical problem in a finite number of steps that frequently involves repetition of an operation. [Merriam-Webster] v, 13–15

BiCMOS A technology integrating both Bipolar and CMOS circuits on the same wafer. ix, 2, 4–6, 17

BiCMOS055 A 55 nm BiCMOS technology developed by STMicroelectronics, basis of the present study. 5, 7, 10, 11, 17

BiCMOS055X A 55 nm BiCMOS technology developed by STMicroelectronics, context in which this study has been conducted. 8, 10, 51

Bipolar Junction Transistor (BJT) A type of junction transistor which has been dominant in older analogic and digital technologies. 2, 4

Calibration In TCAD simulation, the action of tuning some model parameters in order to have results matching the real phenomenon, thus ensuring predictability of next simulations. v, 15

Chemical Mechanical Polishing (CMP) A process used for planarizing and polishing a wafer. It uses mechanical abrasion along with chemical etching, resulting in a very good surface uniformity. 25, 44–46

Chemical Vapour Deposition (CVD) A deposition technique based on the decomposition of a precursor gas on a solid surface and the consequent deposition of the desired material. Many materials can be deposited by this technique. xii, 5, 6, 32

Complementary Metal Oxide Semiconductor (CMOS) A logic family based MOSFET devices, dominant in nowadays digital circuits. 2, 3, 6, 11

Deep Trench Isolation (DTI) Trench isolation few μm deep and in general far bigger than STI, it requires additional steps but ensures optimal isolation between devices. 6, 45

Double-Polysilicon Self-Aligned Selective Epitaxial Growth (DPSA-SEG) A particular process for creating HBTs, see page 2 for more informations. v, vii, xiv, 2, 4, 6–8, 34, 51

End Point Detection (EPD) Particular to etch process, detection of the moment when the etch needs to be stopped, generally when layers of different materials are stacked. Normally done by analysing in real time the etch by-product. 48

Epitaxial eXtrinsic Base Isolated from the Collector (EXBIC) SiGe Heterojunction Bipolar transistor (HBT) architecture, the name stands for stands for Epitaxial eXtrinsic Base isolated from the Collector v, vii, xii, 2, 8, 10, 11, 18, 19, 34, 51

Epitaxy Technique similar to Chemical Vapour Deposition (CVD), is generally used for Silicon growth on a crystalline Silicon surface, allowing a perfect lattice matching. It is possible to dope in-situ, with a sharp doping profile as result (see EXBIC). Selective epitaxy allows the growth only on specific surfaces, eliminating spurious growth on undesired structures. 6, 8, 18, 32

Extrinsic collector/base Collector/base portion not directly playing in the transistor effect. These parts are important because they still play a role as parasitics, potentially having a big impact on performance. 5, 6, 8, 10

Finite Elements Methods (FEM) Numerical simulation method consisting of splitting a continuum in discrete parts by a mesh, thus needing to simulate only in the nodes of the structure. 14

Focus Exposure Matrix (FEM) Photolithography instrument calibration for a specific process. It tunes the machine focus in order to ensure the best pattern reproduction. 48

Heterojunction Bipolar transistor (HBT) An improved version of the BJT based on heterojunctions. xii, 2–4, 9, 10, 12, 17, 51

High Aspect Ratio Process (HARP) Normally referred to a particular dielectric used for the filling of trenches. It is specially designed for an optimal penetration in the trench, escaping the formation of voids and bubbles. 26, 44

International Technology Roadmap for Semiconductors (ITRS) A set of documents produced by a group of semiconductor industry experts. These experts are representative of the sponsoring organisations which include the Semiconductor Industry Associations of the United States, Europe, Japan, South Korea and Taiwan. 4

Intrinsic collector/base Collector/base portion playing a direct role in the transistor effect. It is generally used to refer to the portion close to the p-n junctions and delimited by the emitter window width. 5, 6, 9

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) A modern field-effect transistor, dominant in the nowadays digital circuits for its superior performance in this field. 2, 3

Optical Proximity Correction (OPC) Photolithography enhancement technique for the compensation of image errors due to diffraction or process effects. 48

Photolithography Transfer of a pattern from a mask to the wafer by means of light exposition of a resin. 43, 45, 48

Physical model A physical model describes a phenomenon through formulas and equations and is intended to have predictive capabilities. Because of the complexity of some phenomena, it is possible to have

different models describing the same thing but with different degrees of precision or applicability. v, 13, 15

Process Flow Sequence of steps needed for producing a working device. See appendix B. 6, 12, 43, 45, 48

Process Of Reference (POR) When studying process variations, it is the standard process used for characteristics comparison and evaluation of the differences. 19, 40

Research and Development (R&D) In industry, work directed towards innovation of products and processes. 10, 11

Secondary Ion Mass Spectroscopy (SIMS) Destructive analysis of the atoms present in a bulk. Energetic high-mass ions are sent to the surface, detaching the bulk atoms; mass spectroscopy allows to identify the detached atoms. 34–40, 42

Selectively Implanted Collector (SIC) A collector implantation done by implanting through the emitter window and aiming to enhance control over the collector properties in the DPSA-SEG architecture. 6, 8, 18

Semiconductor fabrication plant Also called **fab** or **foundry**, is a factory where semiconductor processing is done. 12

Shallow Trench Isolation (STI) Vertical trench with a depth on the order of the hundreds od nanometers, used for electrical isolation between zones. vii, 6, 10, 11, 44–48

Short Loop Production of a portion of process flow in order to spare time and money when only a specific process or structure is important by the means of the experiment. See appendix B. 48

Snowplow Effect Dopants redistribution during the recrystallization of amorphous zones, i.e. Solid Phase Epitaxial Regrowth (SPER). The dopants are normally segregated around the crystalline-amorphous boundary and follow it during the process. xiv, 30

Solid Phase Epitaxial Regrowth (SPER) If amorphous silicon has been deposited on crystalline bulk, recrystallization may occur during thermal treatment following an epitaxial-like behaviour: the amorphous/crystalline

boundary gradually rises to the surface, often dragging dopants with it (snowplow effect). xiv, 30, 35, 37

Super Shallow Trench Isolation (SSTI) Vertical trench with a depth below 150 nm. v, vii, 10, 11, 17, 18, 20–28, 43–52

Technology Computer-Aided Design (TCAD) Design of semiconductor devices with the help of computer simulations. v–vii, xi, 8, 12, 13, 15, 17, 30, 34, 35, 37

Transient Enhanced Diffusion (TED) Particularly important for Boron and Phosphorus, consists in an enhanced diffusivity when Silicon self-interstitials are present, generally after ion implantation. vi, 30, 32–35

Transmission Electron Microscopy (TEM) A high-resolution technique based on the interaction (transmission) of an high-energy electron beam with the sample. Requires particular specimen preparation which may result in alteration/destruction. 40

Chapter 1

Introduction

1.1 History

Figure 1.1: Bardeen, Brattain and Shockley, discoverers of the transistor effect. (Picture by AT&T. Public domain.)

After its **invention in 1948** by **John Bardeen, William Shockley and Walter Brattain**, the **Bipolar Transistor** has become a milestone in the human history.

Celebrated with a **Nobel prize** to its inventors in 1956, it has rapidly substituted the thermionic valves thanks to its reduced dimensions and cost in addition to better performances. The invention of dedicated logic families, the amelioration of the production processes and the development of a reliable integrated circuit production process have paved the way to the modern electronics. In the meanwhile, the advancements in the construction of the MOSFET made the development of the CMOS logic possible, replacing the the bipolar-based logics thanks to its high noise immunity and low static power.

Nowadays, the a big part of digital circuits is based on the CMOS logics. The virtues that led to the domination of this technology, however, could not face all the strengths of the Bipolar Junction Transistor (BJT), which kept its superiority in the **High-Frequency applications**. The necessity of combining the CMOS logic capabilities with the RF BJT strengths in increasingly smaller devices, led to the development of **BiCMOS** technology.

In order to keep performances increase whilst having a **CMOS-process compatibility**, the structure of the original bipolar device has been radically changed (fig. 1.3):

- The transistor has become **heterojunction-based**, offering an increased base efficiency. It is then generally called **Heterojunction Bipolar transistor (HBT)** and uses a graded SiGe alloy for the base part, increasing the base efficiency by the means of band gap engineering. The graded profile creates an internal electric field that adds a drift contribution to the electron diffusion, also offering multiple degrees of freedom in terms of Germanium profile. A smaller yet important detail is that carbon is often added (SiGe:C base) for boron diffusion reduction.

- The original simple planar layout has become a more complex yet efficient vertical **Double-Polysilicon Self-Aligned Selective Epitaxial Growth (DPSA-SEG)** structure, likely to further transform in the **Epitaxial eXtrinsic Base isolated from the Collector (EXBIC)** architecture for next technologies. See section 1.3.1 and section 1.3.2 for further details.

- The **process flow** of a full-bipolar integrated circuit has been **adapted** to the constraints of a modern **CMOS-based platform**, leading to particular design choices. BiCMOS circuits offer the union of bipolar performances in power and analogic application with the well known

CMOS digital capabilities. These devices being very different, it is a big challenge to integrate them in the same wafer. Since on the final circuit there will be a majority of MOSFETs, it is more profitable to adapt HBT process to the former than to completely develop from scratch two different devices.

- The advancements in production techniques led to a **structure shrinkage** and to an increase of complexity in order to ensure higher integration density and performances. If for HBTs the structure found is the smallest possible, MOSFETs are often one or two nodes late with respect to the state of the art.

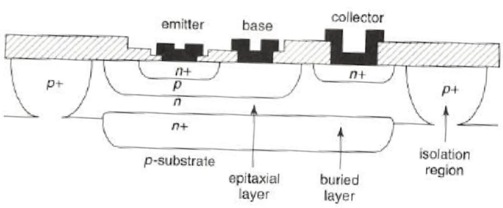


Figure 1.2: Diffused bipolar transistor, one of the first integrated bipolar structures. Picture from [1].

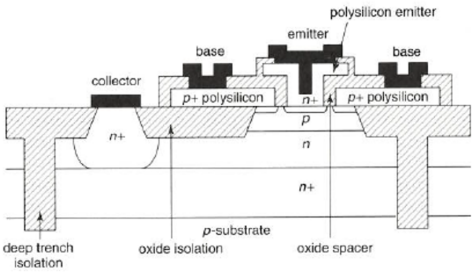


Figure 1.3: Double polysilicon self aligned transistor, a modern integrated structure. Picture from [1].

1.2 Industrial scenario

The challenge represented by the continuous demand for high-speed circuits has led to an increasing effort for obtaining HBTs that could outperform CMOS. Taking as an example the evolution of the mobile phone data rates, if in the '90s the GSM standard could deliver 9 kbit/s, in 2010 the 4G standard was designed for 1 Gbit/s data transmission. This is intended to be for one single mobile device. If we think about the infrastructure that makes telecommunications possible, such as Internet backbones, nowadays we may easily reach data rates of hundreds of gigabits.

Although this field represents a fundamental brick in telecommunications, it has been mainly used in high-end devices limiting the production volume

of BiCMOS with respect to other "mainstream" technologies. In this scenario, only the market leading companies could be competitive and able to offer extreme devices at remunerative levels. The capillarity of fibre optics communications and the introduction of 5G standard require a massive use of high-frequency devices, which will offer big production volumes to the producers of BiCMOS-based circuits.

In order to stimulate a high level in research and to keep companies competitive, the European Union has funded **several projects between european companies and universities**. **DOTFIVE, DOTSEVEN and TARANTO** projects represent the gathering of the major experts in BiCMOS technologies and are the context in which world records are continuously delivered. Enriching the idea of the International Technology Roadmap for Semiconductors (ITRS) consortium, companies do not only accord on results and forecasts but also work in strict collaboration like an extended research network. Once the projects are ended, each member may continue its individual research using the results and the acquired knowledge as a starting point.

Table 1.1: European projects for BiCMOS technologies, with respective years and targets

	DOTFIVE	DOTSEVEN	TARANTO
Years	2008 - 2011	2012 2016	2017 - 2020
Target	0.5 THz f_{MAX}	0.7 THz f_{MAX}	0.6 THz f_{MAX}; high-density BiCMOS

1.3 Technology overview

Because of the important changes done in the later years on the HBT architectures, an overview of the ideas and issues found will pose the basis for this work.

1.3.1 Double-Polysilicon Self-Aligned Selective Epitaxial Growth (DPSA-SEG) architecture

The Self Aligned structure has been first demonstrated by Ning et al. [12] (fig. 1.4) for a standard BJT with interesting possibilities to reduce the number of masks and increase precision in processes. The implementation of a complete DPSA-SEG structure for HBT has been reported by Sato et al. [17] (fig. 1.5) for an HBT architecture and has been demonstrated for a **300mm**

BiCMOS platform in Chevalier et al. [4], namely the **BiCMOS055 technology**.

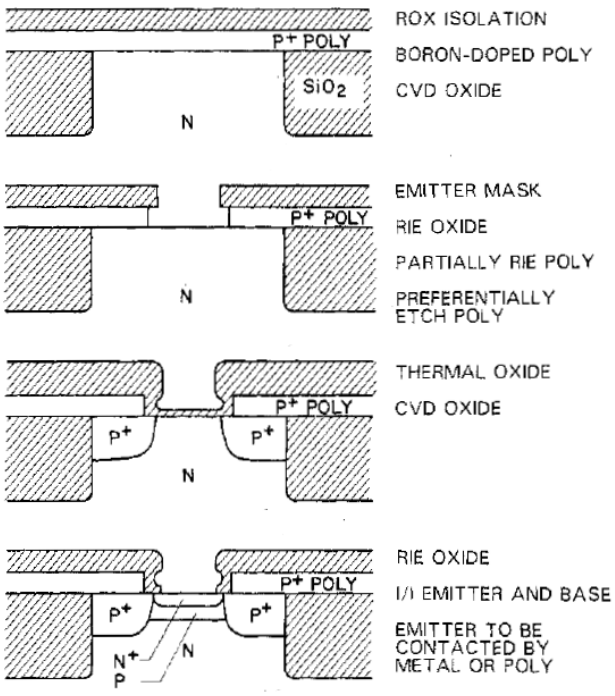


Figure 1.4: First example of Self-Aligned Bipolar Junction Transistor. Notice the absence of heterostructure and epitaxy for the base. Picture from [12].

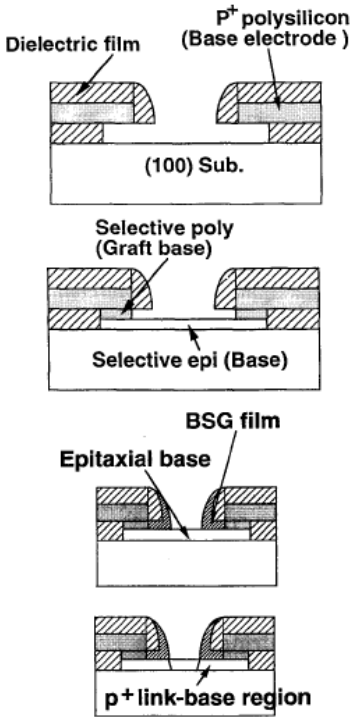


Figure 1.5: First example of a DPSA-SEG Heterojunction Bipolar Transistor. Picture from [17].

Self-alignment reduces the number of masks and cancels alignment tolerance, reducing the cost and enforcing process precision. As a side effect, design rules can result in more efficient circuits, which increase the overall performance. **Double polysilicon** means that emitter and extrinsic base are done by Chemical Vapour Deposition (CVD) of polysilicon, adding a degree of freedom since these parts are no more bound to the bulk. Moreover, polysilicon is capable of recrystallizing when baked in contact with Silicon, reducing resistance. Particularly in the case of the emitter, since the deposition is done on the base layer, the CVD results to depose a crystalline material. When dealing with the intrinsic-extrinsic base contact, The **selec-**

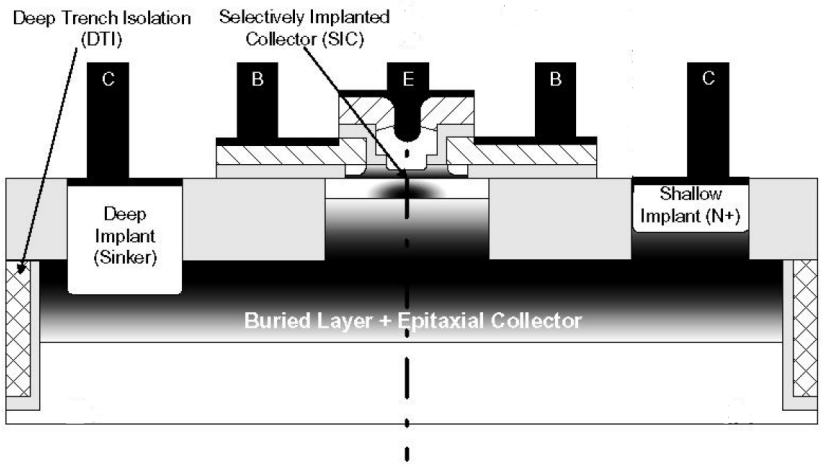
tive epitaxial growth refers to the capability of performing a deposition on a specific material, particularly important for the base epitaxy: spurious growth on undesired points is eliminated, which removes the need of additional etch or clean steps.

Looking at fig. 1.6a the DPSA-SEG process flow can be sketched:

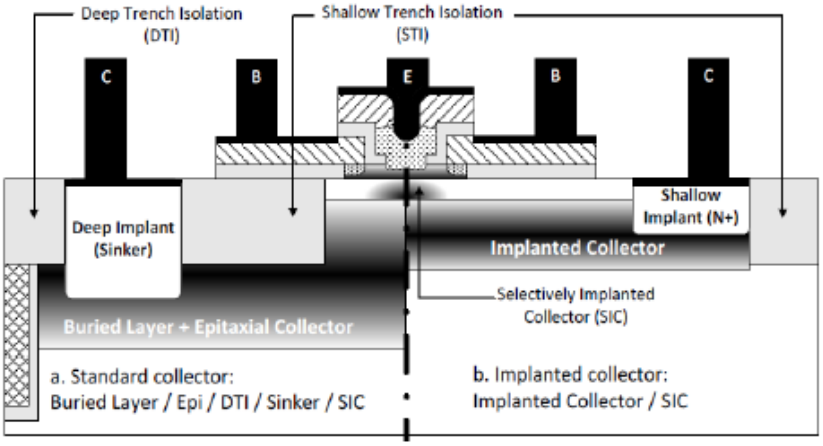
- A buried layer collector is doped before the epitaxial growth of a silicon layer.
- Trenches are created to isolate the devices from the neighbours (Deep Trench Isolation (DTI), Shallow Trench Isolation (STI)) or to reduce base-collector parasitic capacitance (STI).
- Different layers are deposited forming a stack, among them there is the extrinsic base polysilicon.
- The stack is patterned, forming the emitter window. This space is used as mask for Selectively Implanted Collector (SIC) doping.
- In the same window, the selective base epitaxy is done, creating the intrinsic base which contacts the previously deposed extrinsic base. epitaxy allows a graded SiGe profile, with Carbon and Boron as dopants. Different Germanium or doping profiles can be realized according to design choices.
- Emitter spacers are created and emitter is realized by CVD.
- Final patterning of the device.
- Whilst Sinker implant can be done during different moments of the flow, shallow implant is bound to the step of Source/Drain implant during the CMOS part of the process flow.

Presented by Geynet [7] for a 200mm platform and studied from Canderle [2] for the 300mm, the possibility of creating a low-cost version of the DPSA-SEG structure with fully implanted collector has been demonstrated by Gauthier et al. [6] (fig. 1.6b) with **record performances** for a BiCMOS platform. The implanted collector aims to dodge the need of an expensive collector epitaxy with relative isolation processes, i.e. DTI and central STI. The possibility for the implanted species to avoid the thermal budget of epitaxy and trenches bake allows a better control over diffusion and the use of

low-defectivity implants (see chapter 3). This mostly consists in a degradation of the base-collector parasitic capacitance but is capable to result, thanks to the reduced collector resistance, in an outstanding performance of 450 GHz f_T.



(a) Standard collector. Sinker implant vs Source/Drain implant.



(b) Standard collector vs implanted collector structures.

Figure 1.6: Different DPSA-SEG structures which can be derived from BiCMOS055 technology. Pictures from [3].

1.3.2 Epitaxial eXtrinsic Base isolated from the Collector (EXBIC) architecture

A completely new architecture is the EXBIC one. Firstly presented by Vu [20], consists in the **substitution of the SIC with an epitaxy** in the emitter window (fig. 1.7). The possibility to **dope in-situ** is a game changer because allows a sharp dopant profile without the creation of defects, permitting in turn to tune base-collector junction properties independently from the extrinsic collector.

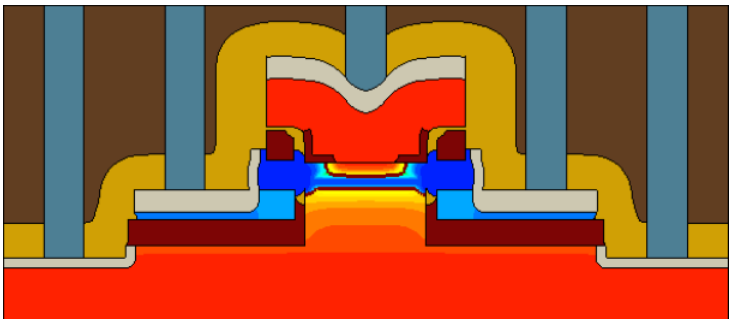


Figure 1.7: EXBIC structure from Technology Computer-Aided Design (TCAD) simulation. The zero level of Silicon is at the lower boundary of the oxide (brown).

Notice that, if the implanted collector structure is kept unchanged from fig. 1.6b, the part grown by epitaxy only has a small spacer separating it from the extrinsic base. Because of the absence of the additional collector steps found in the standard DPSA-SEG and the possibility to enhance control over the base-collector junction, this architecture is the one chosen for the future BiCMOS055X technology. **The present work is based on this architecture and aims to finally ameliorate the collector structure**.

1.4 Figures of Merit

When evaluating a technology, it is important to define some **figures of merit** useful to understand its capabilities in applications and to easily make comparisons between devices.

Assuming a clear knowledge in bipolar transistors technology, it is straightforward to pay particular attention on some parameters which are directly affected by the modifications of the collector structure:

- I_C, I_B, β, **Collector and Base current, Current gain**: define the device currents during operation and are important especially for the circuit design; there is not a particular attention to these parameters in this work since they are not directly dependent on the collector; some secondary effects, however, may impact on them;

$$I_C = \frac{qAD_{nb}n_i^2}{W_B N_{ab}} exp \frac{qV_{BE}}{kT} \tag{1.1}$$

$$I_B = \frac{qAD_{pe}n_i^2}{W_E N_{de}} exp \frac{qV_{BE}}{kT} \tag{1.2}$$

$$\beta = \frac{I_C}{I_B} \tag{1.3}$$

  Where q is the electron charge; A the junction area; D the diffusivity of electrons (n) or holes (p) in base (b) or emitter (e); n_i the intrinsic carrier density; W the width of base (B) or emitter (E); N the density of donors (d) or acceptors (a) in emitter (e) or base (b); V_{BE} the base-emitter voltage; k the Boltzmann constant; T the temperature.

- f_T, f_{MAX}, **Transit and Maximum Frequency**: are the ultimate index of the HBT characteristics, demonstrating the capability to fulfil the need for faster circuits; f_T is the frequency of the unitary current gain while f_{MAX} is the frequency of the unitary power gain;

$$f_T = \frac{1}{2\pi(\tau_F + R_C C_{jC} + \frac{k \cdot T}{qI_C}(C_{jE} + C_{jC}))} \tag{1.4}$$

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi C_{jC} R_B}} \tag{1.5}$$

  Where τ_F is the transit time in the device; C_{jC} and C_{jE} are the collector and the emitter junction capacitances.

  f_{MAX} is sometimes a difficult parameter to extract, particularly in simulations. When its value results problematic to obtain, observations on the variables found in its formula will however give clear indications on its behaviour.

- R_C**, Collector Resistance**: the doping and the length of the collector influence the resistance. Even if it is not accounted in the current equations, its contribution is represented by a parasitic resistance acting on them.

- C_{BC}**, Base-collector Capacitance**: which depends on the base-collector junction capacitance and on the parasitic capacitance between the extrinsic base and collector; the Super Shallow Trench Isolation (SSTI) structure is intended to reduce this parasitic.

- BV**, Breakdown Voltages**: in particular base-collector (BV_{CBO}) and collector-emitter (BV_{CEO}) voltages, which represent the capability of the device to withstand higher circuit voltages, very important especially in power applications.

- VAF**, Forward Early Voltage**: is linked to performance stability among different biases, giving a good insight in the junction effects which are easily affected by the changes in collector doping and is a matter of choice in circuit design.

1.5 Reasons of this study

In the context of **Process Integration Research and Development (R&D)** in **STMicroelectronics**, the development of a better-performing collector for EXBIC HBTs is held. This new design, part of the future **BiCMOS055X** technology, is a major update of the BiCMOS055 technology. Having a strong and direct impact on performance, the emitter and base parts are those who have been mostly studied and improved in the past. The **collector**, since it is placed in the bulk part of the structure, results more difficult to modify and presents the relatively lowest degree of structural complexity.

Once clear that EXBIC will be the architecture, questions on the possibility to **improve collector performance** rise. With the introduction of the implanted collector, whilst the process flow complexity has been reduced, the **base-collector parasitic capacitance** has increased due to the elimination of the STI under the extrinsic base. This, along with a consistent collector doping, has seen the parasitic grow oppositely to the collector resistance reduction. The resulting effect is the augmentation of the transit

frequency f_T and the strong reduction of f_{MAX}. The **parasitic** plays now a **fundamental role**, adding its contribution to the junction capacitance, which was until now the mostly impacting factor. Recalling eq. (1.4)

$$f_T = \frac{1}{2\pi(\tau_F + R_C C_{BC} + \frac{k \cdot T}{q I_C}(C_{jE} + C_{BC}))}$$

we see that even if the parasitic capacitance grows, its total contribution remains limited, particularly in the case of a low collector resistance. On the opposite, considering eq. (1.5)

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi C_{BC} R_B}}$$

, the strong impact of the base-collector parasitic capacitance is shown.

Gauthier et al. [6] have demonstrated the impact of high capacitance between base and collector extrinsic zones, highlighting a decrease of 100 GHz in an implanted collector with respect to the standard one of BiCMOS055. Following the first studies on the EXBIC [20], the increase in the pedestal oxide could resolve this problem. The necessity of CMOS integration on the same wafer leads to a particular **limit for the bipolar transistor height**, making more viable to develop the oxide thickness in the depth of the device rather than increase the pedestal oxide height. This led to the idea of **Super Shallow Trench Isolation (SSTI)**, which is intended to maintain the reduced complexity and the low resistance of the implanted collector adding the minimisation of the parasitics.
The main points of this study are therefore:

- **SSTI**: an STI process modified in order to attain shallower depths, offering a compromise between the up- and downsides of standard EXBIC and implanted collectors;
- **Ion implantation optimized for this architecture**: along with advancements in implantation techniques, the modified structure requires an *ad hoc* recipe in order to exploit the best performance possible. An adequate doping along all the electrons path is fundamental for ensuring performance.

These points require, in the industrial R&D context, to understand the phenomena and to have repeatable and predictable results. This means to add two preliminary objectives:

- **TCAD model for process simulation**: predictive and precise simulations are a very powerful tool, allowing to avoid time- and money-expensive experiments;

- **Ion implantation mastery**: in order to adapt this process to our architecture, it is necessary to know strengths and weaknesses of what we can do, eventually developing other techniques.

1.6 Instruments - TCAD simulations

Present in all engineering fields, Computer-Aided Design (CAD) software allows to modelize and predict the effects of design choices. Becoming increasingly expensive and time-consuming to realize prototypes along with more complex phenomena and devices, the calculation power of modern computers allows to reduce design costs and to have a clear understanding of the impact of design choices.

Specially designed for electronics, **Technology Computer-Aided Design (TCAD)** softwares allow to simulate the complete flow of device fabrication and the electrical performances of a such defined structure. With a proper coding of the models of physical laws playing a role in the represented processes, we can reproduce what we would normally obtain in fab with real instruments.

During this study, TCAD has been the preferred instrument for analysing the possible solutions thanks to its advantages with respect to Silicon trials. When a clear solution to a problem is offered, the reproduction of the structure on Silicon allows to validate the results and serves as feedback for a better simulation.

The software used for simulations is the **Synopsis Sentaurus** suite, which allowed to create **2D simulations** of the structure through the coding of the process flow and use of the masks created for the fab operations. When dealing with specific processes, **1D simulations** have been done; this is the case of the tuning of implantation or diffusion profiles, where reducing the complexity of simulations allows to save time.

In fig. 1.8 an example of how a generic HBT structure simulated with this software looks.

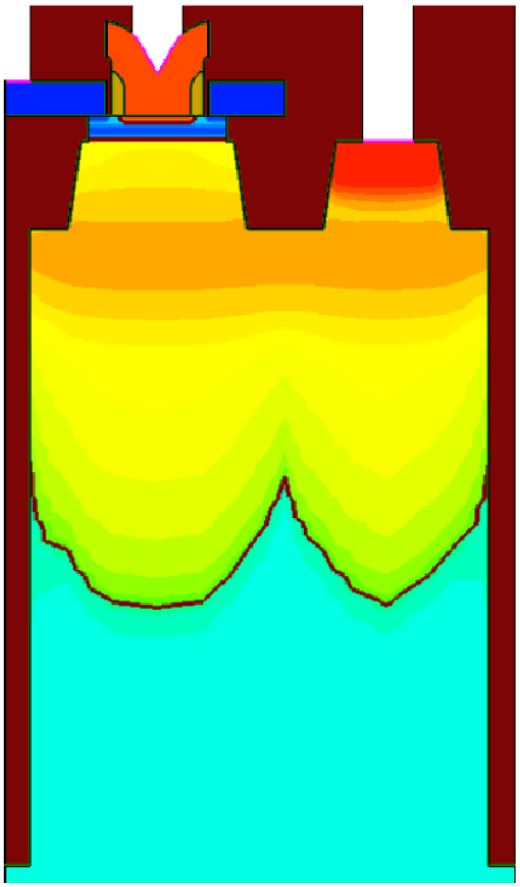


Figure 1.8: Example of a bipolar device simulated with Sentaurus.

1.6.1 Models and algorithms

Synopsis Sentaurus offers a suite of **physical models** useful in semiconductor simulations which can be enchained in a **full process flow** following a coded sequence of operations.

The choice of the model relies on the user and depends on **accuracy and time** required for the simulation. It is obvious that more precise results are always better but, in some cases, elapsed time is more important than strictly accurate results. As rule of thumb, a more precise model relies on higher degrees of complexity, requiring in turn more computation time. The limit of tolerable inaccuracy is to be set case by case depending on the criticality of the process.

Along with the specific model representing a phenomenon, **computation algorithm** plays a crucial role in the time-accuracy trade-off. In practice, the starting state of the device is taken and physical laws from the chosen model are applied through algorithm in order to have as a result the state of the device after the physical process. It is possible to distinguish three main kinds of algorithms:

- **Analytic**: uses macroscopic analytic laws based on experimental data which are tabulated; the required time is minimum but the precision of the results may not be high especially when dealing with certain complex processes. Taking a physical quantity in the simulation, it simply applies a formula from the model giving the resulting value as output;

- **Monte Carlo (MC)**: uses a probabilistic-based model which still relies on analytic laws but admits oscillations on some values which are chosen following a probabilistic distribution; this means generally a better accuracy since the final values are averaged but needs an higher computation time in order to reproduce multiple times the process;

- **Kinetic Monte Carlo (KMC)**: is an improvement of the Monte Carlo method which intends to evaluate the time evolution of the process (parameters variation, etc.); generally this model is used for a microscopic treatment of the phenomenon in order to be more accurate, resulting in an extremely increased amount of elaboration time;

Another important parameter, which is not necessarily linked to the physical phenomena involved, is the **meshing** of the structure. Since the simulations essentially rely on Finite Elements Methods (FEM), the device is discretized and the actual values describing it are stored in particular points which are the knots of the mesh. A denser mesh allows better precision but requires to compute the equations in more points. When small structures are present, e.g. thin base, an adequate meshing is essential for the correct simulation of the phenomena. The possibility of changing the mesh density in some particular areas allows to keep an adequate precision in all points while ensuring limited computation effort.

The final approach when setting up the simulation is:

1. **Choose an appropriate model** for the treated phenomenon, trying to consider its strengths and weaknesses. The algorithm may be directly determined by this choice.

2. **Set the algorithm** according to the chosen model and the desired accuracy.

3. **Set the mesh** depending on the structure. Adaptive meshing may be used, meaning that the mesh will be modified whenever an important modification is done.

4. If the simulation gives unrealistic results or the obtained precision is not satisfying, restart from the beginning by selecting more precise model, algorithm or mesh. **Calibration** may be needed.

1.6.2 Calibration

Since all the models and methods require some **external parameters** in order to work, the availability of process data determines the possibility to reproduce accurately the operations done on the device. Once the physical model has been chosen, it is necessary to match the external parameters of our model in order to be able to forecast the results in different conditions. This process is called **calibration**. With good knowledge of the used model, it is possible to tune some parameters trying to match the simulation results with the experimental results. If the found parameters are adherent to the reality of the same process in other conditions, the calibration is considered accurate. A good calibration ensures the accuracy of the simulation results.

Commercial software like Synopsis Sentaurus, offers most of the parameters needed for a simulation, e.g. constants, material properties, atomic interactions. When something new is introduced, the conditions used for the extraction of these parameters may not be valid anymore, requiring calibration to be done. See section 3.3 for an example of calibration.

Chapter 2

Collector process flow

Along with the major improvements in the HBT architecture, the collector has encountered different modifications, reaching the actual BiCMOS055 version. After the recent improvements in HBT integration, an optimization of the collector has become necessary. Its impact is present in all the principal figures of merit and, at this stage of the bipolar transistor evolution in BiCMOS technologies, it may be determinant.

Previous studies in PhD works [2, 20] have clearly shown the interest of the collector improvement and are the basis for this work. The overall idea is to implement an SSTI structure in an **implanted collector**, where the implantation technique is adapted to the thermal budget and topography constraints. In order to identify the best solution, TCAD simulations will be the main instrument.

Briefly recalling the nomenclature, collector is conceptually separated in **intrinsic** and **extrinsic** zones. The intrinsic part plays on the transistor effects directly and is the part placed right under the base in a range intended to be acting on the junction effects. The extrinsic part is the rest of the collector linking the intrinsic zone to the contacts and plays directly on some parameters and indirectly on others through parasitics.

Referring to section 1.5, the **main parameters** that impact on the final f_T/f_{MAX} performance are the **collector resistance** R_C and the **base-collector parasitic capacitance** C_{BC}. A first study on the **collector epitaxy** an on its impact on the junction effects is done in section 2.1; this will ensure that this part alone characterizes the intrinsic collector and remark its optimization. In section 2.2 the backbone of this work is discussed, inquiring on different proposed solutions for the **implanted collector** in the process

flow order and on the SSTI depth; this constitutes the optimization of the extrinsic collector. In section 2.3 all the considerations are put together to propose a solution to the collector optimization problem.

Specific studies on doping technique and SSTI integration are presented in chapter 3 and chapter 4 respectively. Their results will be used in this chapter with no further considerations.

2.1 Study on collector epitaxy

Collector epitaxy represents the strength of the EXBIC architecture, allowing to decouple the effects related to the base-collector junction from the rest of the collector. This is a major improvement because epitaxy allows in-situ doping, which results in a very sharp profile. The dopant specie used in this case is Arsenic, thanks to the defect-free lattice created with this technique. Using a **two-step doping**, the actual architecture can control the **depletion zone** formed at the **base-collector interface**: the concentration present in the first part of the collector is orders of magnitude smaller than the Boron in the base, resulting in a depletion almost completely confined in the collector. This reduces the base-collector junction capacitance and sets to a high value the Forward Early Voltage (VAF). The underlying collector layer, on the opposite, is strongly doped. This has two effects: if a small portion of this zone is depleted, the depletion zone will move only slightly under bias, further stabilizing the junction effects; the high dose reduces drastically the resistance of the undepleted zone, akin to what is done with the SIC.

An early study has been done by Vu [20] on the impact of different doses and thicknesses of the two layers. Since some modifications have been done to the original EXBIC structure, namely in the part of the flow after collector epitaxy, this study has been done again in order to verify that the values found are still valuable.

Vu [20] studied an epitaxied collector of generic height t_0 subdivided into a high-Arsenic zone of height t_1 and dose d_1 and a low-Arsenic zone of height t_2 and dose d_2. Effects have been analyzed for three values of t_1, namely 2/5, 3/5 or 4/5 of height t_0.

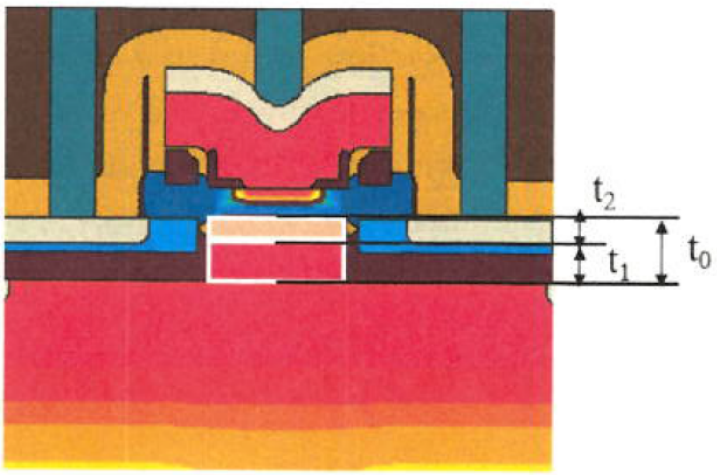


Figure 2.1: Collector epitaxy from [20].

The studies have been repeated with the following scheme:

- Arsenic dose of d_3 and d_4 ($> d_3$) for the high-dose part, d_2 unmodified for the low-dose part.
- Height of the high-dose part (t_1) equal to 1/3, 2/5, 3/5 and 2/3 of t_0.

Results may be found in table 2.1. The **Process Of Reference (POR)** represented by the d_3 $3/5t_0$ epitaxy already shows a **good balance** over the parameters. As it was explained, this process determines the junction properties. An increase up to 20 GHz is possible for f_T but it costs enormously in terms of loss in Breakdown Voltage. On the other side, a more robust collector involves a degradation in the frequency performance, determining a loss over 30 GHz. The tendency shown in the previous study is however confirmed: there is **not an absolutely preferable configuration**, which means that is should be chosen depending on the final use of the device. The differences with [20] in terms of performances and topology are due to some modifications in the EXBIC architecture that have been introduced in the meanwhile and which are not treated in this work.

The present analysis confirms the **good design** of the POR and highlights a certain limit in the amelioration of the performances. Wier et al. [21] showed the opportunities offered by the improvements of the collector structure by the use of so-called **superjunctions**: multiple layers of p- and

n-doped Silicon allow to enhance the base-collector junction properties, offering performance improvement. The difficulty to create this structures with implantation and diffusion could be overcome by the means of epitaxy, thanks to the possibility of in-situ doping.

Table 2.1: Resulting figures of merit from the variations on collector epitaxy, based on simulations.

	d_3 $1/3t_0$	d_3 $2/5t_0$	d_3 $3/5t_0$	d_3 $2/3t_0$
f_T (GHz)	419	435	452	462
BV_{ceo} (V)	1.47	1.44	1.32	1.14
VAF (V)	44	34	26	21
C_{bc} (fF)	1.21	1.30	1.42	1.52
	d_4 $1/3t_0$	d_4 $2/5t_0$	d_4 $3/5t_0$	d_4 $2/3t_0$
f_T (GHz)	438	454	468	475
BV_{ceo} (V)	1.44	1.38	1.19	0.96
VAF (V)	37	28	24	16
C_{bc} (fF)	1.26	1.37	1.52	1.62

2.2 Steps order in the collector process flow

Once stated the influence of the only epitaxial part of the collector on the junction properties, it is time to intervene on the **bulk** part by adding the SSTIs. As stated earlier in section 1.5, the interest in the increase of the oxide thickness isolating the extrinsic base from the collector has clear advantages. While the modification of the pedestal oxide would only require to tune the parameters of the emitter stack deposition, the **addition of a brick** for the **SSTI** demands a more elaborated work both for the trench creation and the substrate doping.

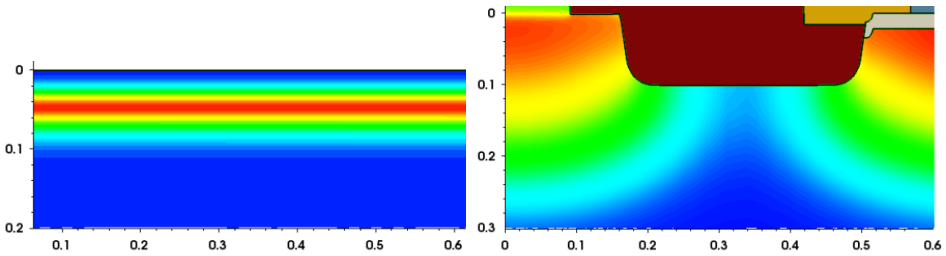
Among the advantages represented by the limitation of parasitics, the presence of the **additional steps** pose some problems. The thermal budget of the bake needed to stabilize the fill oxide is an obstacle, since it is capable to greatly diffuse dopants, i.e. it lowers the control over the doping profile. A second obstacle is represented by the structure itself: since the trenches go down in the extrinsic collector, an optimum has to be found between the reduced parasitic capacitance and the increased resistance introduced by elongating the electron path in the collector.

Layout-only simulations show that the **collector resistance** can be reduced to a value **lower than 50** Ω whilst keeping base-collector parasitic capacitance under acceptable levels. The interest in reproducing these structures is clear.

Four ideas involving dopant implantation are presented:

1. Doping in all the active bipolar area before SSTI etching.
2. Doping in all the active bipolar area after SSTI etch and before the gap filling.
3. Doping in all the active bipolar area after SSTI etch and after the gap filling.
4. Doping in sinker and intrinsic collector areas after SSTI etch and after the gap filling.

2.2.1 Doping in all the active bipolar area before SSTI etching.



(a) Doping profile before SSTI etch. (b) Doping profile after SSTI bake.

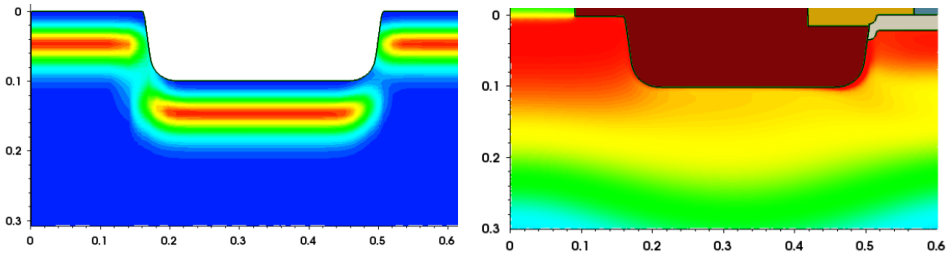
Figure 2.2: Arsenic doping profile in the "before SSTI" flow.

This technique is the **simplest** one, with the minimum of process steps and the most predictable result.

Presence of dopants in the volume to be etched influences the etch rate up to 10%, possibly giving a final depth dependent on the dose and energy used. Moreover, the implant should be close enough to the surface in order to ensure an adequate minimum dose along all the electron path. This practically means that the most of the dopants are within the SSTI depth range, with

the results of completely removing the ions (fig. 2.2). Finally, the **high thermal budget** will result in a **very high diffusion**, meaning an over diffused doping, see ineffective for our means.

2.2.2 Doping in all the active bipolar area after SSTI etch and before the gap filling.



(a) Doping profile after SSTI etching before filling.

(b) Doping profile after SSTI filling and baking.

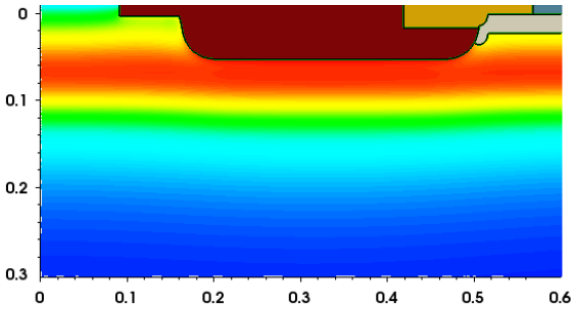
Figure 2.3: Arsenic doping profile in the "before SSTI filling" flow.

This technique is similar to the previous one with the implantation done right after the etch of the SSTI and before its filling. The idea is to produce a **profile** that retraces the **trench border**, resulting in an optimal doping along the electrons path.

Among all the techniques presented, this one offers in **theory** the **best configuration** possible. The main **obstacle** is represented by the dielectric **bake** that is done right after the gap fill, which makes the dopants diffuse enormously. Arsenic would be preferable in this case but the defects introduced by implanting this ion (section 3.2) may degrade the electric performances and it still diffuses too much. Using a carbon-phosphorous process still results ineffective because the thermal budget would still be able to move the dopants making them ineffective. If As+F co-implantation is confirmed to avoid or reduce these defects, it could enable this technique to be used.

2.2.3 Doping in all the active bipolar area after SSTI filling.

Trying to approach the optimal profile and **avoid initial diffusion**, the implantation may be done once the SSTI brick is complete. By implanting



(a) Implantation profile after SSTI filling. Analytic simulation.

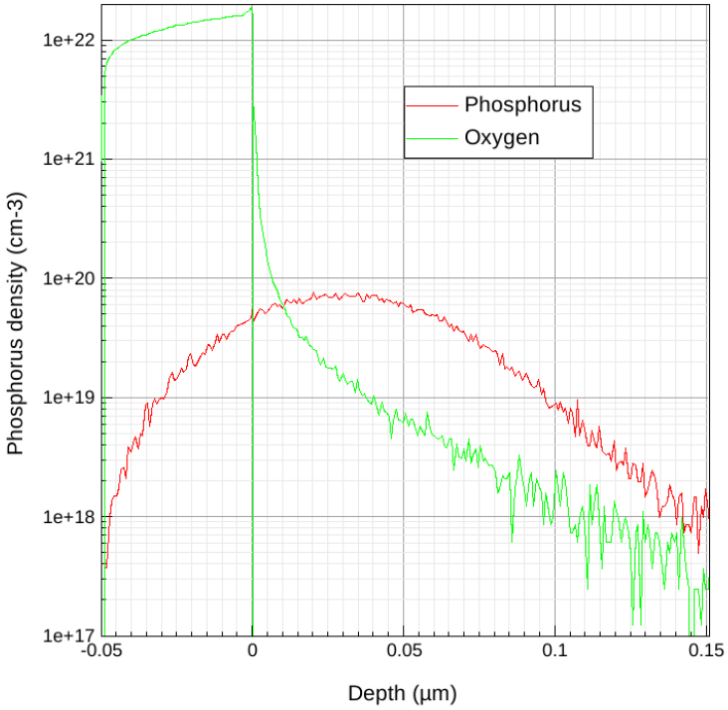
Figure 2.4: Simulation for the "after SSTI filling" flow. SSTI 50 nm deep.

on the whole bipolar area, the **ions** would either directly meet the silicon or **pass through the oxide** before reaching it.

If the dielectric does not interact too much with the dopants, the resulting profile should be close enough to the ideal one (fig. 2.4a). Actually, the ions-oxide interaction may be the main limiting factor of this technique: oxygen ions may be transferred to the silicon substrate, generating impurities that could originate oxidation, clustering effects or simply degrading the lattice, with the final result of increased electric resistance. Another phenomenon that may be observed at the oxide-silicon interface is actually the blurring of this border, with an unknown impact on the actual trench depth or the possibility of oxidation of this zone during thermal treatments.

Studies on the SSTI depth by KMC simulations show that the **penetration** of dopants through the oxide is **critically dependent on the trench depth**: the stopping power appears to be enough to stop more than half of the phosphorous of a standard recipe with only 50 nm of thickness. Remember that implants at higher energies would produce too deep profiles in the zones around them. By now, this represents the main problem linked to the SSTI depth.

When using a KMC simulation to study the Carbon + Phosphorus profiles positioning in this case, the results are not as satisfying as in the analytical model (fig. 2.4b). First of all, the dielectric has a stopping power that prevents the good positioning of the dopants: the Phosphorus peak is placed within the SSTI boundary leading to an ineffective Silicon doping. Moreover, the Oxygen quantity brought to the first nanometers of substrate is in the



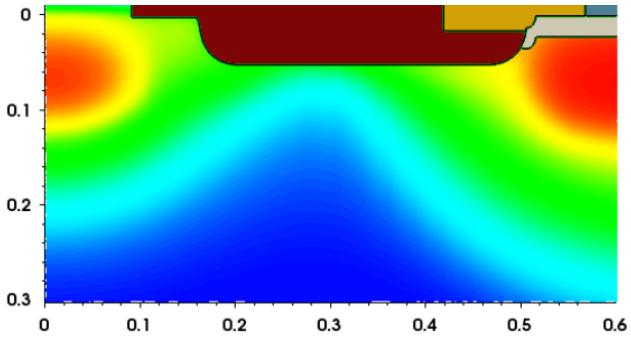
(b) Vertical implantation profile through SSTI after filling. C+P KMC simulation

Figure 2.4: Simulation for the "after SSTI filling" flow. SSTI 50 nm deep.

order of magnitude of the implanted dose. Such a high **concentration of Oxygen** has **unknown effects**, needing an analysis on a real device for a complete evaluation. Notice that the energies simulated are those that could attain an optimal depth when implanting in plain Silicon. The implantation energies could be increased in order to have a deeper implant and **correctly place the maximum under SSTI**; this would require a shallower implant for the no-SSTI zones.

2.2.4 Doping in sinker and intrinsic collector areas after SSTI etching and after the gap filling.

A variation of the previous idea, aiming to **avoid any interaction with the SSTI dielectric**, is to implant only where there is silicon on surface, i.e. avoiding to implant through the oxide (fig. 2.5a). In this case, the



(a) Phosphorus profile at the end of flow. Doping profile along the green line displayed in fig. 2.5b.

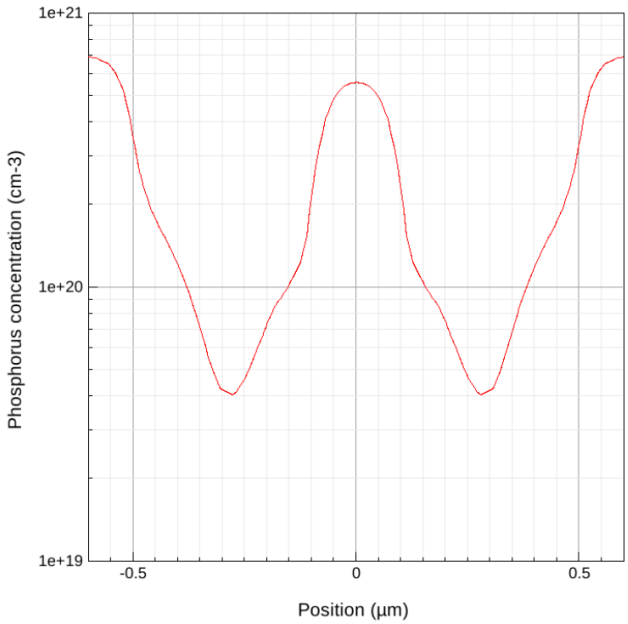
Figure 2.5: Result of a full-P implantation around the SSTI and whole process flow thermal budget.

implant has been done right after the SSTI Chemical Mechanical Polishing (CMP) with a photolithographic resin patterning for masking the ions and with only phosphorus as dopant. This means that a **specific mask** has to be practically designed (a fictitious mix between "emitter window" and "sinker" masks has been done for the simulation) and that **the process won't be auto-aligned**. This adds an extra mask and the possibility of misalignment.

About the **SSTI depth**, an **optimum** is found for **50 nm** of depth. This is greatly influenced by the depth reached by the implant with respect to the trench thickness: deeper implants reduce the base-collector parasitic capacitance and keep an adequate collector resistance. A double implantation with different energies could allow deeper trenches while keeping an adequate resistance.

The **advantage** of this technique, however, is that the eventual **oxygen-related problems** are **avoided** along with the thermal budget. The limit is that the sub-SSTI doping relies on a **controlled diffusion** from the sides based on the successive thermal treatments, eventually resulting in a sub-optimal dose. fig. 2.5b shows that there is about one decade and half of dose difference between the implanted and the diffused zones; the difficulty is to reach a sufficient concentration without increasing too much the implanted dose. When using Phosphorus as dopant, Carbon ability to reduce its diffusion may be exploited to **control the diffusion direction**. Another idea is to do **two implantations**: a deeper and more tilted one for doping deeper under the SSTI (around 0.3 μm in fig. 2.5b) and a shallower more straight

one like in fig. 2.5a.



(b) Horizontal Phosphorus profile right under the SSTI.

Figure 2.5: Result of a full-P implantation around the SSTI and whole process flow thermal budget.

2.3 Choices

So far, the ion implantation techniques shown in chapter 3, along with the considerations on thermal budget, induce to consider **more suitable the processes 3 and 4**. Whether process 1 cannot present any advantage in any case, process 2 would become interesting if a doping with extremely reduced diffusion and low defectivity could be produced.

Process 3 requires further investigations in order to establish if the oxygen penetration and the low final dose in Silicon degrades too much the performance.

Process 4 eliminates the incertitude about the interactions between SSTI High Aspect Ratio Process (HARP) oxide but does not solve optimally the problem of sufficient doping and adds mask-related issues. Multiple implants

could allow deeper trenches and adequate doping.

The **combination of processes 3 and 4** (fig. 2.6), under the condition of clarifying the aforementioned issues, **implies an optimal doping** of the implanted collector: "through SSTI" implants allow to place the doping peak right under the trench oxide, while doping around the trenches is intended to increase the dose and to exploit Phosphorus diffusion. The co-implantation of Carbon and Phosphorus is meant to be used for controlling diffusion in the zone under the emitter window, since penetration of undesired dopants into the epitaxial part would degrade the delicate junction properties; high-dose P implantation are therefore limited to the Sinker zone. Particularly for this case, **an optimum has to be found on the SSTI depth**.

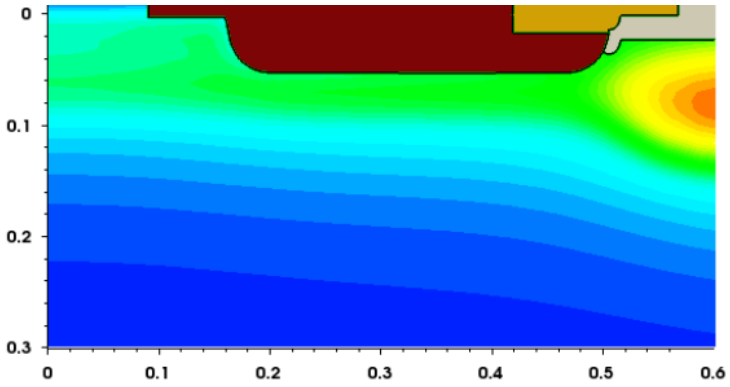


Figure 2.6: Simulated final structure for the SSTI integration in the B55X process flow.

After the doping of the whole transistor window by the implantation Carbon and Phosphorus, an additional doping of about three times its dose is done in the sinkers area with Phosphorus only. The first one is meant to dope in the most critical areas, namely under the SSTI and directly under the emitter window, while the sinker one means to reduce the sheet resistance in non-critical zones. Particularly for the central collector, it is important that the dopants cannot diffuse in high quantity toward the delicate base-collector junction: this explains why the higher-dose doping of the sinker is avoided here.

Because of the limited energy for carbon implantation (see chapter 3) it is not possible to achieve great depths for a C+P doping. This results in a

SSTI of only 50 nm, which can ensure that the most of the atoms can reach the Silicon. If deeper profiles could be reached, it is estimated that 100 nm SSTI would offer the best performances.

The maximum dose available on the machines shows simulated transition frequencies f_T of over 700 GHz but would pose problems on the reliability of the device. Anyway, the use of a smaller dose still gives encouraging results: peak f_T/f_{MAX} values of 550 GHz/350 GHz are reported (fig. 2.7). The simulations on the original deck showing f_T/f_{MAX} of about 535 GHz/180 GHz at the same polarization, the estimated improvement adds up to 94 % for f_{MAX}.

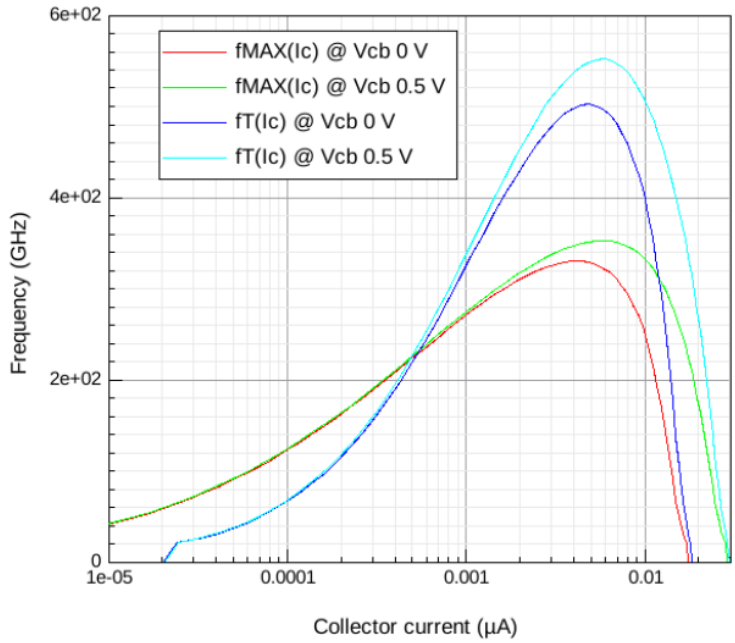


Figure 2.7: Simulated f_T/f_{MAX} of the final device at different V_{cb} polarizations

Chapter 3

Ion implantation process

Studies on doping by ion implantation used for the considerations of chapter 2, are here presented .

Ion implantation and the subsequent diffusion of the implanted species is a major concern in all microelectronics processes. Understanding this technique is an important prerequisite for mastering the collector architecture and achieve better performances. Considering the complex vertical structure, the **collector doping** is normally performed in the very beginning of the process flow, bringing to a relatively big thermal budget for its dopants to withstand. Along with the effort in reducing the high-temperature processes, particular attention is put in the choice of the implanted species.

Prior to the evaluation of what will be implanted, knowing the available tools ensures the possibility to realize the desired process. In particular, for these experiences, two equipments were available:

- **High-current implanter**: 0.2-60 keV, 8e12-3e16 cm^{-2}
- **Medium-current implanter**: 5-411 keV, 1e11-7e14 cm^{-2}

Notice that, depending on the implanted species, it is not always possible to use both the equipments, e.g. Carbon which was available only on high-current machines. The **implanted atoms** are, for the collector, **n-type dopants**, i.e. Arsenic and Phosphorus, while the **co-implanted impurities**, with attended supplementary effects, are Carbon and Fluorine.

Another parameter is the **implantation angle**: channeling effects along with shadowing problems are controlled by the tilt of the ion beam and eventually using wafer multi-rotation technique.

Lattice **amorphisation** is easily induced with the ion implantation process because of the high energies and doses used in the process. Lattice recrystallization during thermal treatments may have particular and interesting results such as the snowplow effect during the **Solid Phase Epitaxial Regrowth (SPER)**. This effect induces dopants redistribution because of their different solubility in amorphous (A) and crystalline (C) zones: while the A/C boundary moves, dopants are captured and spread in the reformed lattice depending on their concentration and eventual interaction with the defects. A **total amorphisation** is usually preferable since it allows a better healing of the substrate with respect to a partial lattice degradation, i.e. no defects are present after the process. If some residual defects are present, they may diffuse in the structure eventually leading to Oswald ripening and degrade the electrical performance or inactivate the dopants through clustering (see section 3.2).

3.1 Diffusion Mechanisms

A good comprehension of the diffusion phenomena is important for the design choices and the TCAD simulations setup.

For the doping species selected, two basic phenomena are taken into account:

- Fick's diffusion laws
- Transient Enhanced Diffusion (TED)

3.1.1 Fick's diffusion laws

Describing diffusion in a multitude of phenomena, Fick's diffusion laws (eq. (3.1)) can accurately describe dopant diffusion in a crystal lattice through analytic equations:

$$J = -D\frac{d\varphi}{dx} \tag{3.1a}$$

$$\frac{\partial\varphi}{\partial t} = D\,\frac{\partial^2\varphi}{\partial x^2} \tag{3.1b}$$

Where J is the diffusion flux, D is the diffusivity, φ is the concentration of dopants, x the position and t the time.

These equations are generally valid for **simple diffusion mechanisms** which involve the interstitial or vacancy diffusion without the inclusion of clustering mechanisms. Consider that the important parameter in these equations is **diffusivity** D, which relies on the Arrhenius law (eq. (3.2)):

$$D = D_0 \cdot \exp\left(-\frac{E_\mathrm{A}}{RT}\right) \tag{3.2}$$

Where D_0 is the maximum diffusivity, E_A is the diffusion coefficient, T is the temperature and R is the gas constant.

In fig. 3.1 is shown the **effect of temperature on diffusivity**. Notice how the exponential dependence may change diffusivity by several orders of magnitude, making clear the impact of thermal budget on the final result.

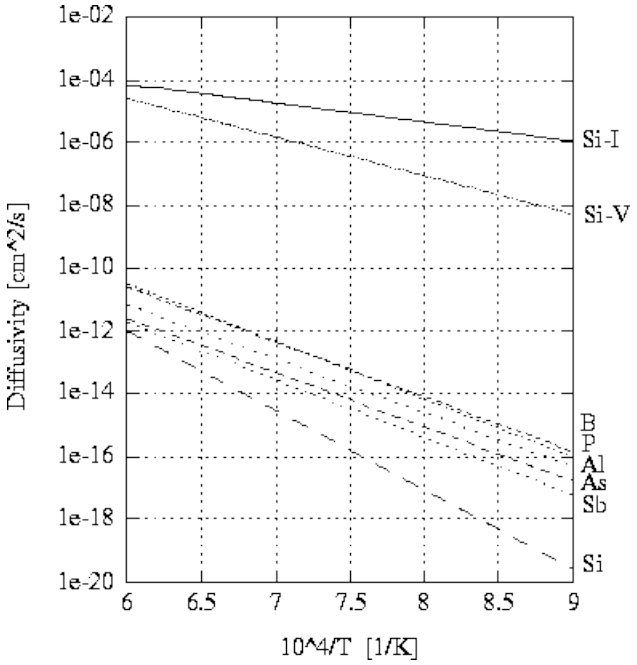


Figure 3.1: Diffusivity vs temperature of the principal diffusing species in Silicon. Picture from [15].

The time and temperature dependence of Fick's and Arrhenius' laws clarify the effort of the late years to migrate towards **low-thermal-budget processes** which could ensure the best control over diffusion ensuring a correct dopants activation.

3.1.2 Transient Enhanced Diffusion (TED)

The formation of various types of **clusters** may occur after the creation of point defects during ion implantation. These clusters, according to the nature of the defects, may originate anomalous diffusion phenomena not directly considered in Fick's diffusion laws: this is called **Transient Enhanced Diffusion (TED)**.

TED has been explained by Stolk et al. [18] as the result of the **clustering** between a **substitutional atom** A_s with a **Silicon self-interstitial** I (eq. (3.3a)). The chemistry of Phosphorus or Boron allows the formation of these complexes. The increased interstitial concentration [I] in the ion-implanted region will shift the local equilibrium between substitutional and mobile dopant atoms, thus the resulting **enhanced dopant diffusivity** D_A^{enh} is given by eq. (3.3b).

$$A_s + I \Leftrightarrow A_I \tag{3.3a}$$

$$D_A^{enh} = D_A^* \tag{3.3b}$$

Since in this way diffusivity grows, TED represents the **main limitation** when dealing with phosphorus implants, making extremely difficult to maintain them over a narrow profile in presence of even normal thermal budgets. In section 3.2 is explained how **carbon co-implantation** may overcome this difficulty.

3.2 n-type dopants - techniques

Historically, the most widely used n-type dopant is **arsenic**. When silicon is deposited (CVD, epitaxy), arsenic remains the preferred n-dopant because of its **very low diffusivity** and its atomic radius close to the silicon one, reducing the lattice stress in highly doped structures when it becomes a substitutional impurity. A not negligible problem, when it is **implanted**, is the onset of **defects**, which eventually cluster forming dislocation loops very harmful for dopants activation. If their number is reduced after the application of thermal budget, their size increases: the problem is not eliminated and presents important reliability problems. Because of the mass higher than the silicon one and the consequent high energies used for reaching useful depths, it easily induces crystal defects. In fig. 3.2 are shown some important defects that could arise from implantation and anneal of Arsenic

in a Silicon wafer through the phenomenon called **Ostwald ripening** [10], known to be harmful for the electric performance. It is possible to suggest that this phenomenon limits the performances of a collector implanted with this dopant, explaining why in [6] better parameters are found in devices differently doped. The **correlation** with performance is however **not proven**.

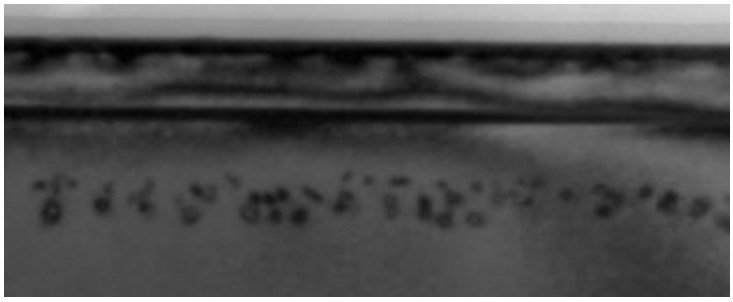


Figure 3.2: Dislocations in Arsenic-implanted Silicon.

Another quite common dopant is **phosphorus**. With its lower mass and atom dimensions, it requires less energy to reach a certain depth (~ 1 nm/keV) and creates almost the same defects as Arsenic. It is subject to **TED**, which makes it undesirable when high control on the doping profile is needed, particularly in presence of important thermal budgets.

In order to mitigate phosphorus diffusion, it is known [11, 13, 16, 23] that **Carbon** may have very interesting effects. Substitutional Carbon atoms transform into interstitial by a reaction with the Si self-interstitials created by implantation or dissociates itself in an interstitial with subsequent formation of a vacancy (eq. (3.4)):

$$C_s + I \Leftrightarrow C_i \tag{3.4a}$$

$$C_s \Leftrightarrow C_i + V \tag{3.4b}$$

This results in **suppression of TED**-originating Si self-interstitials and creation of vacancies, with the result of stopping Phosphorus and increasing Arsenic diffusion.

Studies on the presence of defects have been done by Gauthier et al. [6], showing that implantations of Carbon and Phosphorus are able to **widely**

reduce the creation of defects thus decreasing TED (fig. 3.3). This is a major improvement for the DPSA-SEG with implanted collector, allowing to reach record performances. This type of doping is therefore the most suitable to be used in the collector implants for EXBIC structure presented in this work.

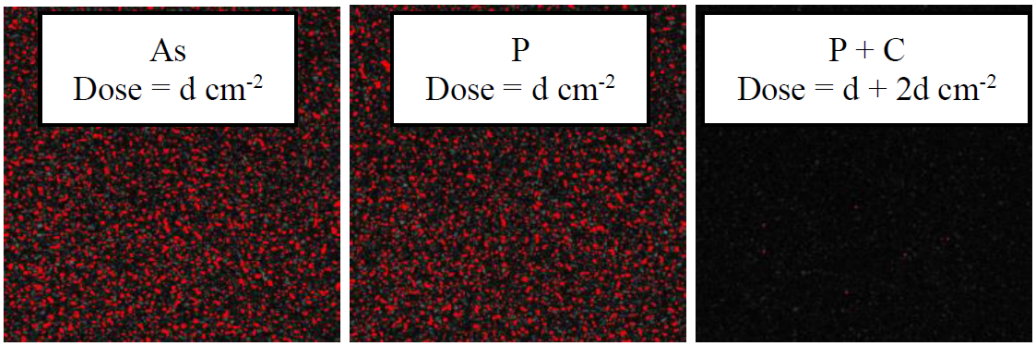


Figure 3.3: Photoluminescence Imaging (PLI) results showing defectivity after the implantation of different species. So-created Point defects generate dislocation loops through the application of thermal anneals, becoming radiative and detectable by this technique. Picture from [6].

3.3 TCAD simulation calibration for predictive analysis.

Considering the EXBIC collector structure, some implants are done in the beginning of flow, consequently diffusing because of the thermal budget. In order to achieve a good **calibration**, some parameters have been tuned using a Secondary Ion Mass Spectroscopy (SIMS) profile with a thermal treatment from the flow as reference.

Phosphorus calibration is here taken as an example to show how different may be the final result. The simulation/experiment conditions are an implant at 30 keV using a dose higher than 1e14 cm^{-2} and a thermal treatment slightly above 1000 °C for few seconds.

Knowing the **diffusion mechanisms** and what may be mostly impacting, the tuned parameters are:

- **Intersitial defects**: which are Si atoms positioned between the standard positions in the perfect crystal lattice. These defects are those

playing the essential role in P diffusion because of TED, as seen before. Modifying the number of created defects per implanted atom, it is possible to control diffusion. Here the number of defects created with the standard model is multiplied by a factor PhIf.

- **Vacancy defects**: which are the absence of a Si atom in the usual position of the crystal lattice. These defects have smaller impact on P diffusion. Modifying the number of created defects per implanted atom, it is possible to adjust diffusion. Here the number of defects created with the standard model is multiplied by a factor PhVf.

- **Amorphous threshold**: species diffusion is different between crystalline and amorphous silicon because of the multiple effects influencing diffusion. Over a certain density of defects, the material is considered amorph, i.e. without crystal structure. This is represented, in the simulation, by the saturation of the number of defects. This will affect the number of particles eligible to interact with the diffusing dopants, changing their redistribution. Changing the threshold, it is possible to impact on the overall process.

- **Recrystallization model**: standard simulations consider the recrystallization of the amorphized zone as an instantaneous process. Activating the **SPER** model, more adherence to the real process is ensured using in turn more calculation resources. SPER takes into account that the amorphous-crystalline interface will move during recrystallization tending to restore the order in the degraded lattice layer by layer, with particular effects in dopants distribution.

As a first trial, it is possible to observe the impact of these parameters in fig. 3.4. While the green curve is the SIMS, i.e. our target, the red curve represents what we obtain without any calibration. We clearly see that spanning the parameters PhIf and PhVf in a range of [1;15] the difference is dramatical, which explains the importance of a good refinement of the curves.

Narrowing the range of useful values, it is then possible to observe the impact of amorphisation threshold (fig. 3.5): considering that silicon has an atomic density of 5e22 cm^{-3} and that the standard value is 1.25e22 cm^{-3}, the explored values are on the same order of magnitude. The curves displayed represent the combination of extreme values of PhIf and PhVf for values of Ath spanning from 1e22 to 4e22 cm^{-3} Defining at which point silicon loses its

crystallinity, we set the number of defects that are eligible to interact in the dopants diffusion and we may also change the depth where the amorphous-crystalline boundary is found. This parameter, added to the previous two, should ensure enough control over the curve shape.

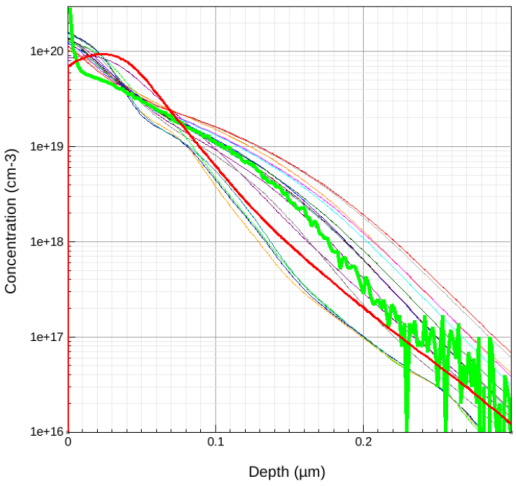


Figure 3.4: Effects of parametric multiplication of interstitial (PhIf) and vacancy (PhVf) defects, 1.25e22 amorphization threshold. Green = SIMS, Red = uncalibrated.

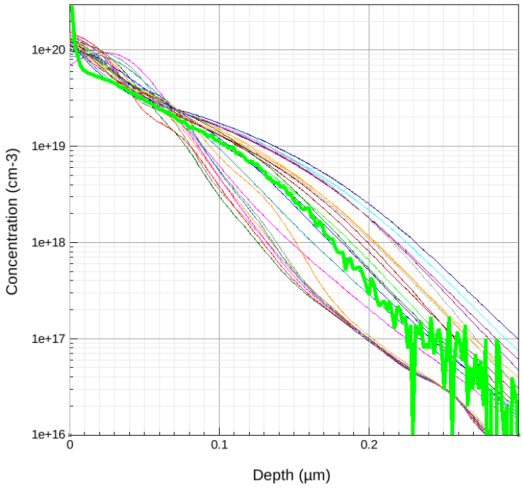


Figure 3.5: Effects of parametric multiplication of interstitial (PhIf) and vacancy (PhVf) defects, amorphization threshold variation (Ath). Green = SIMS.

While the implantation profiles are the same between SIMS and simulation, the diffused profiles show, apart from the defects difference, also a dose anomaly. Integrating the curves, we see a dose loss between as-implanted and diffused profiles that is not the same (fig. 3.6). Since this difference appears to arise from the first nanometers, it may explain the bulk in the simulated curves. This may be due to dopants out-gasing during the anneals, originating a flux that in the end influences the surface Phosphorus distribution. Two strategies have been adopted: calibrate the curves not considering the first nanometers (fig. 3.7) or adapt the implanted dose achieving the same final value between SIMS and simulation (fig. 3.8). A proper calibration on surface diffusion should be done, paying particularly attention on the interface phenomena. However, if the solutions could give acceptable results, this calibration would be useful as first approximation.

Operating a refinement in the values, it is finally possible to achieve a

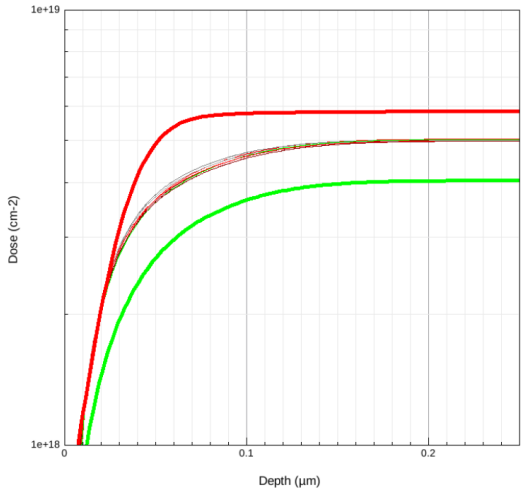


Figure 3.6: SIMS vs calibration curves integrals - Red = as-implanted, Green = SIMS diffusion, others = simulated diffusion.

very good adherence to the experimental data. If the tolerance in the SIMS measure is also taken into account (10%), the calibration process is done.

In fig. 3.8 are the final results for the calibration with the original dose, where displayed curves have an amorphization threshold value of 2e22 cm^{-3} and interstitials and vacancies are multiplied by values in the range [3;4].

In fig. 3.8 are the final results for the modified-dose calibration, where displayed curves have an amorphization threshold value of 3e22 cm^{-3} and interstitials and vacancies are multiplied by values in the range [4;5]. The dose has been reduced by almost 20%.

Efficacity of the SPER model is studied to evaluate its impact on the simulated parameters. Using SPER model (fig. 3.10), more adherent curves are found with a higher defects multiplication factor, in the range of [6;7]. This model will be used when a strictly more precise curve is needed; notice that, specially for the curve with unmodified dose, the amelioration obtained by the activation of this model is negligible. In the other cases, the precision of the normal model is considered sufficient.

A final remark on the SIMS curves has to be done. Because of the analysis technique used, the first nanometers are usually not well measured and it is difficult to clearly observe surface effects. In particular, since prior to this measure there was a thin layer of oxyde on the surface which has been stripped, segregation may be present but hardly evaluated in our calibration.

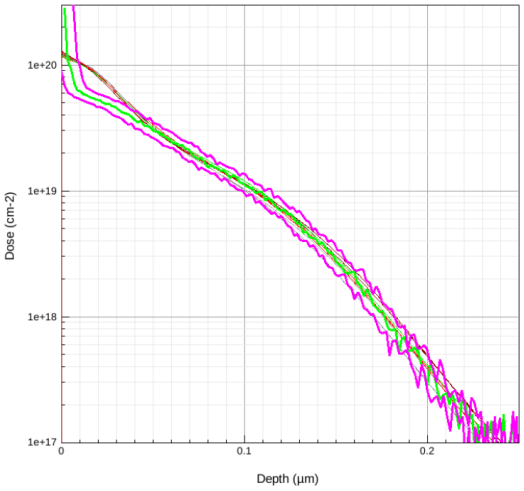


Figure 3.7: Final curves after calibration without dose refinement- Green = SIMS, Pink = SIMS tolerance limits

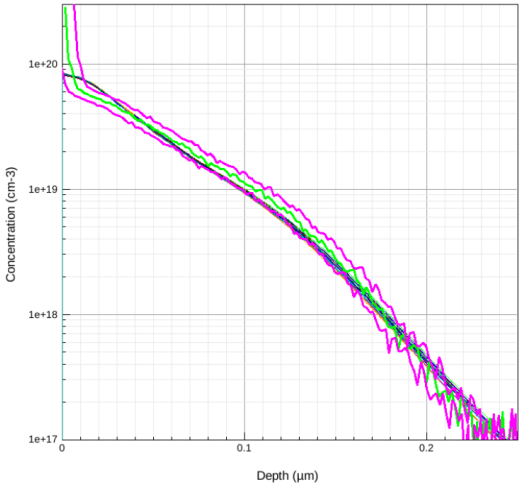


Figure 3.8: Final curves after calibration with dose refinement - Green = SIMS, Pink = SIMS tolerance limits

Also degasing of dopants is though to fake the simulation results, which may treat this phenomenon with uncalibrated parameters that have not been tuned in the presented process; further investigation is needed.

As a final consideration for the current calibration process, a calibrated curve has been obtained with predictive abilities on the qualitative result of diffusion. The successive step is to verify the results with other experiments and to refine the calibration.

3.4 Fluorine and Arsenic implantation

Searching for some kind of co-implantation that could improve Arsenic properties, an improvement in the implantation results has been found in literature[9], consisting in a co-implantation of **arsenic** and **fluorine**. Even if in conditions not much close to ours, this process seems **interesting for our purposes**.

Another paper [14] shows that **Fluorine** may have profound **different interactions with the defects** created during implantation, leading to clustering effects that can impact on diffusion. Referring to Arsenic co-implantation, this may result as defect suppression or diffusion modification.

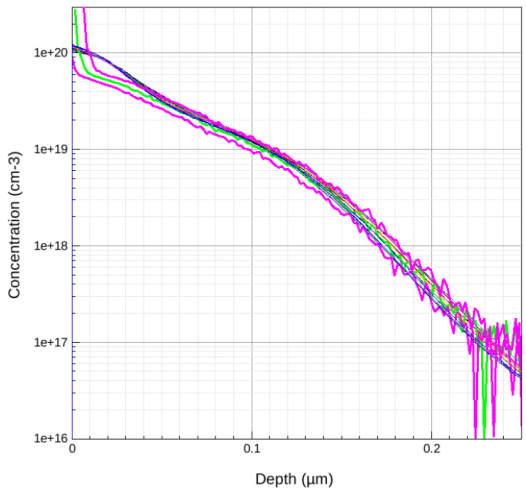


Figure 3.9: Final curves after calibration without dose refinement but with SPER model active- Green = SIMS, Pink = SIMS tolerance limits

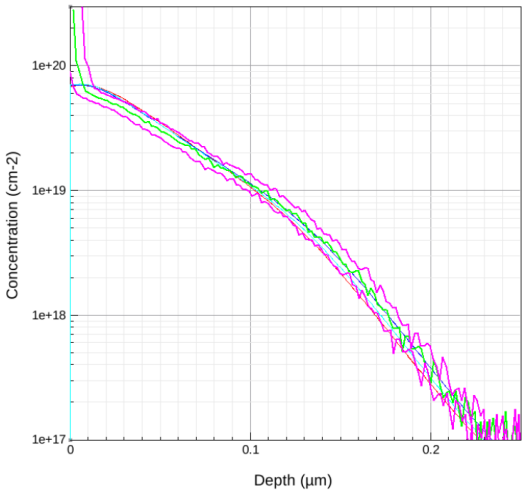


Figure 3.10: Final curves after calibration with dose refinement and SPER model active - Green = SIMS, Pink = SIMS tolerance limits

The tests will be repeated in process conditions compatible with our technology, i.e. implantation energy/dose adherent to the needs and thermal treatment at similar temperatures. This will show us if this process may be helpful for our needs. It is important to notice that in the cited paper [13] there is no evidence on the Fluorine behaviour or Arsenic interaction and its redistribution is not shown. Moreover, different annealing temperatures show different redistribution of Arsenic, without a precise explanation on the diffusion mechanism. One evidenced effect is the reduction of the created defects after annealing in presence of fluorine, possibly due to a so-far **unexplained mechanism**.

3.5 Silicon results

The **test conditions** are:

- Two-steps As implant with energies in the range 100-200 keV, doses in the range 5e13-5e14 cm^{-2}.
- Fluorine implant with energies in the range 30-100 keV, doses in the range 5e13-5e14 cm^{-2}.

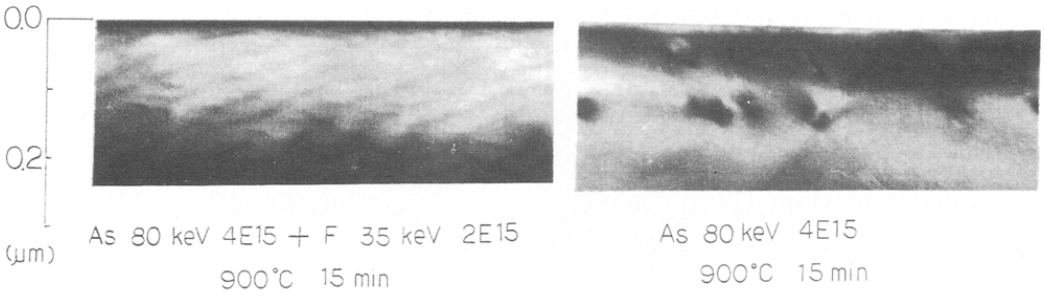


Figure 3.11: As+F implantation defects reduction by thermal anneal; Transmission Electron Microscopy (TEM) photo from [9]. Notice the thermal treatment different from the 1050 °C 5 s used here.

- Rapid Thermal Anneal (RTA) 750 °C 1 h.

A **POR** is done with no fluorine implanted.

Prior simulations have been done in order to place the fluorine implant peaks at the good position, i.e. in correspondence with the As peak and a bit further like it is done for C+P implantations. From the **as-implanted profiles** (fig. 3.12) it possible to confirm a good positioning.

After thermal treatment (fig. 3.13), the **Arsenic** profile shows **low diffusion** (10 nm shift for the $1e18cm^{-3}$ point) as usual but **Fluorine** highlights the occurrence of an opposite and **unclear phenomenon** with respect to diffusion: the curve shrinks and concentrates dopants almost in the same points with practically the same behaviour for every split. This tendency is also confirmed by the slight bending of the Arsenic profile in correspondence of the Fluorine maximum. A first idea is to attribute this result to the Fluorine segregation in high-defectivity regions and to the snowplow effect during recrystallization. KMC simulations will eventually confirm this tendency. Moreover, **up to 50 % of Fluorine disappears** after thermal anneal. Surface segregation and substrate diffusion are hypothesized, considering the broad as-implanted curves and a small layer of oxide (not shown in SIMS) present on the wafer. Concerning diffusion, there is also the possibility of Fluorine out-gasing from the substrate due to an enhanced solubility in the oven atmosphere. Another possibility is the formation of particular clusters not detected by the SIMS analysis because of their different mass.

Even if the bibliography related to this specific process is scarce, some studies have been done on the behaviour of Fluorine, corroborating some

hypotheses:

- Diebel et al. [5] demonstrated through *ab-initio* simulations the interaction between Fluorine and punctual defects.
- Jeng et al. [8] highlighted a consistent dose loss after thermal treatments, attributing this effect to volatile species originated from the combination of Fluorine with Silicon or Oxygen point defects found in the lattice.
- Both Tsai et al. [19] and Wilson [22] highlight interaction of Fluorine with defects and its distribution during recrystallization. It is however not clear the final impact on residual defects that may be harmful for the device.

Other analyses will be done in order to establish if this process is capable to offer Arsenic doping profiles with minimum defects as it is shown by Kato [9].

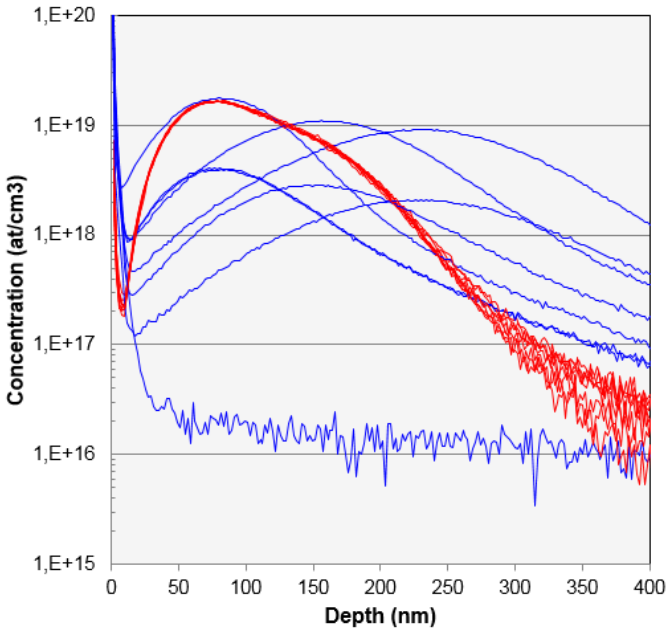


Figure 3.12: SIMS results of 7 different As+F implant splits, as-implanted profiles. RED = Arsenic, BLUE = Fluorine.

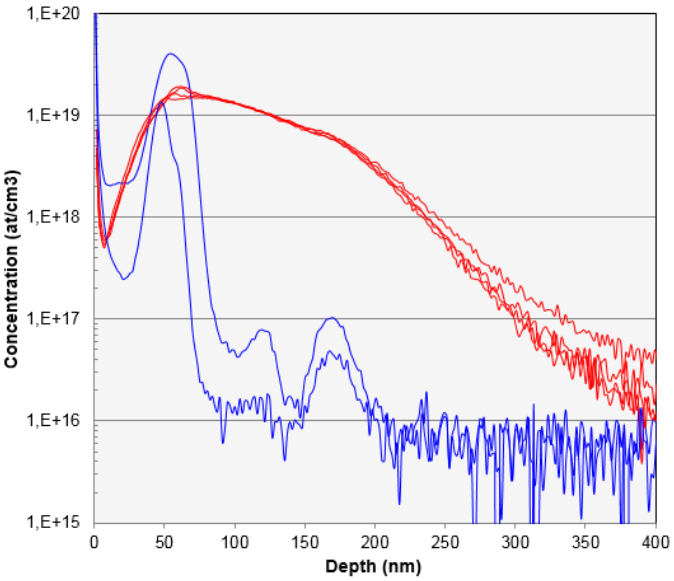


Figure 3.13: SIMS results of 2 different As+F implant splits, annealed profiles. RED = Arsenic, BLUE = Fluorine.

NOTICE: only two Fluorine curves are shown since all the others are practically superposed.

Chapter 4

SSTI process for a new collector architecture

Integration studies on Super Shallow Trench Isolation (SSTI), introduced in chapter 2, are here presented .

Integration process development aims to transfer what is working in theory to what is practically working, which results in having a real functioning device. This part of the engineering of the device is the one asking more effort, once the device physics are known, and consists in **assembling multiple processes** in order to create a **device with improved performances**. New production techniques allow engineers to create new shapes in the device, which in turn will allow to play with the device physics pushing further the performances. One clear example is represented by the old bipolar transistors: when only surface diffusion was available as doping technique and lithography could not approach nanometric dimensions, micrometric diffused transistors were considered cutting-edge technology; once ion implantation was mastered and photolithography improved, the recent devices were created making the diffused ones obsolete.

This is a critical point in the device development, since even the best transistor needs to be put on silicon and it is not always possible to transfer it exactly as it has been designed. Moreover, even if simulations reproduce quite accurately the **process flow**, they do can not consider all the variations and details that may influence the actual production, e.g. instruments calibration, impurities or defects in the recipe. It happens sometimes that what is a promising device in theory has to be abandoned because it is too complicated, expensive or simply the available process cannot ensure its re-

liability. Sometimes, on the other hand, what presents small problems in the final production line may be refined in order to ensure performances and reliability to the client. This is called **industrialization process**.

4.1 Process constraints and solutions

SSTI structure will require a **different process** from the STI one (etch, mask, etc.) but the twos still have to be present in the flow: whilst SSTI is used for bipolar transistors, STI is needed for inter-device isolation. Their coexistence means that the etch-related processes will be different but the fill, planarization and bake will be the same.

Indeed, a co-integration consists in different steps:

1. **Mask deposition and patterning**: depending on the trench width a different photolithographic process may be needed, whilst the trench depth influences the type of mask. Materials used for the mask take into account optical effects (anti-reflection, etc.) and the etching recipe used. In general, a hard mask is needed in order to avoid the elimination of the resin mask during the etch process: the polymer alone could be insufficient.

2. **Trench etching**: different depths require different etch recipes (etching species, etching time, etc.). The properties of the etch process influence the degree of anisotropy and the resulting shape; in our case an anisotropic etch with a trapezoidal profile is needed to ensure a correct fill.

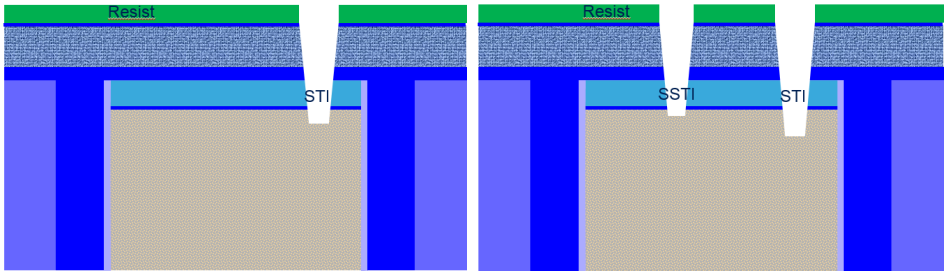
3. **Mask strip**: cleans the surface from mask residuals.

4. **Trench filling**: a dielectric (usually HARP oxide) is deposited on the wafer surface. It is important to completely fill the trenches in order to ensure uniform performance; this depends on the trench width and on the angle of the side walls.

5. **Thermal treatment**: is used to stabilize the oxide and make it resistant to the etches used later in the flow.

6. **Planarization**: eliminates the dielectric in excess, giving a flat base for successive processes. The usual process for this step is CMP, where a material different from silicon is used as stop layer.

A **first idea** was to use only one hard mask stack for both STI and SSTI (section 4.1): after etching the STI, a second exposition on the same mask would pattern the SSTI and allow the second etch. This solution was intended to be the simplest possible, reducing the need for different and complex masks a keeping the number of steps low. Since the etch recipe would degrade the hard mask, this solution could not ensure good control over the process needing some rework steps, thus eliminating the advantage of a single mask. It therefore **abandoned**.



(a) STI mask stack (b) STI patterning + etch

Figure 4.1: Single-hardmask process for SSTI. Discarded.

The **final process flow** chosen for integrating STI and SSTI on the same wafer consists in the realization of **two different hard masks**. In order to minimize the total steps, the process is in common for the two structures beginning from the gap fill step whilst the photolithography and etch part are done specifically for each one. This means doing steps 1 to 3 for STI, repeating them for SSTI and continuing with 4 to 6. It is schematically represented in figure 4.2 without any topological adherence to the final device. The DTI , filled with different dielectrics, is present on the sides, giving an idea on the proportions between the trench types.

The beginning silicon structure for this schematic process follows: the silicon part is covered with a thin oxide layer and a thicker nitride layer used as stop-layer for different CMP processes. The DTI is displayed on the sides as reference.

The **first hard mask** stack is **deposited**; multiple layers are needed each one with different functions ranging from anti-reflection layer to base for eventual reworks during the process. The photolithographic exposition allows to transfer the mask pattern to the surface resin. Figure 4.2a.

STI etching is performed through the multiple mask layers and realizing

the desired pattern. Beginning from the resin, each time a new layer is reached the etching gas is changed according to the material. The presence of multiple layers combines the possibility of reworks with the fact that during the different etch steps some layers are totally etched thus changing the surface exposed to the gas. Figure 4.2b.

The **mask is stripped**, leaving the nitride layer exposed along with the formed trench. Figure 4.2c.

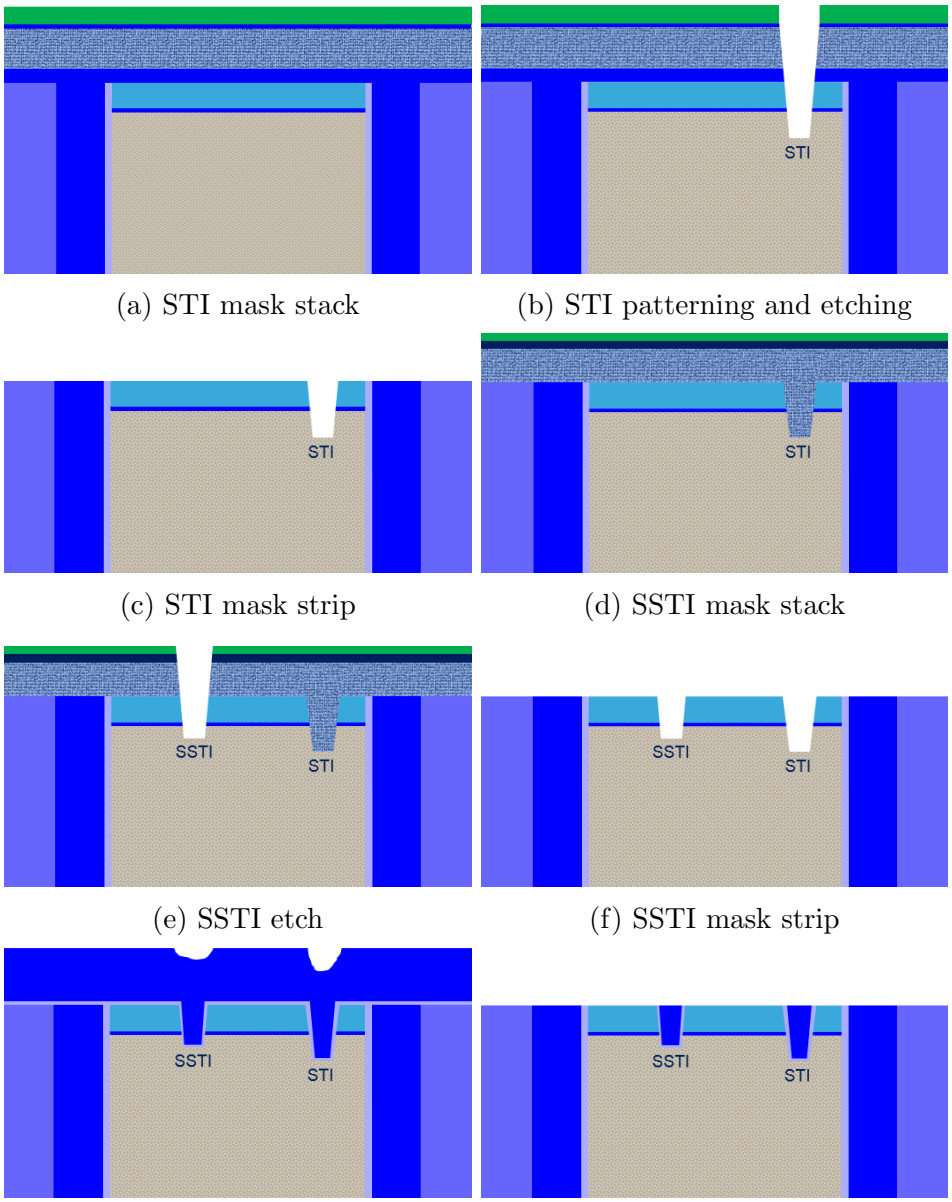
A **second hard mask** is **deposited**, covering the wafer and filling the STI. This mask is a tri-layer mask therefore simpler than the previous one thanks to the reduced depth of the trench: degradation of the layers will be lower because of the reduced etch time, not requiring higher complexity. Light exposition transfers the mask pattern to the resin. Figure 4.2d.

SSTI etching is performed. Figure 4.2e.

The second **mask** is **stripped**. Figure 4.2f.

The **gapfill dielectric** is **deposited**. The dielectric is carefully chosen because it is important to ensure the absence of voids in the trenches. Shallow structures have normally quasi-vertical walls, whilst deeper ones tend to increase their angle becoming trapezoidal; this has an impact on the capability to correctly fill the empty spaces. The bake finally ensures the dielectric to chemically stabilize and become ready for the following processes. Figure 4.2g.

CMP planarizes the structure to the nitride level which is used as a stop layer. The fact that SSTIs are a small structure only present in bipolar transistors, means it may be difficult to correctly planarize them: an appropriate polishing process is chosen for this reason. Figure 4.2h.



(a) STI mask stack

(b) STI patterning and etching

(c) STI mask strip

(d) SSTI mask stack

(e) SSTI etch

(f) SSTI mask strip

(g) Gap fill + thermal treatment

(h) CMP

Figure 4.2: Full STI+SSTI brick

4.2 Silicon results

To develop specific bricks of the process flow, a **short loop** is normally used in order to avoid the complete device process, allowing to spare time and money and to allow an easy analysis.

The STI process being well know, does not require particular attention and will be considered only in a final moment to ensure perfect process compatibility.

The creation of a new process for a specific product requires some **trials on the recipes** even if the used techniques are well known. This involves some experiments with the instruments in the conditions imagined in the production line.

A **full sheet deposition** of the **tri-layer mask** is done and a **full sheet etching** is conducted for the **End Point Detection (EPD)**. Since SSTI shapes are not wide and are not densely present on the wafer (few percent points in the mask transmission rate), it is difficult to detect the end point during the actual process. By using a full wafer, it is possible to do the EPD and, measuring the correct etching times, have a quantity easily measurable in full flow production. Whilst the etching time of the mask will be fixed by the EPD, the trench etching time is firstly determined theoretically and then calibrated through experiments.

Needing a good pattern for the etch, a **Focus Exposure Matrix (FEM)** is used to get the best photolithography conditions. This requires another wafer with a full mask stack.

Once the photolithography conditions are determined and the end point of the mask is known, it is possible to proceed with the actual **SSTI etching**. The etching procedure of the SSTI for the silicon part is the same used for the STI but, as already mentioned, there are differences in terms of width and density which may impact on the effective etched depth. A test etch (fig. 4.3) is then done with the theoretical time needed for etching about 100 nm down. The etched depth in silicon is 155 nm (section 4.2): knowing this it is possible to **calibrate the process** for the next experiments. The top-view observation of the trench after etching (section 4.2) demonstrates a good photolithography shaping; Optical Proximity Correction (OPC) can be used to eliminate the corners rounding if needed.

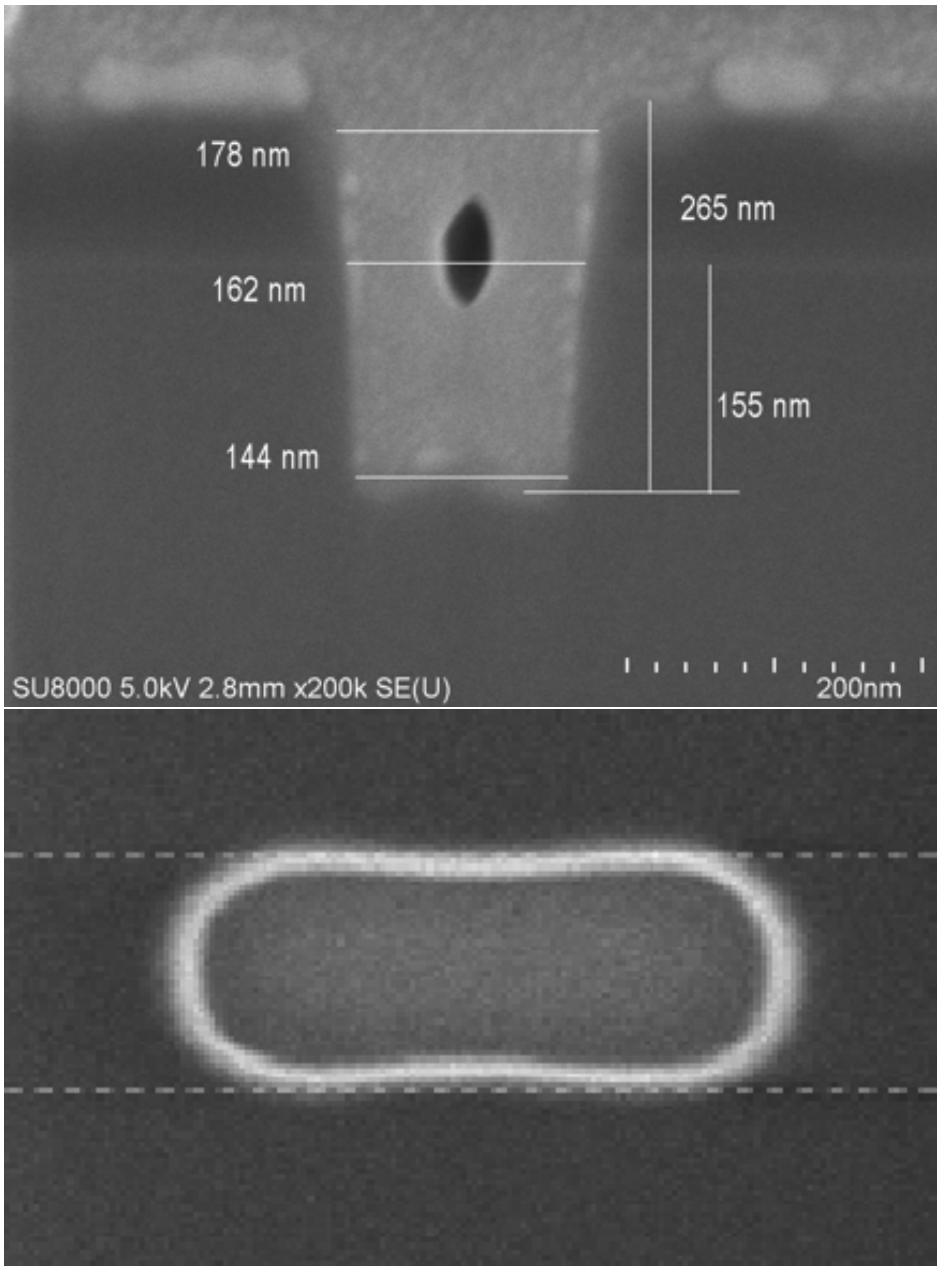


Figure 4.3: Scanning Electron Microscopy (SEM) pictures of the first SSTI experiment. Notice: the filling dielectric displayed is only used as contrast material to easily detect the structure borders and is not the final dielectric

A second experiment with a corrected etching time is meant to reach the target depth of 100 nm. The resulting trench proves that it is normally possible to produce such shallow trenches without difficulty. Moreover, since this experiment has been realized with the addition of the trench filler oxide (not present in the previous test), the compatibility with standard filling process is demonstrated. Notice however the small concavity on the bottom, probably related to the dry etching method. Anyway, this small defect is easily fixable and does not pose limits to the technique.

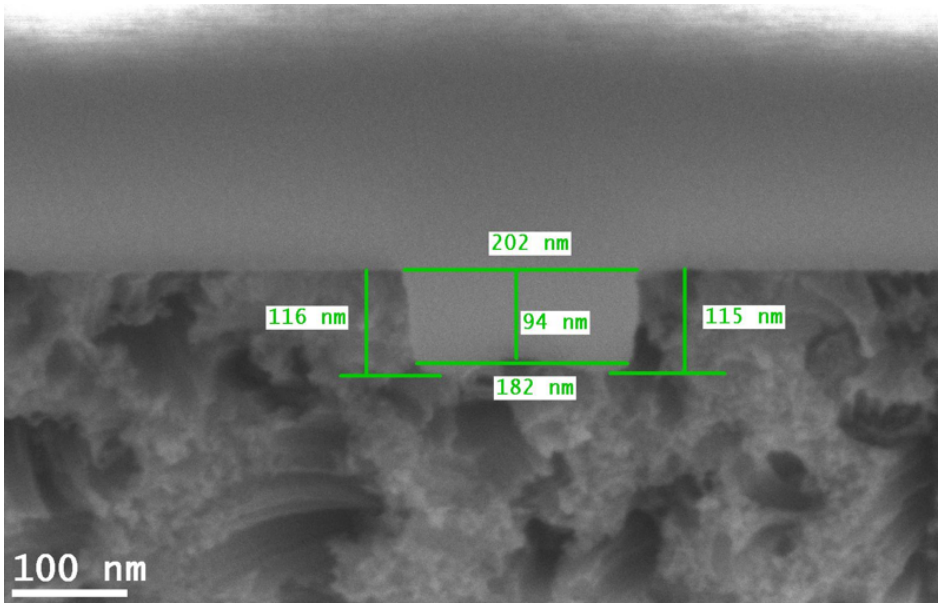


Figure 4.4: Scanning Electron Microscopy (SEM) pictures of the second SSTI experiment. The trench is filled with the final dielectric without voids.

With a good trench shape and the absence of critical problems, the structure is considered feasible in the imagined range of 50-100 nm. Process optimization will be studied to integrate it in a **full flow lot** for the reproduction of the final solutions found in chapter 2 and the electric performance evaluation.

Chapter 5

Conclusion

In the field of the next BiCMOS055X technology development in STMicroelectronics, the improvement of the collector part of the Heterojunction Bipolar transistor (HBT) devices with Epitaxial eXtrinsic Base isolated from the Collector (EXBIC) architecture is a matter of interest that could deeply impact on the performances.

Knowing the limits of the Double-Polysilicon Self-Aligned Selective Epitaxial Growth (DPSA-SEG) implanted collector structure showed by Gauthier et al. [6], the design of the new implanted collector for EXBIC transistors has two main targets: improve the overall transistor performance and offer a low-cost process. With these objectives, a new type of isolation trench called Super Shallow Trench Isolation (SSTI) has been developed and an adapt collector doping technique investigated.

The first TCAD simulations showing promising results, the criticality of the process has been demonstrated and research on different topics has been done:

- **Process flow organization**: the optimal sequence of steps to be done to realize the collector. A first proposal consists in the ion implantation done after the SSTI gapfill and only on the exposed-Silicon-zone; deeper implants go along with deeper trenches and lower capacitances. A second proposal is to implant through the whole bipolar active zone after the SSTI filling; a shallow trench means an easier trespassing of the filling oxide. Eventually, the combination of the two techniques seems to be the most promising solution, offering peak f_T/f_{MAX} values of 550 GHz/350 GHz with an estimated 94 % f_{MAX} improvement. Space is left for other solutions in case of future improvements. The

reproduction of the designed structure on Silicon will confirm the results.

- **SSTI process and structure engineering**: the study of the specific steps needed to realize this structure with an optimal depth. The actual optimum depends on the doping technique chosen, being anyway in the range 50 - 100 nm. Experiments for realizing a 100 nm structure have been done with no critical problems. A refinement in the recipe is needed and shallower structures will be investigated as well. Full compatibility with the other steps is ensured without critical modifications of the process flow.

- **Doping species**: the choice of the appropriate doping species is fundamental for a good performance. The chosen ions are Carbon and Phosphorus, offering a good balance between process control and defect creation. An additional technique consisting in Arsenic and Fluorine co-implantation has been investigated giving unclear results; a deeper understanding of the phenomenon may unveil useful characteristics for further improvements.

Appendix A

Gantt diagram

The Gantt diagram is intended to give an overview of how the time has been spent during the project.

Considering that this work has been conducted in a pure research and development approach, it was difficult to clearly define how much time would be spent on each subject and set deadlines. Instead of this, the focus has been put mostly on the desired results. The chart presented shows how the time has been employed. Each period comprehends the actual time spent for the production of the result, e.g. simulation coding, data analysis, and all the preparation work, e.g. bibliography, problem study.

Sometimes happened that encouraging results were found in spite of the initial estimates, thus requiring additional time for investigations.

Last of all, the time required for the full production of a lot and its analysis requires an amount of time that, added to the pauses needed for studying and discussing the problems, exceeds the total amount available for the development of this work. This means that part of the work will be continued out of the circle of the present research, in order to better understand some phenomena (chapter 3) or to practically reproduce and analyse the designed structures (chapter 2).

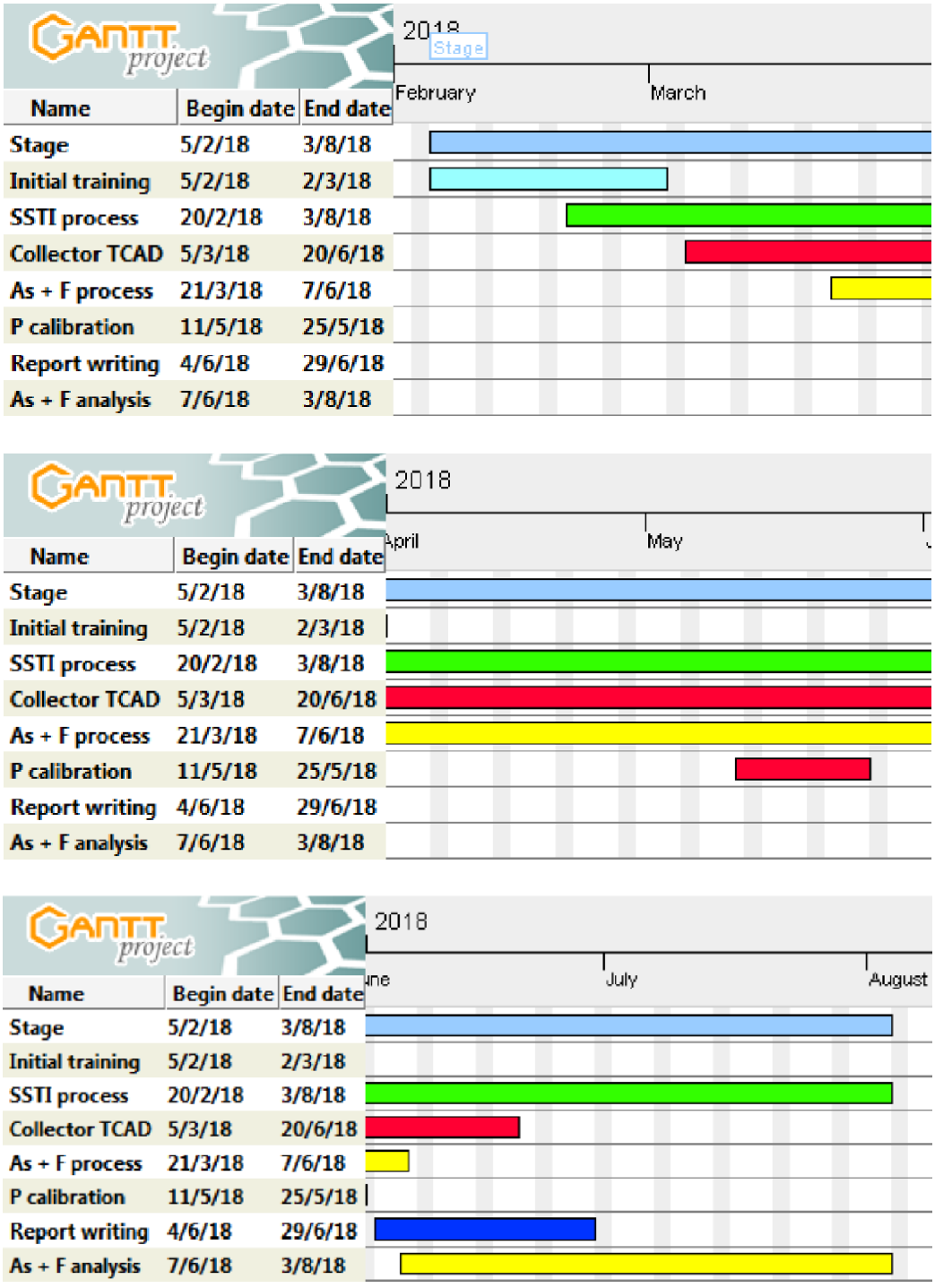


Figure A.1: Gantt diagram of the project.

Appendix B

Process flow, production lot and short loop

The process flow is the ensemble of operations done on the substrate in order to produce the final device.

All the products created in the ST Microelectronics' BiCMOS055 and BiCMOS055X technologies are fabricated in the 300 mm fab of Crolles, France on 300 mm Si wafers. Since this plant is completely robotic and intended for mass production, it is fundamental to define and code all the steps in a clear, reusable and complete way. The consequence is a schematic organization of the flow:

- **Brick**: is the main chapter of a process flow, generally corresponding of the realized part pf the structure, e.g. SSTI, collector epitaxy, intrinsic base epitaxy.
  - **Process Operation**: splits the brick in more specific modifications done on the wafer, e.g. mask deposition, photolithography, trench etch.
    - **Step**: corresponds to each instrument used for realizing the operation. Consider that for a single deposition, cleaning, measurements or rework steps may be necessary for ensuring a well done device.
      - **Recipe**: only one is chosen for each step. The recipe explains in detail everything that has to be done with the

single instrument. For an implantation it defines dopant, dose, energy, tilt, rotation angles.

A standard and unified system for the production management is important, particularly in a robotic automatic plant. **Production lots** are the main way of identifying a group of wafers and processing them: they are all from the same technology and mostly undergo the same processes. A lot is generally composed of 25 wafers and is stored in a **Front Opening Universal/Unified Pod (FOUP)** which ensure easiness of transportation and stable and safe environment. Consider that all the processes are done in cleanroom, i.e. rooms with a purified atmosphere, to exclude all the possible external contaminations. A numeric code corresponds to each lot and allows to easily refer to it especially in an IT system linked to the fab that is meant to control the instruments and to monitor the state of the production.

Especially when a particular experiment is needed, it may be necessary to modify the flow in a certain point, not requiring to produce the whole device. A clear example are the SSTI trials presented in this work. The modification of the process flow with the elimination of some unnecessary bricks, is called **short loop**.

The wafers in a lot do not forcedly undergo the same processes: a **split** may be done, meaning that from a certain point the wafers will see different steps; this is particularly useful when a process variation is studied. At this point, the lot is useful for relating a certain set of experiments to the same set of wafers.

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