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Tesi di Laurea

Investigation of a 3-Level DC/DC Converter as Buck Topology in the kW Range

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Abstract

The aim of this work is to investigate and realize a 3-Level Dual-Active Bridge. Starting from the theoretical investigation of the converter's working principle, this work later focused on the realization of its control, which modules the device thanks to a DSP-FPGA control board. Lastly, the hardware setup was built and tested, leading to results up to 2kV on the high voltage side, for a maximum power transfer of 13kW.

Contents

1 Introduction

The importance of renewable energies is increasing more and more by the years. In fact, the depletion of fossil energy resources and the already strong skepticism over nuclear impact on the enviroment, will cause a neat expansion of sustainable energy production. As renewable energies share increases, the size of the DC power grid can be enlargened, offering to the overall system a much higher transmission capability and an higher efficiency. [3] [16]

Thanks to DC/DC converters, the interest in DC transmission has heightened due to their ability to actively regulate the power flow between two terminals at different voltage levels. The dual-active bridge converter, realized with two H-bridges and a transformer in its simplest, single-phase structure, rapresents one of the most propitious topologies, due to its high energy density, galvanic isolation and bi-directional power flow.[6][7]. The voltage drop over the stray inductance of the transformer, which determines the transferred power, can be regulated by phase-shifting primary and secondary voltage of the transformer. Different topologies can be overwieved in [18] and [1]

Realizations of small power rating DABs are common, while its design at increasing voltages becomes rare. [15].To overcome the blocking capability limitations offered by the classical DAB, multi level topologies can be developed for dual active bridge. By already using an NPC (neutral point clamped converter) [17] or an ANPC (active neutral point clamped) [2] , the DC-link voltage can be increased. The higher the number of voltage levels, the larger is the number of degrees of freedom that can be strategically used by the user to increase the converter's efficiency.

Reading through the vast literature for low voltage DABs, and a recently published analisys of a medium voltage multi-level DC/DC converter up to 100kW, the aim of this work is to design and build a three-to-two levels 40 kW DAB, able to transmit power from the rectified low-voltage grid to an high voltage dc-grid, connected to the NPC side of the converter, chosing a reliable control structure that has to be programmed on an FPGA-DSP control board, which sends the switching pulses to the IGBTs and shuts-down the converter under undesidered working circumstances.

Chapter 2 introduces the working principle of the NPC three-levels/two levels DAB converter; an analytical description of a switching sequence in steady state condition will be explained for different operating modes of the converter, leading to the formulas which describe the mean output current of the converter and the transmitted power over one switching period.

In chapter 3, basics of FPGA and FPGA programming are shown; the compiling and testing enviroment of a VHDL code is presented, which has been used to achieve the desidered functionality of the FPGA; its role in this application is the generation of IGBTs switching

pulses, the exchange of data with the DSP through SPI communication and, lastly, application of a dead-time to the switching pulses.

Chapter 4 describes the control structure adopted: initially, a voltage-current control was intended, since the converter will, in the future, be connected to a 7MW converter realized at RWTH PGS institute. Unsatisfactory results and the lack of accurate current measurement has lead to the realization of an only voltage control, which regulates the phase shift to control the NPC terminal voltage.

In Chapter 5, the author will explain the hardware setup that has been built and tested: a three-phase diode rectifier to obtain the low DC-link voltage, employing a pre-charging circuit to avoid inrush currents, the H-bridge, the transformer and the NPC, the load that has been used and the control board to execute the control strategy and the safety devices that have been tested during safety routines.

The final chapter brings the results obtained with the realized,partial, set-up, read in real-time through a Labview interface and later compared with simulations results.

2 Three-Level NPC/Two-Level Dual-Active Bridge

2.1 Introduction

The three-level NPC/two-level dual active bridge is realized with a Neutral Point Clamped module on the high-voltage side and an H-bridge converter at the low voltage side. A transformer guarantees galvanic isolation between its primary and secondary side. The topology is shown in Fig 2.1

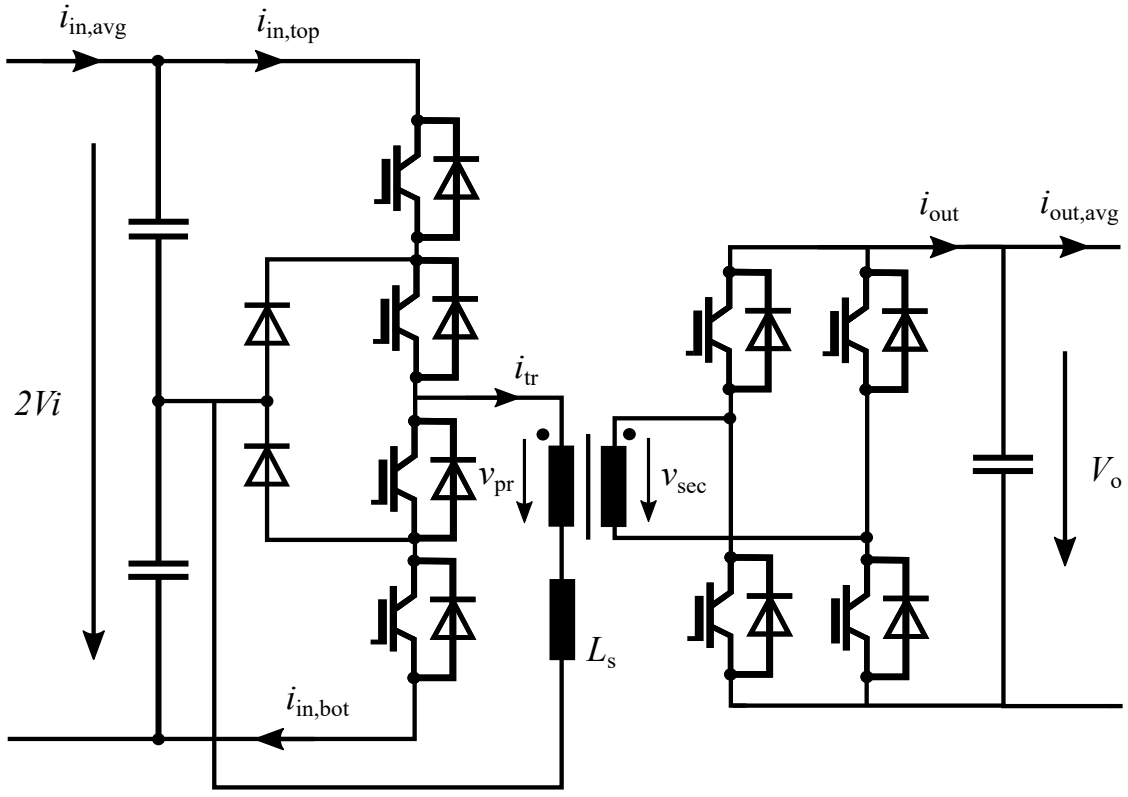

Figure 2.1: The three-level NPC/two-level dual active bridge; This topology offers galvanic isolation and an high energy density

A multi level converter topology, such as the NPC, ensures an increased voltage blocking capability on the high voltage side, since it is realized with a certain number of switches

connected in series. The converter realized, for example, is able to block twice the voltage rating of each IGBT, since during its operation, at most two switches conduct current, meanwhile the other two are in blocking mode and sustain the DC voltage. Also, with each level introduced, a new degree of freedom can be used to heighten the efficiency of the converter. This application features a transformer with high leakage inductance (design details can be found in [14][16]) :

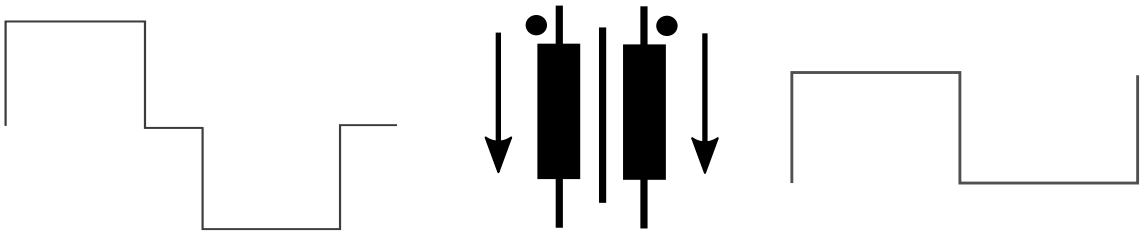

Figure 2.2: Primary and secondary voltage are not related to each other by a scale factor, such as the transforming ratio of the transformer. The difference in voltage is applied on the high inductance of the converter

It is obvious that the primary and secondary side of the transformer are not related to each other by means of the transformer's ratio. Fig 2.2. The difference in voltage is applied accross the leakage, thus causing the power flow. That's why, this inductance, which generally is designed in a transformer to be the smallest possible and assumed non-existing in ideal conditions, has to be chosen high in value according to this application.

2.2 Principle of Operation

In this section, an analytical description of the converter is shown. Simplifications take place as much as feasible to describe a system as close as possible to reality but introducing much simpler equations. The simplifications assumed are:

- Ohmic resistances are neglected,
- Switches are considered to be ideal; the switching is instanteneous and no voltage drops or on-resistances are accounted,
- No parasitic effects of stray inductances or capacitors are mentioned,
- Voltage sources are modeled as ideal
- The transformer is ideal, making exception for its leakage inductance; windings are ideally resistance-free and the magnetizing inductance is assumed to be infinite.

The NPC, mounted on the medium-voltage side, is able to feed to the transformer a positive, negative DC-link voltage or zero. Meanwhile, the H-bridge, at low-voltage side, applies a squarewave at the secondary side. By phase-shifting primary and secondary voltages, the

power flow between the two converter terminals can be controlled. The topology is realized to ensure bidirectionality of the power flow. To realize it, a negative power shift can be applied, leading to a negative power flow. As mentioned before, in a n-level converter, n-1 degree of freedom are introduced. in an NPC/two level DAB, the additional parameter with respect to a two level converter,is the duration of the zero-state, by moduling the width of β.

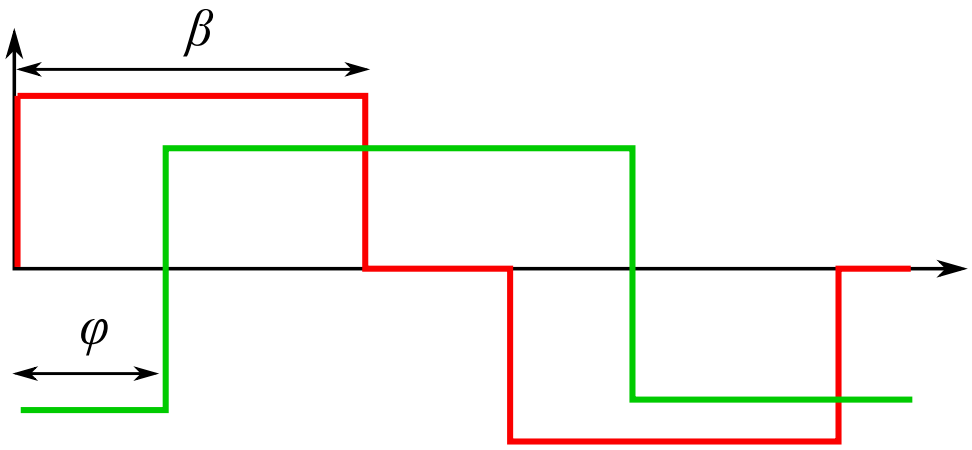

Figure 2.3: The two degrees of freedom of the topology are shown : ϕ is used to regulate the power flow, β to increase the converter efficiency.

Depending on the amplitude of ϕ and β, the converter can be operated in many operation modes. Nonetheless, since the interest is to transmit in every instant a non-positive power, the control always applies a negative phase-shift, causing the primary voltage to always lead the secondary one. The control, also, ensures a negative shifting between the voltages always lover than β-0.5, since the adoption of a greater value would still cause a positive transit of active power.

The desired working range is achieved between$-0.5 < x < \frac{\beta-0.5}{2}$, where is it possible to identify the two operation modes of the converter [19]:

- -OP2 for a lower power flow and low load condition.
- -OP1 when a deeper utilization of the converter is needed due to an higher load.

Working outside of this range would cause an undesidered positive power flow from the NPC to the H-bridge terminals. It is still possible to distinguish OP1 and OP2 for a positive power transfer; the analytical description of positive Operation Modes is identical to the negative ones, and can be obtained by simmetry.

2.2.1 Operation Mode 1

If $-0.5 < \phi < \beta - 0.5$, the converter works into negative OP1. This relationship between the two angles is always true in case a very high power is transmitted. Altough -OP1 is

symmetrical to OP1, meaning that the same power flow can be achieved in absolute value, -OP1 has a lower efficiency than its mirrored counterpart, since an higher phase-shift, and consequently an higher voltage drop, is applied on the inductor during each interval. Figures from 2.5 to 2.12 illustrate a switching sequence of the converter working in this operation mode, the red dotted line rapresent the path of the current while the arrow its direction. Fig 2.4, instead, shows current and waveforms during one switching cycle, assumed the converter is working in -OP1 steady state. V_i rapresents the NPC voltage,V'_o the H-bridge output refered to the primary side, i_tr the transformer current waveform, while the last,i_in shows the input current of the NPC. β has been choosen equal to 0.375, meanwhile $\phi = 50$ degrees approximatively.

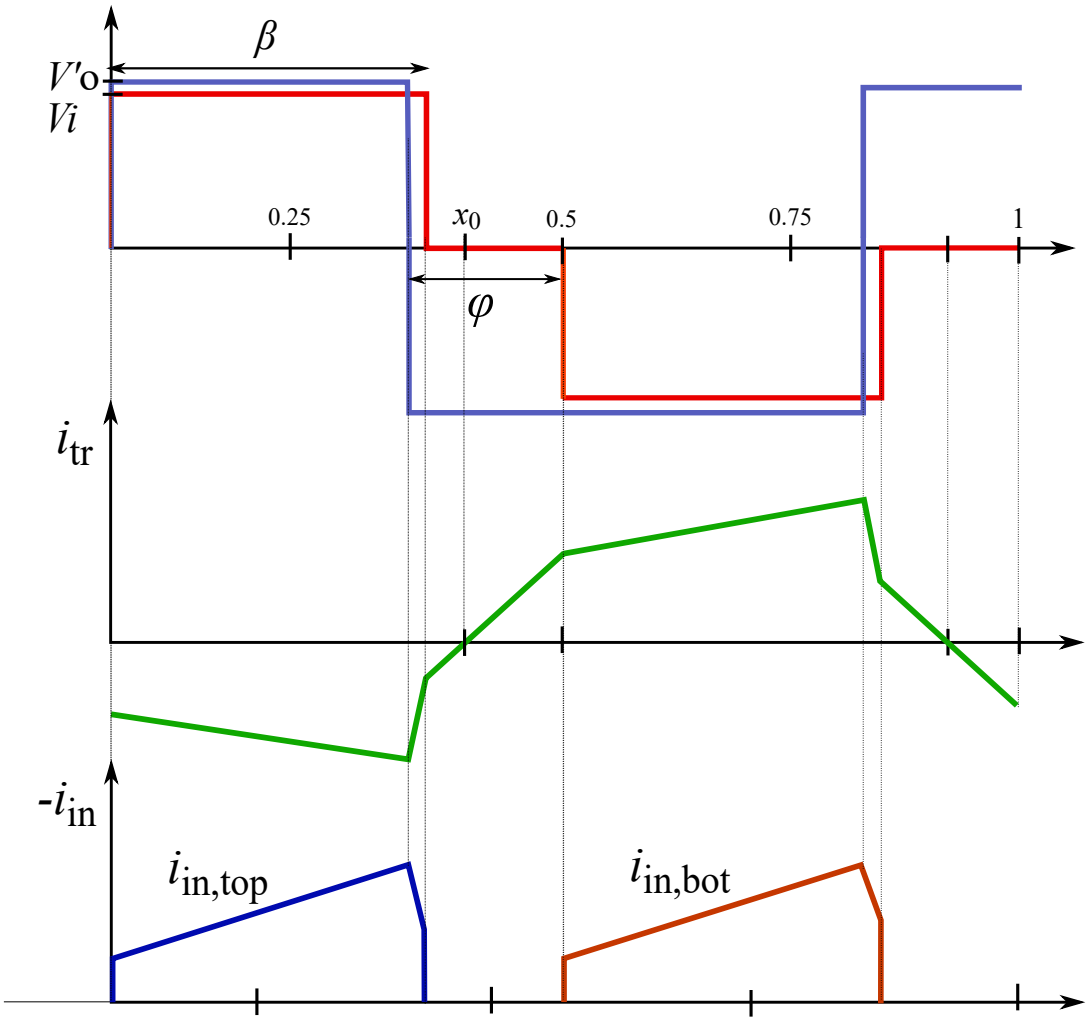

Figure 2.4: The waveform of one switching cycle are shown; a negative phase angle is applied, resulting in a negative high power transmitted in -OP1.$V_\mathrm{i} = 2500V$, $V_\mathrm{o} = 530V$, the transformer ratio is 5. Since V'_o> V_i, the converter works as a Buck converter.

$0 < x < 0.5 - \phi$: The NPC voltage is high, same as the H-bridge output, while the

current at the transformer is negative. This means that the current flows through the two upper anti-parallel diodes of the NPC, as show in Fig 2.5.

$0.5 - \phi < x < \beta$: During this interval, the inductor is demagnetized due to a positive voltage drop at its terminal: the current rises positively with a very high slope. Fig 2.6

$\beta < x < 0.5$: A reversal of the current can be observed. Initially, since the NPC output is zero, the negative current flows through the third switch and the clamping diode connected to ground. After the zero crossing, a positive current at the transformer flows through the second switch of the NPC, while in the H-bridge the current commutates in the first leg bottom and second leg top switches.

$0.5 < x < 1$: In steady state the average current through the inductor is zero; therefore the current during this interval is equal to the already observed one but mirrored with respect to the x-axis.

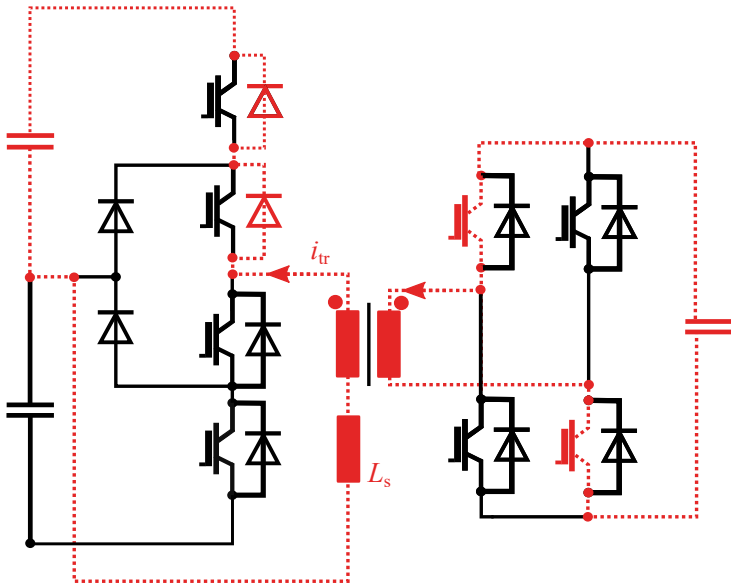

Figure 2.5: The red dotted line rapresents the current path: for $0 < x < 0.5 - \phi$ the current is negative and can only flow in the NPC anti-parallel diodes of IGBTs 1 and 2.

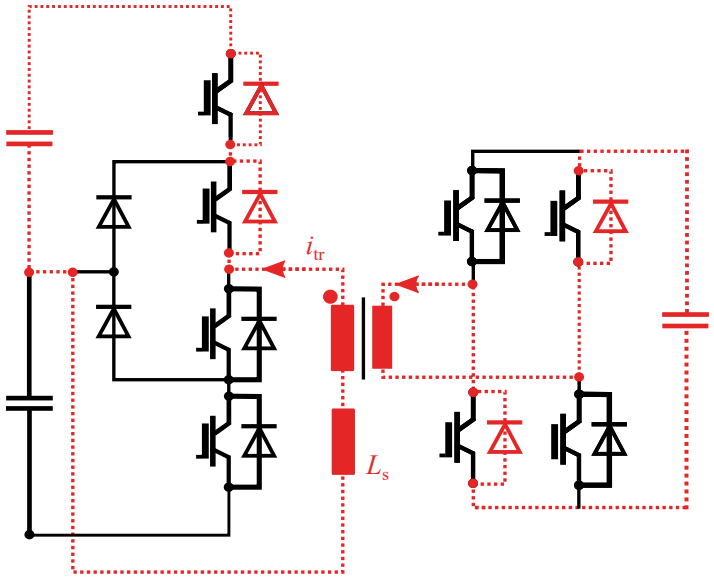

Figure 2.6: The picture depicts the current flow during the interval $0.5 - \phi < x < \beta$.The current is negative and still flows through the NPC antiparallel diodes, while in the H-bridge, whose output is negative, the current commutates in second top and first bottom antiparallel diodes.

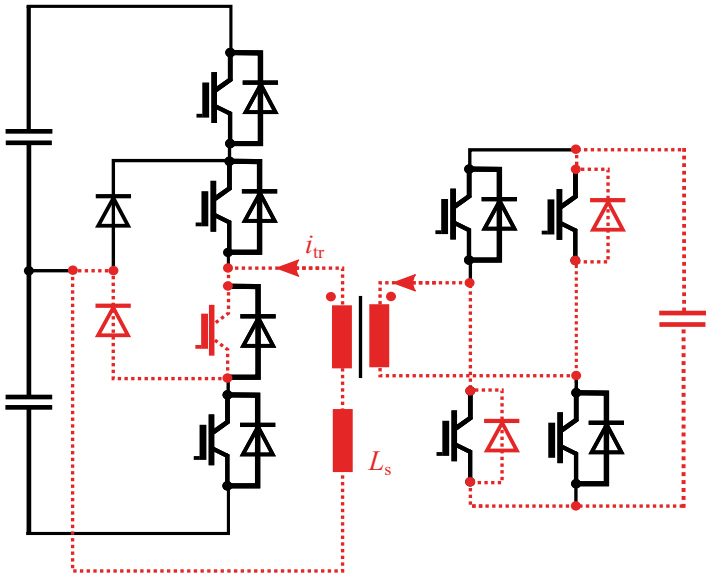

Figure 2.7: $\beta < x < x_0$: The NPC output is now zero, the negative current commutates from the two top switches of the NPC to the mid-point

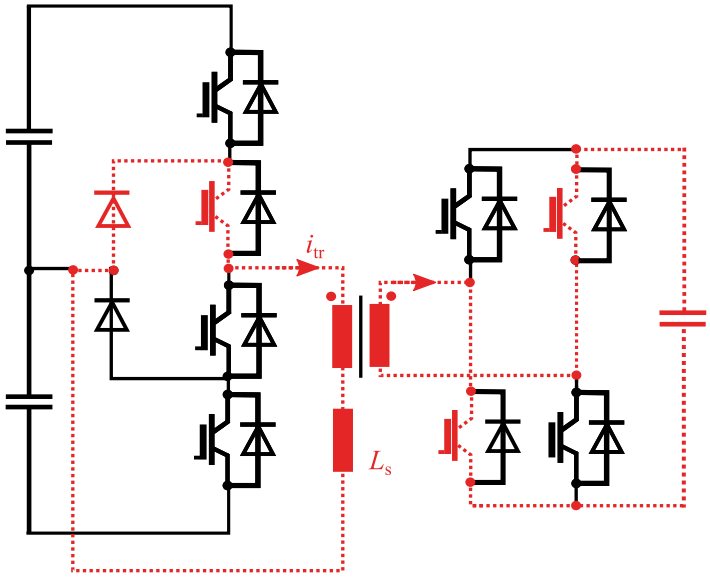

Figure 2.8: $x_0 < x < 0.5$: The voltage drop on the inductance is still positive: the current crosses zero and the inductor is positively magnetized. The current switches in the higher path of the NPC mid-point while it commutates through the switches in the H-bridge

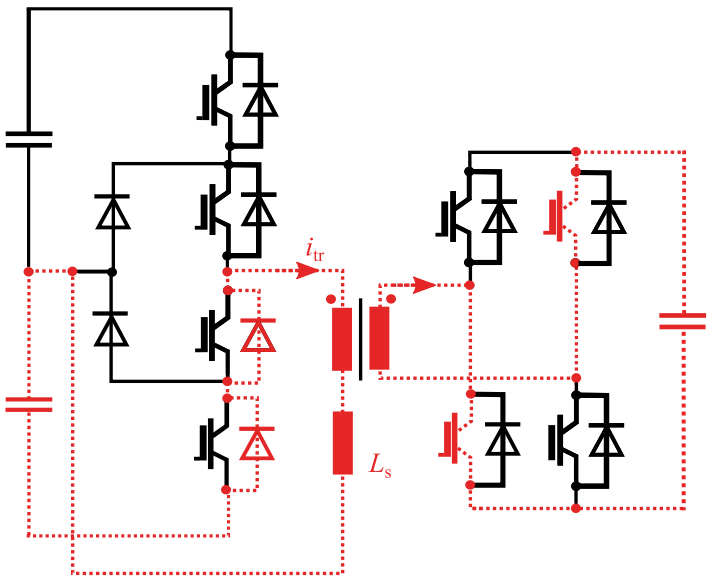

Figure 2.9: Current flow according to primary and secondary voltage during the interval $0.5 < x < 1 - \phi$; The NPC applies a negative voltage meanwhile the current is positive and can only flow in the antiparallel diodes of the ON IGBTs.

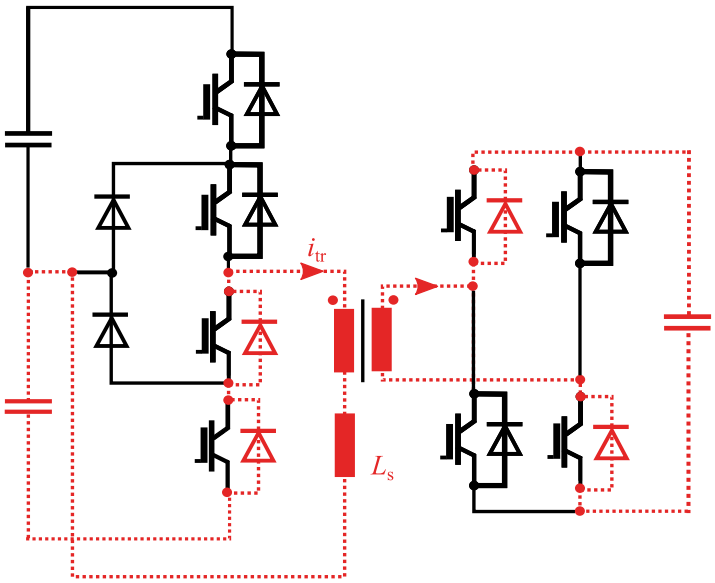

Figure 2.10: The H-bridge commutates applying a positive voltage; the inductor is demagnetized due to a negative voltage drop over its terminals.

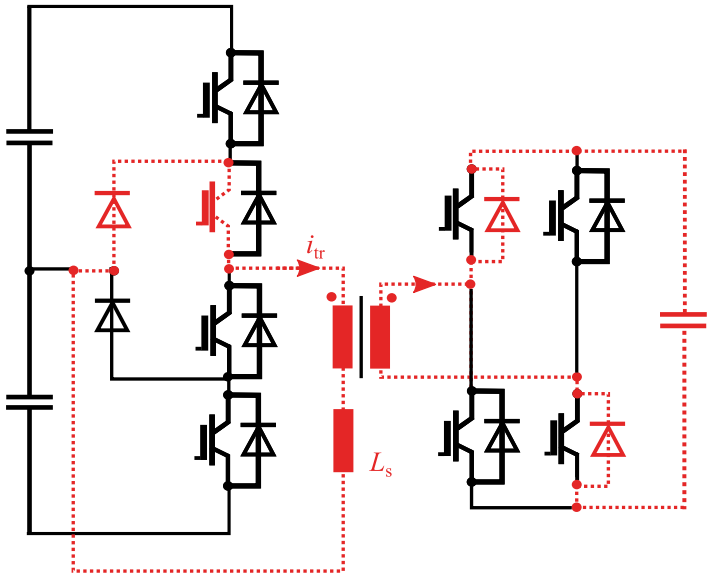

Figure 2.11: The NPC applies a zero output while the H-bridge a positive one, the current flows in the upper switch that connects the NPC midpoint.

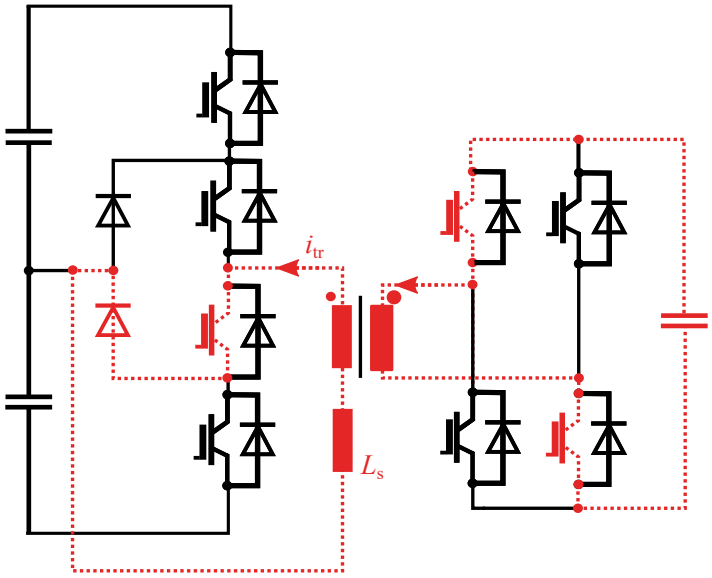

Figure 2.12: In this picture the last current commutation over one switching period is shown. The voltages at the transformer are equal to the previous cases, altough the current crosses zero and becomes negative, flowing through the bottom IGBT connected to the midpoint.

Now the analytical investigation of the working principle will follow. Thanks to the previous semplifications, the capacitors are ideal,no ESR and ESL are accounted, the transformer and inductor are resistance free and no stray inductances or capacitances are taken into consideration. In order to calculate the power transfer, the investigation of the current waveform needs to be performed, since it rapresents the only state variable of the model. Once known the transformer current waveform, it is fairly easy to draw the input or output current and to calculate its mean value over one switching period; this value will later lead to the power once it is multiplied by the DC-link voltage. The current through the inductor can be calculated during each time step by considering the voltage drop across its terminal and the initial current during the interval which is investigated :

$$0 < x < 0.5 - \phi : \qquad i_{\mathrm{tr}}(x) = \frac{V_{\mathrm{i}} - V'_{\mathrm{o}}}{fL_{\mathrm{s}}} \cdot x + i_{\mathrm{tr}}(0) \tag{2.1}$$

$$i_{\mathrm{tr}}(0) = \frac{-V_{\mathrm{i}} \cdot \frac{\beta}{2} + V'_{\mathrm{o}} \cdot (\frac{1}{4} - \phi)}{fL_{\mathrm{s}}} \tag{2.2}$$

$$0.5 - \phi < x < \beta : \qquad i_{\mathrm{tr}}(x) = \frac{V_{\mathrm{i}} + V'_{\mathrm{o}}}{fL_{\mathrm{s}}} \cdot x + i_{\mathrm{tr}}(0.5 - \phi) \tag{2.3}$$

$$i_{\mathrm{tr}}(0.5 - \phi) = \frac{V_{\mathrm{i}}(\frac{1}{2} - \frac{\beta}{2} - \phi) - V'_{\mathrm{o}} \cdot \frac{1}{4}}{fL_{\mathrm{s}}} \tag{2.4}$$

$$\beta < x < 0.5 : \qquad i_{\mathrm{tr}}(x) = \frac{V'_{\mathrm{o}}}{fL_{\mathrm{s}}} \cdot x + i_{\mathrm{tr}}(\beta) \tag{2.5}$$

$$i_{\mathrm{tr}}(\beta) = \frac{V'_{\mathrm{o}}(\beta + \phi - \frac{3}{4} + \phi) + V_{\mathrm{i}} \cdot \frac{\beta}{2}}{fL_{\mathrm{s}}} \tag{2.6}$$

Since the desidered mean average current through the inductor is zero, the voltage waveform during the second half of the switching period are symmetrical to the interval already investigated; solving the equations would therefore lead to equal solutions but with sign inverted. This condition can be synthetized as:

$$0.5 < x < 1 : \qquad i_{\mathrm{tr}}(x) = - i_{\mathrm{tr}}(x - 0.5) \tag{2.7}$$

Once drawn the current waveform, it is easy to obtain the output current of the NPC. During the first half cycle, in fact, the voltage fed to the primary side of the transformer is high for $0<x<\beta$, which means that the primary side of the transformer is at the same potential of the upper terminal of the NPC : a current is flowing, and this current is equal to i_{tr}. During the NPC 0 state, instead, the current ricirculates through the clamping diodes in the mid point and does not flow through the NPC terminals. During the second half-cycle, the same current flows through the lower terminal. This means that in order to calculate the mean output current, it is convenient computing this variable during only half switching period and then scaling up the result by a factor of two, as follows :

$$I_{\mathrm{av,p}} = \frac{1}{1}\int_0^1 i_{\mathrm{pr}}(x)\,\mathrm{d}x = \int_0^{0.5-\phi}\left[\frac{V_{\mathrm{i}} - V'_{\mathrm{o}}}{fL_{\mathrm{s}}}\cdot x + i_{\mathrm{tr}}(0)\right]\mathrm{d}x + \int_{0.5-\phi}^{\beta}\left[\frac{V_{\mathrm{i}} + V'_{\mathrm{o}}}{fL_{\mathrm{s}}}\cdot x + i_{\mathrm{tr}}(0.5-\phi)\right]\mathrm{d}x \tag{2.8}$$

Solving the integral leads to the following solution:

$$I_{\mathrm{av}} = 2I_{\mathrm{av,p}} = 2\cdot\frac{V'_{\mathrm{o}}}{fL_{\mathrm{s}}}\left[\beta\left(\frac{\beta}{2} - \frac{3}{4} + \phi\right) + \phi^2 - \phi + \frac{1}{4}\right] \tag{2.9}$$

The transferred active power is calculated by multiplying the obtained average current by the DC voltage, according to [10]. Thanks to the semplifications introduced, the voltages are constants and not state variables, which means that power and current are related to each other by a scale factor; to control the current or the power is the same operation in steady state.

$$P_{=} V_{\mathrm{i}} I_{\mathrm{avg}} = 2\frac{V_{\mathrm{i}}\cdot V'_{\mathrm{o}}}{fL_{\mathrm{s}}}\left[\beta\left(\frac{\beta}{2} - \frac{3}{4} + \phi\right) + \phi^2 - \phi + \frac{1}{4}\right] \tag{2.10}$$

The formula obtained is a function of two variables : ϕ and β. Both of them can be included in the control structure, altough generally is a simpler strategy (and more efficient) to module the power flow by modulating ϕ, while the second parameter can be changed (in a much more structured control) to achieve an higher efficiency. Deriving the computed formula with respect to angle ϕ, is it possible to obtain the phase-shift at which the transmitted power is maximum in negative value:

$$\frac{\mathrm{d}P}{\mathrm{d}\phi} = \frac{V'_{\mathrm{o}}}{fL_{\mathrm{s}}}[\beta + 2\phi - 1] \tag{2.11}$$

To meet a maximum the derivative must be set to zero. This condition is true for a phase shift :

$$\phi_{\mathrm{Pmax}} = \frac{1-\beta}{2} \tag{2.12}$$

Given the last result, it is easy to calculate the maximum negative power that the converter is able to transmit at given voltages.

$$P_{\mathrm{max}} = \frac{V_{\mathrm{i}}\cdot V'_{\mathrm{o}}\cdot\beta}{2fL_{\mathrm{s}}}(1-\beta) \tag{2.13}$$

The mimum power is transferred for an angle equal to :

$$\phi_{\mathrm{Pmin}} = \beta - 0.5 \tag{2.14}$$

And can be numerically calculated through this formula, obtained by substituting ϕ_{Pmin}.

$$P_{\min} = \frac{V_{\mathrm{i}} \cdot V'_{\mathrm{o}} \cdot \beta}{2 f L_{\mathrm{s}}}(1 - 2\beta) \tag{2.15}$$

Later on will be shown that the minimum power transmitted in OP1 equals the maximum transferred power in OP2. With the results obtained, it is easy to calculate the phase-shift that has to be applied in order to transmit a certain active power, assuming the converter in -OP1 :

$$\phi = \frac{1}{2} \cdot (-(\beta - 1) + \sqrt{\left(\frac{P}{f L_{\mathrm{s}} \cdot V'_{\mathrm{o}}} - \beta^2 - 3\beta\right)} \tag{2.16}$$

The analytical investigation of positive OP1 follows the same steps that have been walked through in this section, and lead as well to the same results, that can be simply achieved by making the following substitution :

$$\phi_{\mathrm{pos}} = -\left(\frac{1}{2} - \beta\right) + \phi_{\mathrm{neg}} \tag{2.17}$$

2.2.2 Operation Mode 2

The converter enters in the second operation mode whenever the DC/DC devices has to transmit a low power due to the application of a low load. Analitically, the converter works in OP2 with a positive power transfer whenever $\frac{\beta-0.5}{2} < \phi < 0$ and $\beta < \phi < \frac{\beta+0.5}{2}$, while works in OP2 with a negative power whenever $\beta - 0.5 < \phi < \frac{\beta-0.5}{2}$ and $\frac{\beta+0.5}{2} < \phi < 0.5$. Fig 2.13 shows voltage and current waveforms for a negative phase-shift that result in a negative power flow; during this section, an analitical investigation of OP2 is carried out with an identical approach to the previous section in which OP1 has been explained.

As already seen, the inductor current has to be investigated during a switching period, as it rapresents the only state variable of the system. Depending on the voltage across this element, the current varies linearly in time, causing the power flow. The semplifications already made are still applied during the folling steps:

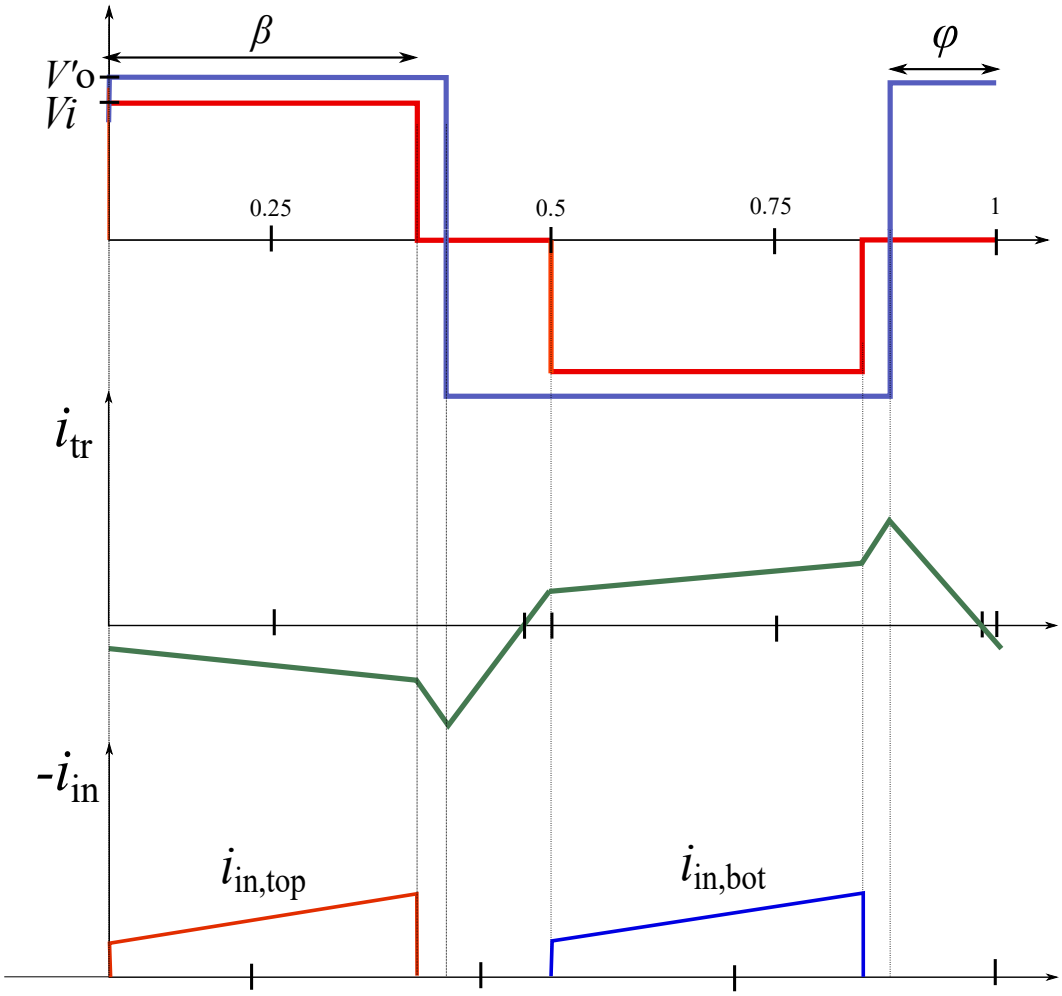

Figure 2.13: The picture illustrates voltage and current waveforms whenever $\beta - 0.5 < \phi < \frac{\beta - 0.5}{2}$. The NPC input current is negative, therefore the power flows from the NPC to the H-bridge.

$$0 < x < \beta : \qquad i_{\mathrm{tr}}(x) = \frac{V_{\mathrm{i}} - V'_{\mathrm{o}}}{f L_{\mathrm{s}}} \cdot x + i_{\mathrm{tr}}(0) \tag{2.18}$$

$$i_{\mathrm{tr}}(0) = \frac{-V_{\mathrm{i}} \cdot \frac{\beta}{2} + V'_{\mathrm{o}} \cdot (\frac{1}{4} - \phi)}{f L_{\mathrm{s}}} \tag{2.19}$$

$$0 < x < 0.5 - \phi : \qquad i_{\mathrm{tr}}(x) = \frac{-V'_{\mathrm{o}}}{fL_{\mathrm{s}}} \cdot x + i_{\mathrm{tr}}(\beta) \tag{2.20}$$

$$i_{\mathrm{tr}}(\beta) = \frac{V'_{\mathrm{o}}(\frac{1}{4} - \frac{\beta}{4} + \phi) + V_{\mathrm{i}} \cdot \frac{\beta}{2}}{fL_{\mathrm{s}}} \tag{2.21}$$

$$0.5 - \phi < x < 0.5 : \qquad i_{\mathrm{tr}}(x) = \frac{-(V'_{\mathrm{o}} + V_{\mathrm{i}})}{fL_{\mathrm{s}}} \cdot x + i_{\mathrm{tr}}(0.5 - \phi) \tag{2.22}$$

$$i_{\mathrm{tr}}(0.5 - \phi) = \frac{V'_{\mathrm{o}}(\frac{1}{4} - \frac{\beta}{4} + \phi) + V_{\mathrm{i}} \cdot \frac{\beta}{2}}{fL_{\mathrm{s}}} \tag{2.23}$$

The current flowing in the transformer during the second half-cycle can be easily obtained thanks to symmetry, as already seen in the previous subsection:

$$0.5 < x < 1 : \qquad i_{\mathrm{tr}}(x) = - i_{\mathrm{tr}}(x - 0.5) \tag{2.24}$$

The average current as output of the NPC is double the average current that flows through the top bus of the converter; this current flows only during the NPC high state, therefore between $0 < x < \beta$. This value can be obtained solving the integral :

$$I_{\mathrm{av}} = 2 \cdot \frac{1}{1} \int_0^1 i_{\mathrm{pr}}(x)\,\mathrm{d}x = 2 \int_0^\beta \left[\frac{V_{\mathrm{i}} - V'_{\mathrm{o}}}{fL_{\mathrm{s}}} \cdot x + i_{\mathrm{tr}}(0) \right] \mathrm{d}x \tag{2.25}$$

The solution yelded is :

$$I_{\mathrm{av}} = 2\frac{V'_{\mathrm{o}} \cdot \beta}{fL_{\mathrm{s}}} \left(\frac{1}{2} - \beta - 2\phi \right) \tag{2.26}$$

Scaling up the formula obtained by the constant primary voltage leads to the active transferred power.

$$P_{=} V_{\mathrm{i}} I_{\mathrm{avg}} = 2\frac{V_{\mathrm{i}} \cdot V'_{\mathrm{o}}}{fL_{\mathrm{s}}} \left(\frac{1}{2} - \beta - 2\phi \right) \tag{2.27}$$

Since this formula is valid for $\beta - 0.5 < \phi < 0$, is easy to observe that if $\frac{\beta - 0.5}{2} < \phi < 0$, the solution yelded is positive, otherwise the power results negative. The maximum positive power flow is transmitted for $\phi = 0$ and is equal to:

$$P_{\text{max,pos}} = \frac{V_{\text{i}} \cdot V'_{\text{o}}}{f L_{\text{s}}} \beta \left(\frac{1}{2} - \beta \right) \tag{2.28}$$

Increasing negatively the shifting, will result in a zero power transfer $P = 0$ whenever the following condition is met:

$$\phi = \frac{1}{4} - \frac{\beta}{2} \tag{2.29}$$

The phase angle at which the maximum negative power transfer in OP2 is met for a shifting equal to:

$$\phi_{\text{max,neg}} = \beta - \frac{1}{2} \tag{2.30}$$

Thanks to symmetry, the maximum power transfer is equal to the maximum negative one.

$$P_{\text{max,neg}} = -P_{\text{max,pos}} \tag{2.31}$$

This analytical investigation has proven that the maximum power transfer during OP2 is equal to the minimum active power converted into OP1.

$$P_{\text{max,OP2}} = P_{\text{min,OP1}} \tag{2.32}$$

2.2.3 Summary

In this chapter the analitical investigations of the two operating modes of converter, OP1 and OP2, have been carried out. The knowledge of the transformer current during at least half switching period is a preliminary requirement in order to draw the input (or output) current through the NPC terminals; the active power transfer can be then calculated if the voltage is known and the average input current has been calculated. Thanks to symmetry, is not needed to analyze the equations for both negative and positive power transfer of same operating condition, since they both yeld the same result with inverted sign. The equations obtained show that OP1 is an operating condition in which the converter is able to feed a great active power and is therefore able to supply a very high load. OP2 instead is prefered when the converter has to be limited in power. Due to the voltages value assumed and the transforming ratio, $V_{\text{i}} < V'_{\text{o}}$ is an always true relationship, that leads to a non zero power altough a zero phase shift is applied. This offset has to be taken into consideration if the converter wants to transmit a zero power transfer. Fig. 2.14 synthetize the results obtained, showing in which operating condition the converter works depending on the applied phase shift. The blue line rapresents qualitatively the magnitute of the power transferred as a function of the phase angle. Since in the whole phase-shift range possibilities the converter can operate in -OP2 (and OP2)in two intervals, generally it is always better to apply the smallest phase-shift possible: the reason lies behind the higher voltage drop on the inductor,

which determines the same output of the average current, but determines also higher losses of the core. That's the reason why, if two phase- shift determine the same output, the user should design a control that optimizes the losses.

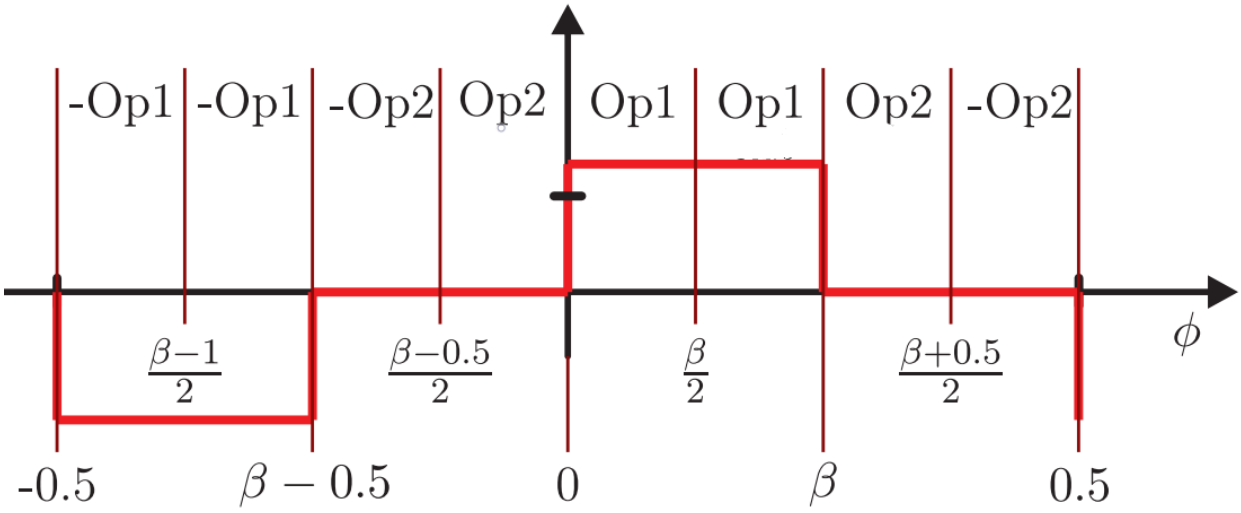

Figure 2.14: The figure illustrates in which operation mode the converter works depending on the phase shift; the red line shows that in OP1 the power transfer is positive and relevant, as opposed in OP2.

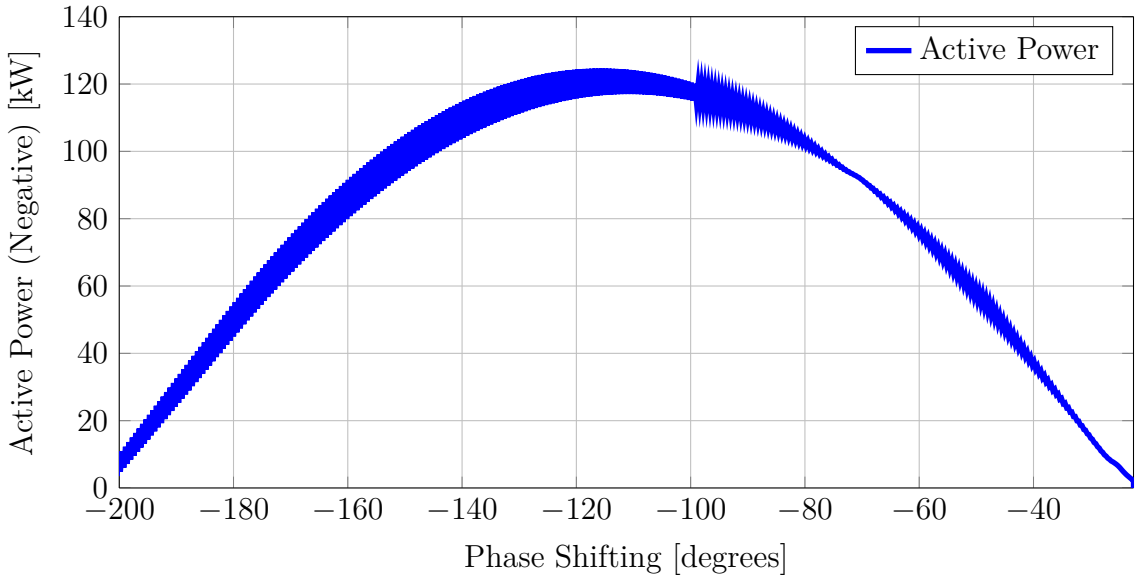

Figure 2.15: The figure rapresent the result collected through a simulation in which a progressively increasing negative shifting has been applied. In the simulation, $\beta = 0.375$,$V_{\mathrm{i}} = 2500V$,$V_{\mathrm{o}} = 530V$ while the phase angle is sweeped between -22.5 and -200 degrees.The simulation proves that the maximum is met with a phase angle equal to -110 degrees, as expected from the analytical investigation with the assumed value of β.

3 Fundamentals of FPGA

3.1 Introduction

In order to achieve the desidered modulation of the converter, switching signals must be generated and sent to the IGBTs. This is done with an FPGA, which has been programmed to fulfill the already mentioned task togheter with the execution of safety algorithms to safeguard endangered equipment and people during faults. FPGA stands for Field Programmable Gate Array, which means it is structured as an array of inter-connected digital circuits that can be specified through an hardware description language (HDL). The user, through the dedicated programming language to this device, is able to wire togheter programmable logic blocks which the FPGA is made of. This recombination allows to perform very complex functions as well as easy tasks such as logic gates. The strenght of using an FPGA rather than a microcontroller stands in the fact that the latter succeeds its tasks by executing instructions in a sequential fashion, which means that the operations are inherently constrained: it is impossible for the mentioned device to accomplish simultaneously multiple processing tasks. Assuming the switching of a leg of inverter can easily figure the strenght of the FPGA compared to a microcontroller : while the first achieves simultaneous and safe switching, the second generates a latch between the two operations, that may cause a short circuit. Fig 3.1. Thanks to dedicated hardware, most microcontrollers are able to overcome this software limitation.

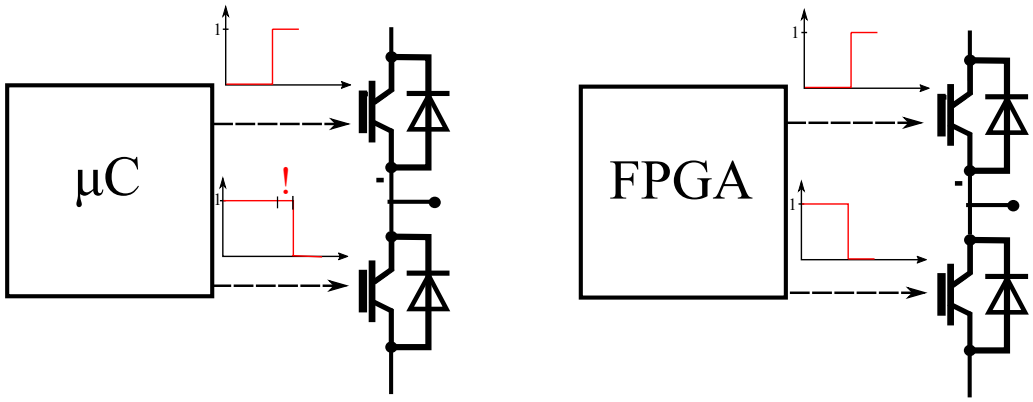

Figure 3.1: The strenght of the FPGA compared to a μC: altough both aim is to switch the IGBTs simultaneously, the μC is costrained to execute commands sequentially.

3.2 ISE Design Suite

As a matter of facts, nowadays the main manufacturers of FPGA are Xilinx and Altera and each of them provide a software for the development of the code that will be executed by the FPGA. The FPGA device that has been programmed by the author is Xilinx Spartan®-6, and it has been accomplished using Xilinx ISE design suite. The user is in fact able to "wire-togheter" the configurable logic blocks the FPGA is made of through this tailored development enviroment. The two main features of ISE Design Suite that have been used to design and test the code were:

- Xilinx Platform Studio (XPS) - provides an integrated environment for creating software and hardware specification flows for embedded processor systems based on MicroBlaze and PowerPC processors. It also provides an editor and a project management interface to create and edit source code. XPS allows you to customize tool flow configuration options and provides a graphical system editor for connection of processors, peripherals, and buses. [13]
- System Generator for DSP - allows the user to define and verify complete DSP systems using industry-standard tools from The MathWorks. When using System Generator, previous experience with Xilinx devices or RTL design methodologies is not required. Designs are captured in the DSP-friendly Simulink® modeling environment using a Xilinx-specific blockset. All of the downstream synthesis and implementation steps are automatically performed to generate a device programming file. [13]

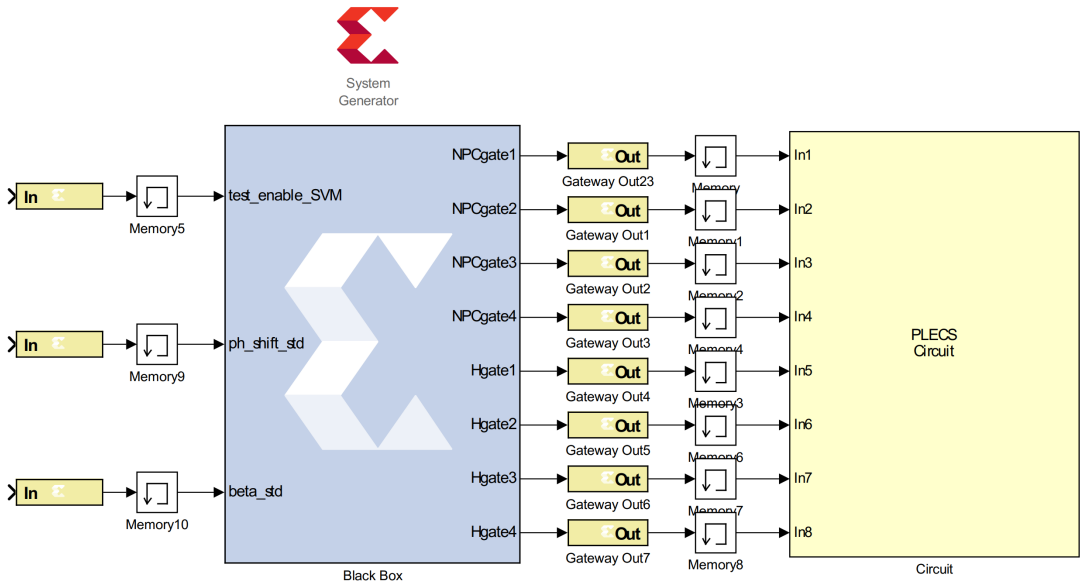

Figure 3.2: Simulations for testing the VHDL code have been run on System Generator, a Xilinx Toolbox for Simulink enviroment. Xilinx's "black box" is programmed with the developed VHDL code and simulates the physical board whose clock frequency is 50 Mhz.

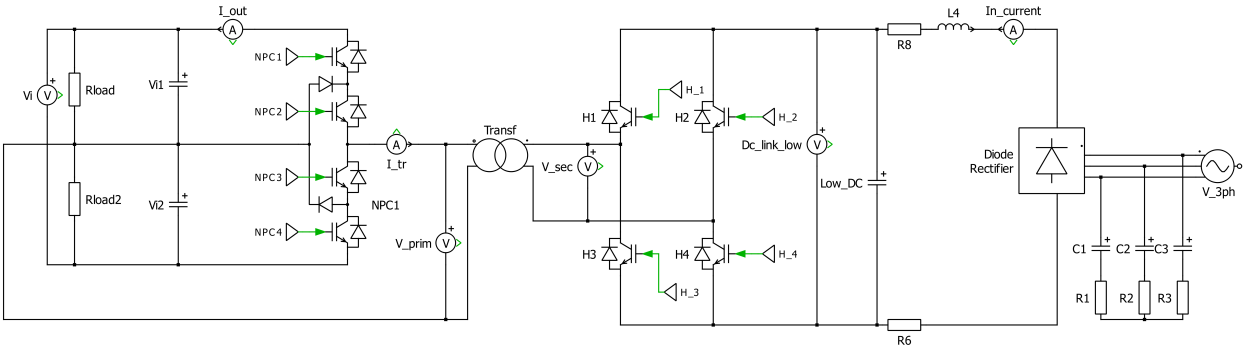

Figure 3.3: The DC/DC converter schematic is simulated in PLECS Blockset.

3.3 Steps for programming an FPGA

FPGA can be programmed in different programming languages. One of them, which has been used, is VHDL, which stands for Hardware description language for Very High Speed Integrated circuit. Altough it has the same contruct of a typical programming language, like *if,else..* this language has some peculiarities, since it describes functions executed by hardware components. Those functions are basically the signals exchanged by various object that build togheter the physical system, and are exchanged simultaneously as already mentioned.

The tipical steps of a VHDL code development are:

- In the first phase how the component seen from outside, also defined as ENTITY, is described: its inputs and outputs ports, configuration parameters, the widths of buses and delay times.
- In the second one, the user has to design the ARCHITECTURE, so the description of how the internal structure behaves: this is by far the most challenging phase since it rapresents how the actual circuitry functions.

Altough the user can design an ARCHITECTURE the way it fits its purpose, generally two fashions of design are used : *behavioural* or *structural*. With the first, *behavioural*, the functional relationship between inputs and outputs can be described by means of a function or an algorithm. Applying the second style of design, one can rapresent the internal structure made of its low-level components and their connections, so one can already choose with which objects the functionality has to be achieved and how they are inter-connected (RTL: *Register transfer level*). The last step, which is automatically done by the code development enviroment, is the synthetization of a *netlist*, therefore VHDL is compiled and mapped into the circuit.

3.4 Generation of switching pulses

Now some insights about the VHDL code that has been developed are given. The entity consists of eight outputs which are the switching signals to be sent to the IGBTs, two 19 bits Data registers exchangeded between the DSP and the FPGA via SPI, and the clock, which is defined in the entity but it is not an input as it is embedded already in the FPGA.

To realize the switching pulses, two counters, one for the NPC IGBTs and one for the H-bridge, have been realized, which sum up during each clock event. Because Xilinx Spartan 6 has an internal clock whose frequency is 50 MHz, the two counters have to reach 50.000 before being reset to zero to realize a switching frequency of 1kHz. The relationship is rather simple :

$$\frac{f_{\mathrm{FPGA}}}{f_{\mathrm{SW}}} = Counter_{\max} \tag{3.1}$$

The NPC during one period feeds to the transformer respectively an high state, zero, low and again zero state, therefore, four different events must happen, and each of them will generate switching pulses for each IGBT. This is realized by setting four numerical tresholds: each time the counter reaches one of them, the switching signals change according to the state of the NPC to be applied. One example is as follows : if $\beta = 0.375$, the counter has to sum up to 50,000*0.375=18,750 counts before commutating the NPC from an high to a zero state. Each state is defined by four sets of value, which rapresent the four IGBTs on/off state, therefore an high to zero commutation happens if the FPGA signals change according to the pattern showed in Fig 3.3:

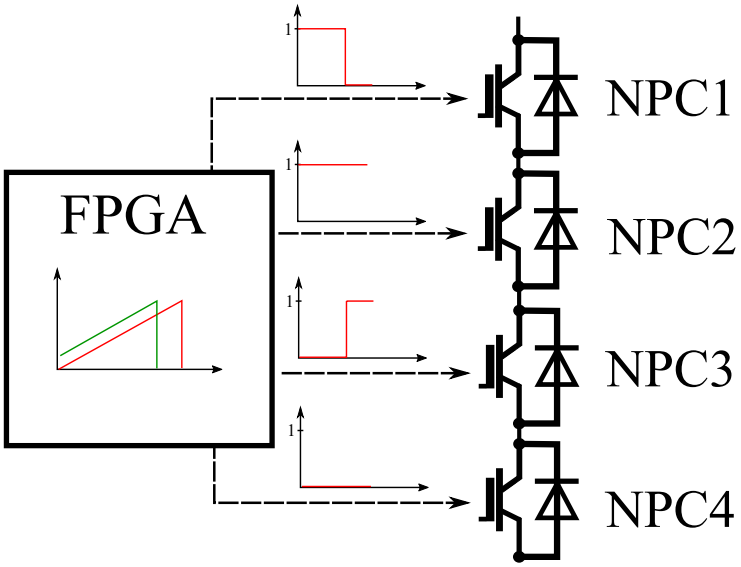

Figure 3.4: The FPGA sends generates and sends the switching pulses to all 8 IGBTs of the converter.

As for the H-bridge, only two switching instants can be observed, since its output is a squarevawe. Applying a phase shift means that either the set of threshold values have to be traslated or the the counter has to be shifted. The second solution has been implemented : if the phase shift is positive, the primary is leading, otherwise it is the secondary voltage to lead. The counters have same logic, as shown in Fig 3.5 : in the first case the H-bridge counter is shifted to the left, while the NPC counts from zero; on the contrary, when the phase-shift is positive, the NPC counter is shiftet while the H-bridge one counts from the axis origin.

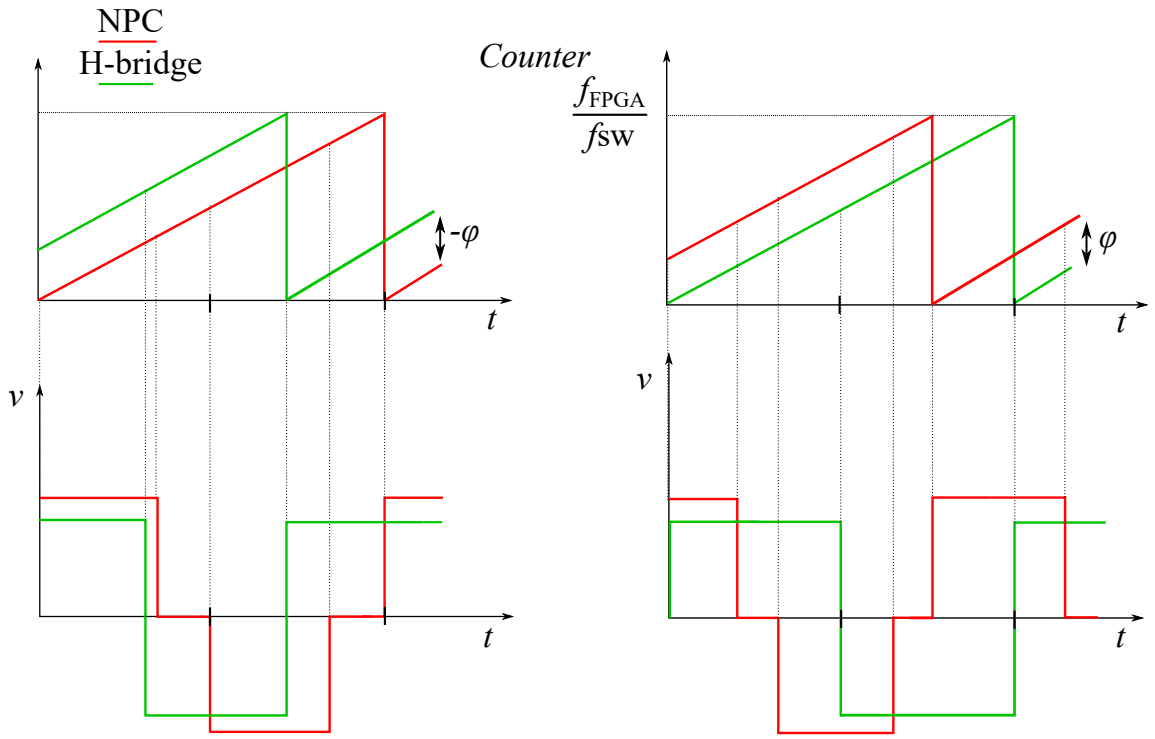

Figure 3.5: The FPGA is embedded with two counters, shifted as in figure; whenever a treshold is met, which corresponds to a switching instant, the IGBT drive signals are updated.

Which phase angle has to be applied is dictated by the control structure embedded in the DSP : given a reference that has to be reached and kept at steady state, a discretized PI controller gives as output the phase-shift that is able to power the load meanwhile matching the voltage requirement. This value is exchanged between the DSP and FPGA through the SPI ,a communication protocol which has been embedded in both platforms.

The switching is enabled by the user whenever the flag *svm enable*is switched high, and it only occurs if no faults are detected : whenever a manual switch is pushed by the user, or a fault such as overcurrent or overvoltages is detected, the converter is shut down by disabling *svm-enable*; a relay decouples the converter from the low voltage three-phase grid and the

DC-link capacitors discharge on discharging resistors. Whenever the fault has been cleared, the user has to manually reset the system. The latest feature has been implemented to prevent that any flickering signal intermittently turns on and off the converter.

The board also applies a delay to the IGBT that turn on: this procedure has to be applied since the devices do not ideally interrupt the current instantly; if this is instead assumed and no delay is introduced, there is an high chance that a short circuit would happen, flowing across the turning-on switch and a switch connected in series that hasn't interrupted the current. The FPGA, whenever a rising edge of a switching signal is detected, counts up to 15μs; before the counter has reached a numerical value which corresponds to that time interval, its output is zero and the IGBT is still in off state. Right after the count has finished, the IGBT can be turned on. Falling edges, which rapresent turn-off switching signals, are instead not affected by the delay.

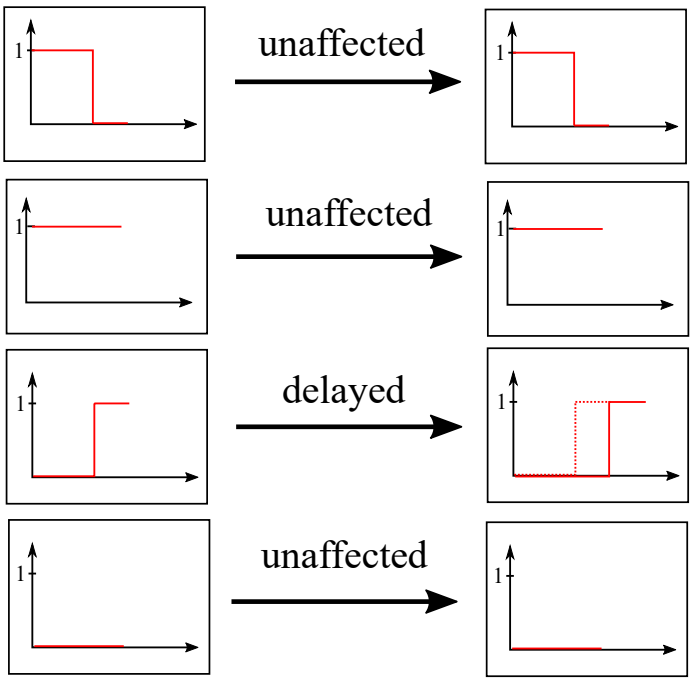

Figure 3.6: The figure rapresent the output result of a delay function executed by the FPGA. Only the rising edges are delayed, to ensure that all series devices to the switching IGBT are in blocking mode.

3.5 Summary

In this chapter, fundamentals of FPGA have been shown. The FPGA is a device which is constituted by several logic blocks that the user can "wire togheter", to create an hardware circuit that is able to execute rather complex instructions. It is described with VHDL, a programming language dedicated to this device. Thanks to its ability to simultaneously execute commands, the FPGA can achieve with great performances tasks such as the generation of switching pulses of power electronic devices. Xilinx Spartan6, has been embedded with two counters, that are matched with constant values which rapresent the switching instant of the H-bridge and NPC IGBTs. If an IGBT has to be switched on, the FPGA also applies a dead-time according to the IGBT module datasheet, in order to prevent any short circuit across the on-switching IGBT and a series connected device which hasn't interrupted yet the current.

4 Control strategy

4.1 Introduction

Such converter will, in the future, be connected to a 7MW converter, realized at RWTH's institute for Power Generation and Storage systems. In fact, up to 40 kW is a magnitude of transferred power which corresponds to the losses of the mentioned experimental device. Since the converter will be connected to an active load, the original control strategy that has been designed was a cascaded voltage-current control, in which both NPC voltage and output current are regulated. Therefore, such strategy would ensure a steady voltage equal to the reference meanwhile controlling and limiting the current. Currently though, due to lacking of high precision current sensors, unsatisfactory results collected from the simulations and lacking of equipment to test up to 5kV, only a voltage controller has been tested experimentally with a series of resistances as load. Both controls will be shown and their results presented. To ensure a zero steady-state error, Proportiona Integral controllers have been designed and tuned. It consists of a proportional gain and an integrator, which introduce a pole, to obtain infinite gain in and zero error in steady-state conditions, and a zero, which can be opportunely placed to increase the phase margin.

$$G_{\mathrm{PI}}(s) = \frac{K_{\mathrm{I}} \cdot (1 + \tau s)}{s} = K_{\mathrm{p}} + \frac{K_{\mathrm{I}}}{s} \tag{4.1}$$

4.2 Control structure

As shown in Fig. 4.1, the control originally simulated consists in a cascaded structure that is able to drive the primary voltage and to control the output current of the converter. The reference voltage, set to 5kV, is compared to the measured, low-pass filtered value of the voltage accross the NPC capacitors. A proportional-integral controller amplifies the error as a reference average current that has to flow as output. This output is then compared to the measured current, and a second PI calculates the phase-shift that has to be applied between primary and secondary voltage to have the given reference input.

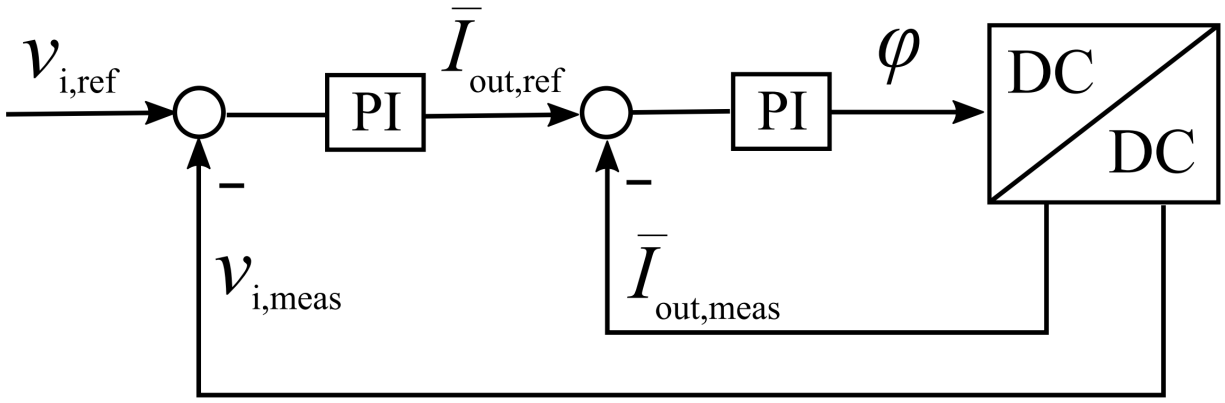

Figure 4.1: The control strategy that will, once the converter hardware setup is completed, be optimized and implemented.

4.3 PI tuning

For the tuning of the PI voltage controller, the following semplifications take place :

- Inner current loop assumed to have infinite bandwidth
- Kp tuned assuming only proportional open-loop system
- The delay introduced by the modulation is neglected
- The bandwidth is assumed to be 40 Hz
- Sensors are assumed with infinite bandwidth, therefore no delay is introduced

The PI has been tuned according to chapter 5 of [5]. Further literature can be found in [8], [9], [11]. Practical approaches can be also be attempted, as explained in [20], [12], [4]. The control structure can be now simplified according to Fig 4.2; The current loop is shown as a unitary transfer function: this conditions facilitates the tuning of the controllers, since both current and voltage PI can be designed independently. The open-loop transfer function of the system is:

$$G_{\mathrm{ol}}(s) = \frac{K_{\mathrm{p}}}{sC} \tag{4.2}$$

Assuming $|G_{\mathrm{ol}}(j\omega_{\mathrm{bw}})| = 1$, the proportional can be obtained :

$$K_{\mathrm{p}} = \omega_{\mathrm{bw}} C = 2\pi f_{\mathrm{bw}} C \tag{4.3}$$

The cut- off frequency of the zero is placed one decade below ω_{bw} not to reduce the phase margin and gain instability, therefore $\tau = \frac{10}{\omega_{\mathrm{bw}}}$. The integral gain is :

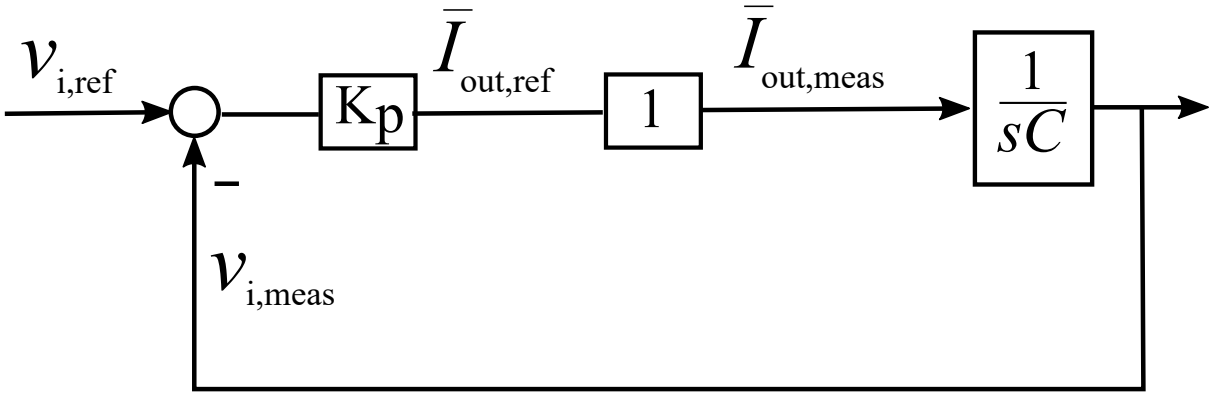

Figure 4.2: Assuming the inner current loop to have a very large bandwidth, it can be rapresented as a unitary gain inside the voltage loop.

$$K_{\mathrm{I}} = \frac{K_{\mathrm{p}}}{\tau} \tag{4.4}$$

Very similarly the PI controller of the current loop has been designed, this time assuming a bandwidth of 300 Hz. The PI output is a phase-shift, that will be communicated and executed by the FPGA. The phase-shift, as seen in the second chapter of this work, modules the voltage drop over the effective inductance, thus causing the power flow. This leads to the conclusion that $\frac{1}{sL}$ rapresents one pole of the current loop, which has to be considered for an optimal PI tuning. The steps of this second PI design are the same of the previous case:

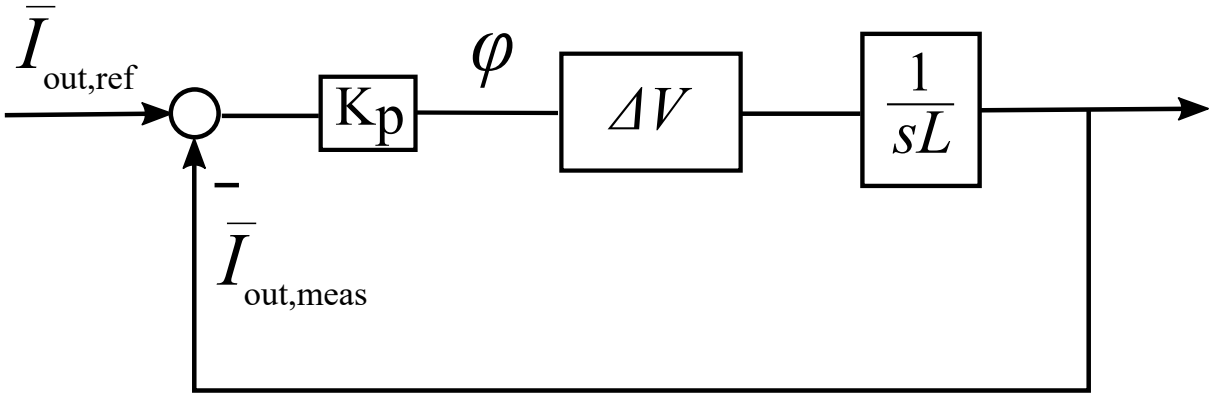

Figure 4.3: The phase shift modifies the voltage drop over the inductor, causing its magnetization or demagnetization depending on the sign of ΔV.

$$G_{\mathrm{ol}}(s) = \frac{K_{\mathrm{p}}}{sL} \tag{4.5}$$

Assuming once again $|G_{\mathrm{ol}}(j\omega_{\mathrm{bw}})| = 1$, the proportional gain can be obtained :

$$K_{\mathrm{p}} = \omega_{\mathrm{bw}} L = 2\pi f_{\mathrm{bw}} L \tag{4.6}$$

The integral gain is calculated as previously, placing the zero one decade below the cut-off frequency.

$$K_{\mathrm{I}} = \frac{K_{\mathrm{p}}}{\tau} \tag{4.7}$$

Both PI have a saturation threshold : if the proportional and the integral exceed a certain value, they are limited to the maximum allowable. This means that the maximum output current that the controller can ask as a reference, is set to maximum 20A, which corresponds to 100kW of power transmission; the phase shift is instead limited at the value which corresponds to the maximum transferred power. Those values of course exceed the maximum power that the converter can currently transfer : fuses would in fact trip whenever a power of around 40 kW is transmitted. Whenever the control strategy will be implemented on the system, a limitation according to the capabilities of the converter will be set. Fig 4.4 shows the performance of the control obtained with simulations. The evolution of the measured voltage to a step of reference voltage is fast, stable, with zero steady state error and with no overshoot. Later, at instant $t = 0.3s$,the load increases, and to the converter a step of around 25kW is asked. The response of the voltage loop is satisfactory, as it recovers from the load step in around 200ms. As for the current loop, its response is less satisfactory, as in steady state it has zero error, but the response to a step of the load is really slow. This is the reason why no feed-forward has been implemented : if the reference current is always greater than the actual current, the feedforward will cause the voltage loop to fail or to be unstable. Simulations have shown that increasing or decreasing the bandwidth of the loop doesn't improve the efficiency of the response; therefore, a different design approach has to be taken.

Most probably, the error of this control has to be adressed to the fact that the load current wants to be controlled: in this case, a current through a resistor connected in parallel to a fixed voltage source can't be controlled, as it is enforced by Ohm's law. Most probably, the variable to be controlled has to be the current flowing into the inductor, that is equal to current flowing into the capacitor and the load. Considering the load current as a disturbance, the current into the inductor can be integrated in time, giving as output the voltage to be fed back in the voltage loop.

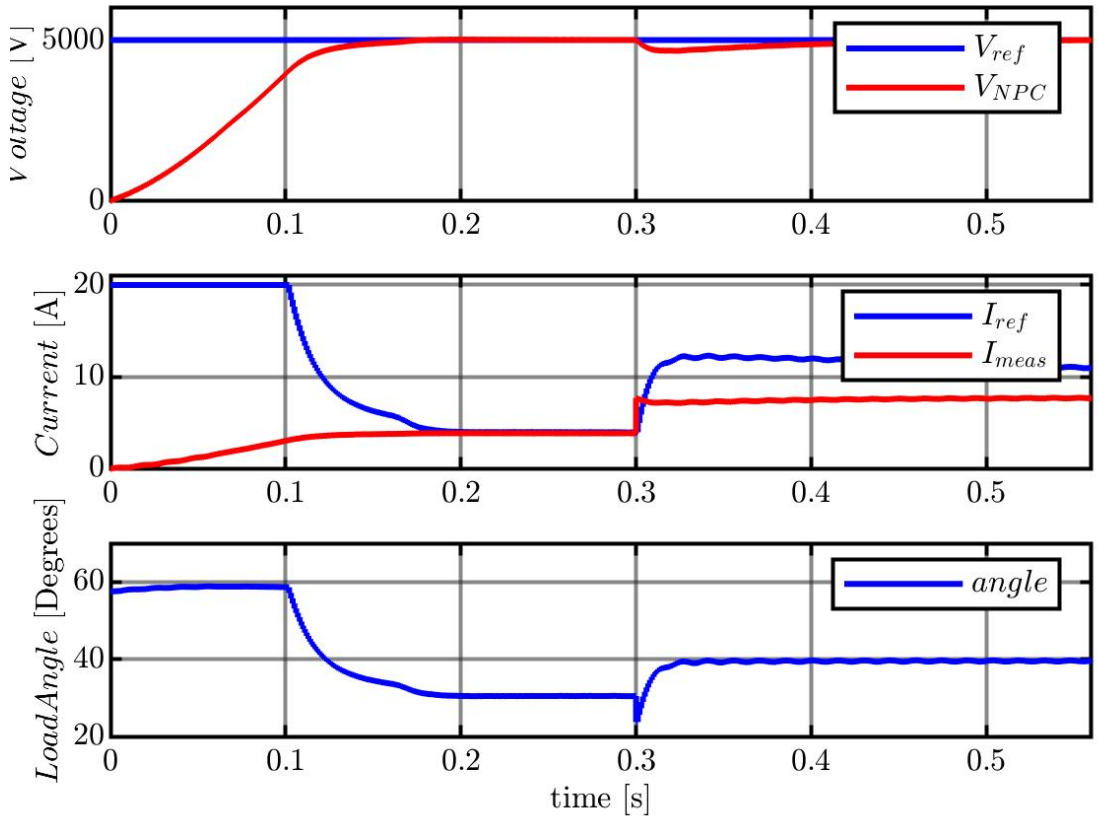

Figure 4.4: Simulation results of the control structure are shown; The voltage loop response is stable, fast and rejects disturbances quite effectively. The current loop is instead unsatisfactory, since reference and true value match after a very long transitory.

4.4 Control Structure of the Experimental Setup

As already mentioned, the lack of appropriate equipment for medium voltage measurement, the low precision of current sensors and the unsatisfactory simulation results obtained with the shown cascaded control, have brough to the realization of a simpler control.

This is realized, as shown in Fig 4.5, with a simple voltage controller. The PI controller calculates the error and amplifies it as a reference phase-shift. Due to imprecise voltage measurements, the PI controller has been tuned, like in the previous section, assuming its output is a current reference and choosing a rather small bandwidth of 70 Hz. This causes the dynamic to be slower, but it avoids any overshoot due to delays introduced by the filtering of the measurement signals and the relatively low bandiwdth of the sensors. To increase the response speed, a feedforward has been implemented : since the load is a resistance, to control the output voltage or the output current is the same, therefore, known the reference voltage, it can be easily calculated the reference current by means of Ohm's

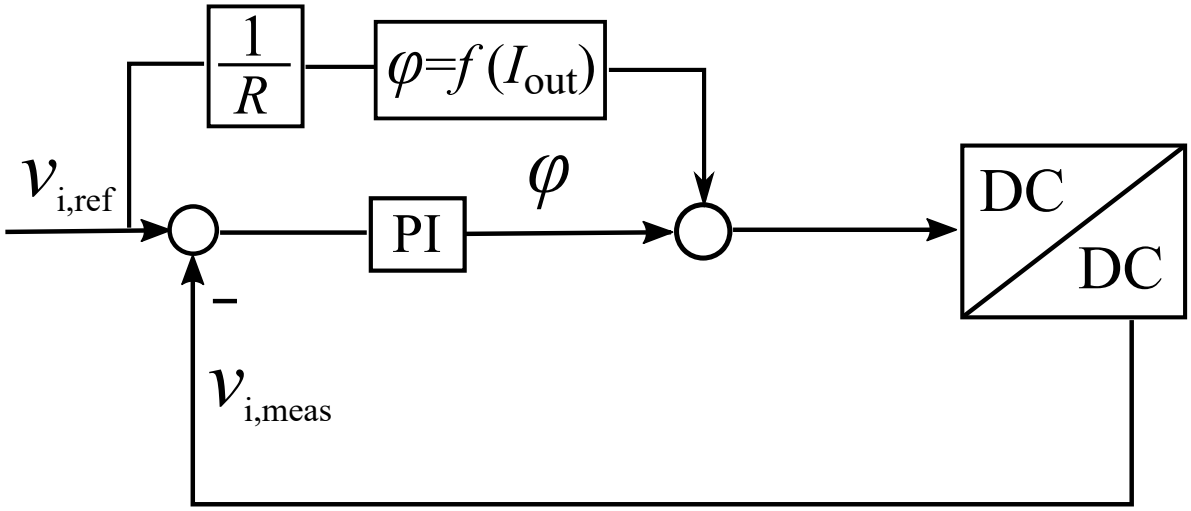

Figure 4.5: The control adopted during experimental setup. A slower PI avoids any overshoot caused by delays not taken into consideration, while a feedforward enhances the converter's dynamic.

law, which allows to feed to the modulator the phase-shift that meets the desidered current. Simulations results are shown in Fig 4.6.

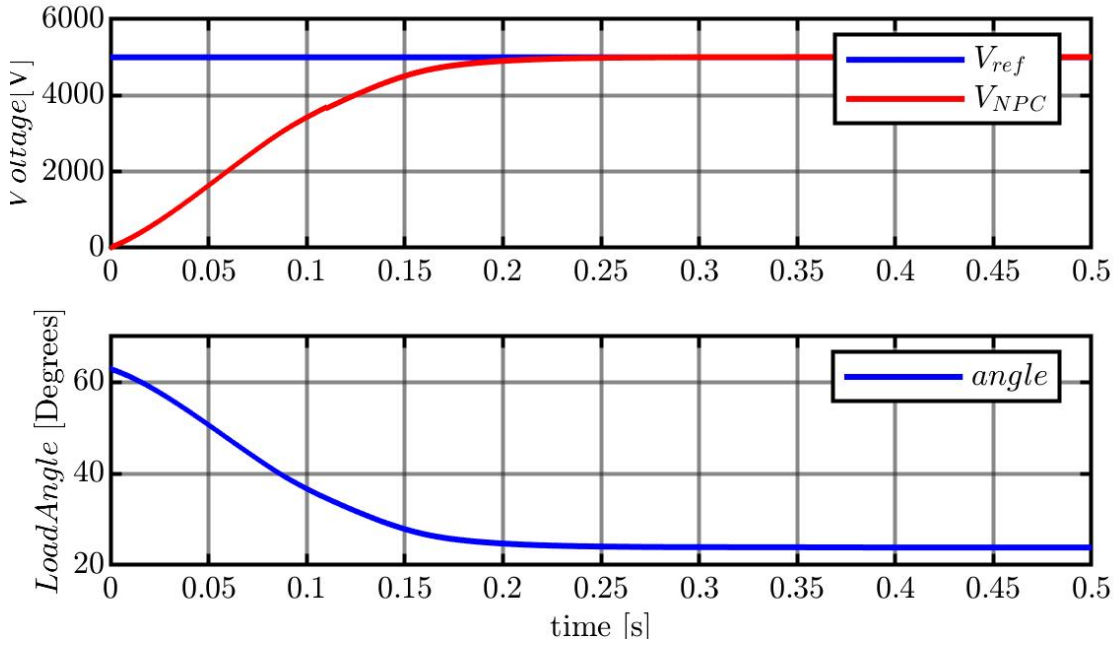

Figure 4.6: Simulation results of an only Voltage controller with feedforward.

4.5 Summary

In this chapter, two control strategies have been presented and their simulation results shown. The first is a cascaded voltage- current control, which has not been implemented because of the lack of reliable current measurement and because of unsatisfactory results. The PI controllers have been tuned by choosing a larger bandwidth of the inner current loop and a smaller one of the outer loop. The proportional gains were chosen according to the bandwidth and the physical variables of the system, such as the inductance for the current loop and the medium voltage capacitors for the slower controller, while the integral gain has been obtained by placing the zero one decade below the cut-off frequency. The results obtained with simulations are poor, and underline the bad control design: simulating with a resistor as a load, it has been observed that the controller is uneffective. To meet the temporary need of experimental results, a simpler and slower voltage control has been simulated and implemented on the control board DSP, which takes advantage of Ohm's law to feedforward a phase-shift which increases the response the a step of reference voltage.

5 Hardware Set-Up

In this chapter most of the author work is presented. The Dual Active Bridge is built, as already mentioned, with an NPC, H-bridge, medium frequency transformer, an inductor and a certain number of capacitors to ensure an high enough value of capacitance. The H-bridge is connected to the low voltage trìhree-phase grid through a three-phase diode rectifier and an inductance, installed as power factor corrector and to filter harmonics introduced by the passive converter. As for the control, it is enabled by a DSP which computes the phase-shift with the given information by voltage and current sensors, and then laters communicates its output to the FPGA via SPI communication protocol.

5.1 Control Board

Xilinx's Spartan6 and TI C2000 series TMS320F28335 processor are without any doubts the core of the control board.

TI manufactured DSP has been embedded with a large number of functionalities, such as communication and receiving data with the FPGA through SPI, communication with the converter's user interface realized in Labview, ADCs to convert analogical signals from measurement equipment, discretized proportional-integral controllers and lowpass filters to extract mean,noise-free values over each computational period. One crucial feature embedded in the processor is a fault code : whenever the values of measured currents and voltages exceed the maximum allowable, the converter is shut down, and the error that has occured is visible to the user as a lightened up red button on Labview's user interface. The user has to manually reset the system in order to re-run it again.

The control board also offers several LAN connections through Rj45 connectors, for the reception of signals coming from the measurement setup. The signal is then amplified with a differential operational amplifier, whose resistances can be tuned so that the full-scale value of the measurement corresponds to a Op Amp output of 3 Volts, which is the maximum voltage the ADC can receive. One advantage of using LAN cables to receive measurement signals is that it provides three additional wires, that can be employed to deliver to the sensors the required power supply to operate, as well as a reference bus. The leftover wire is used to provide a negative voltage wether it is a requirement for the sensor operation. The positive and negative voltages are fournished by a traco power DC/DC converter installed on the PCB, whose output is connected to all the LAN connections in parallel.

Using optical data as switching signals has nowadays become very popular since galvanic isolation between the control board and the converter is achieved. The control board in fact

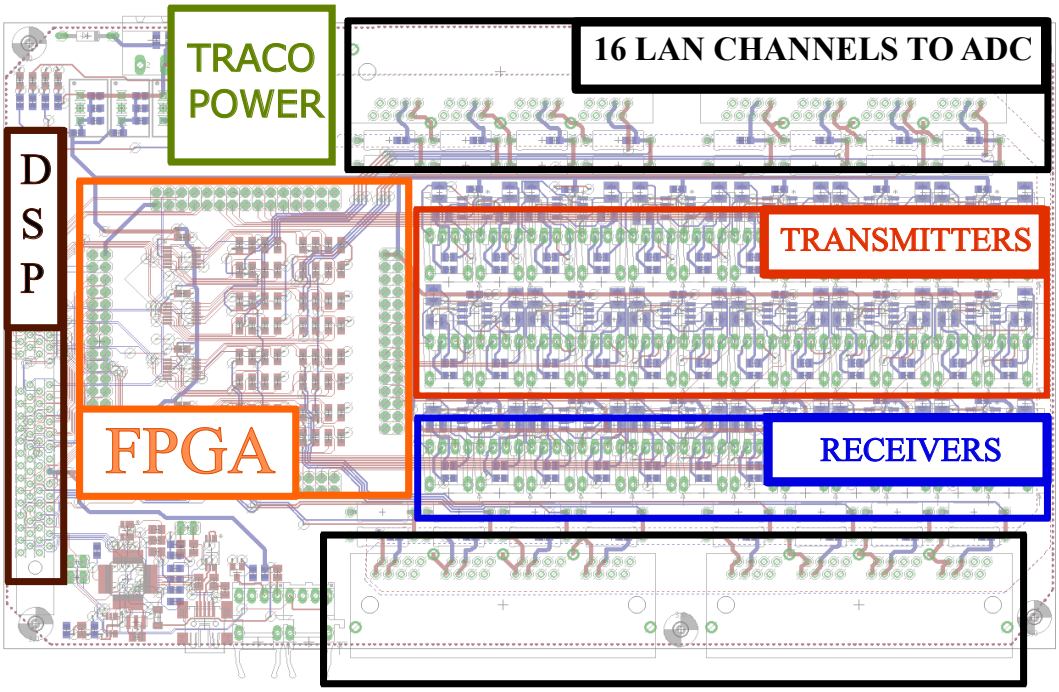

Figure 5.1: The control board that has been previously realized and now recommissioned for this project; It is equipped with an FPGA and DSP, transmitters and receivers of optical signals and RJ45 connectors through which the sensors are supplied and measurement signals are received.

is supplied with very low voltage and generally is not robust enough to stand noises due to a direct coupling with medium-voltage equipment. This is the reason why many optical receivers and transmitters are employed in this application. Specifically, transmitters are used to send switching pulses to the IGBTs, meanwhile to receivers is delivered the detection of any fault, which disable the modulation of the converter. This solution has been chosen since optical signals are EMI and noise-immune, therefore both mentioned signals do not flicker, regardlessly of the switches electromagnetic noisy activity.

5.2 Diode Rectifier and Pre-Charging Strategy

Fig 5.2 shows the passive converter which has been realized to obtain the low voltage DC-link. The three-phase voltage is rectified via a diode rectifier, which is able to impress around 530V as output. Protective fuses, which connect the rectifier to the grid, trip whenever the converter is overloaded or a fault happen, shutting down the current when its rms value surpasses 63A, a value which corresponds during normal operation at a transferred power of

approximatevely 40 kW; this limitation is also implemented in the control structure in order to avoid the failing of the fuses during normal operation.

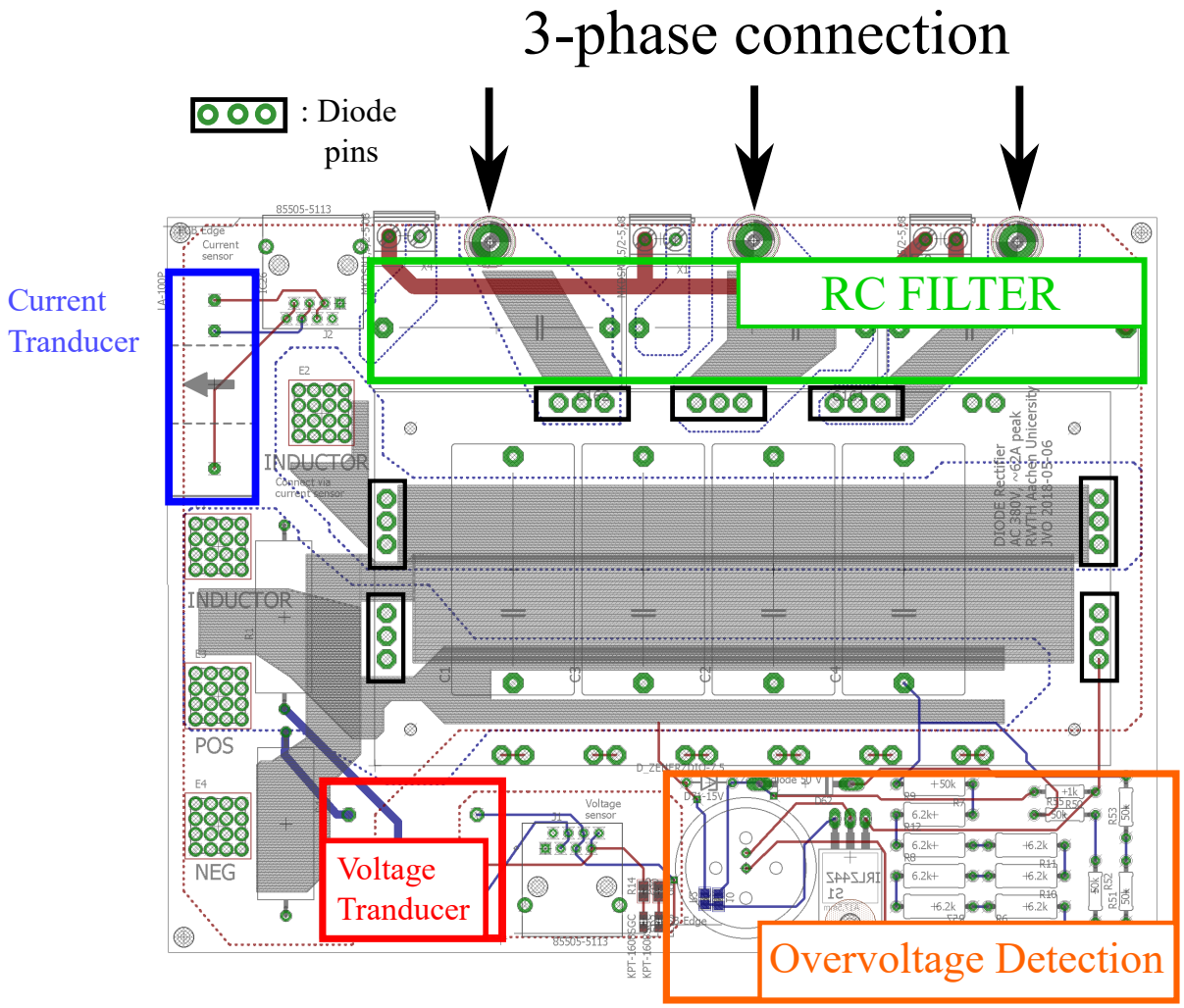

Figure 5.2: The passive rectifier schematic: the grey areas are copper stripes which allow a relatively small PCB able to carry high currents. In orange a circuit for overvoltage detection, equipped with a LED that turns on whenever the voltage exceeds 700V. The diodes are mounted on the bottom of the PCB. The converter is also able to filter harmonics thanks to an RC filter.

Since a rectification causes distortion of the grid voltage and current, an RC filter has been tuned to damp undesidered harmonics. To filter distortion, an inductance is also mounted after the diode rectifier. The relatively high current that the PCB has to sustain flows through copper stripes which have been soldered and covered with an insulating coating pen. It is possible to notice in the schematic two sensors, LEM la- 100 and Lp 25-p, which sample the DC-link voltage and the output current of the rectifier.

The capacitors which sustain the DC-link voltages are very large in capacitance, which

is equal to 11 mF : running the system without any pre-charging strategy would lead to very high inrush currents, causing overheating and degradation of conductors insulation, desoldering of PCB's contacts resulting in sparkles, damaging of the capacitors and in short failing of rather expensive equipment. The current is limited by a pre-charging circuit Fig. 5.5 :

- In order to enable the precharging, the user must manually activate a switch, that can only be on if the converter's cabinet is closed: this prevents anyone from being harmed during the converters operation. The cabinet is only open if this switch is off.
- Whenever a connection between the remote user interface to the converter and the control board is enstablished, a switching signal is sent to a normally-open relay, which connects the DC-Link to the three- phase grid (K1 in the figure)
- A relay (K2) is connected to a timer, set on 5s:whenever K1 is closed, K2 is open and the timer starts counting down, forcing the current to charge the capacitors through two 80 Ω resistances. The circuit evolves as a first order RC circuit with a time constant of $\tau = RC$. The design has been realized according to the heat dissipation capability of the resistors and the maximum temperature tolerated.
- After $\Delta t = 5$ seconds the relay closes, shorting the connection between the passive rectifier and DC-link capacitor. 5s is a more than sufficient time interval to fully charge the capacitors as it satisfies the relationship $\Delta t >> 6\tau$

At this point, the switching can be enabled by the user by flicking on Labview's user interface to the converter the switch *svm-enable*; This operation will be successfull only if no faults are detected. Fig 5.3 show the preliminary conditions that have to be met in order to turn on the converter. If faults, such as overcurrent, overvoltage, short circuit, lost connection between FPGA and DSP, or between the DSP and the user, the converter is shut down and *svm-enable* is forced to zero, meanwhile the converter is decoupled from the grid by opening the relay K1.

Enabling switching at this instant, moreover if the phase-shift is set to transmit an high power, would cause the abrubt application of medium-voltage capacitors the DC-link voltage heightened by the transformer winding ratio, causing high inrush currents that have to be limited to safeguard expensive equipment. The strategy applied, in order to prevent this to happen, is to rampup the H-Bridge duty cycle,increasing in time the non-zero voltage as output. This strategy permits a fast charging of the capacitors meanwhile limiting high currents, as seen in Fig. 5.4.

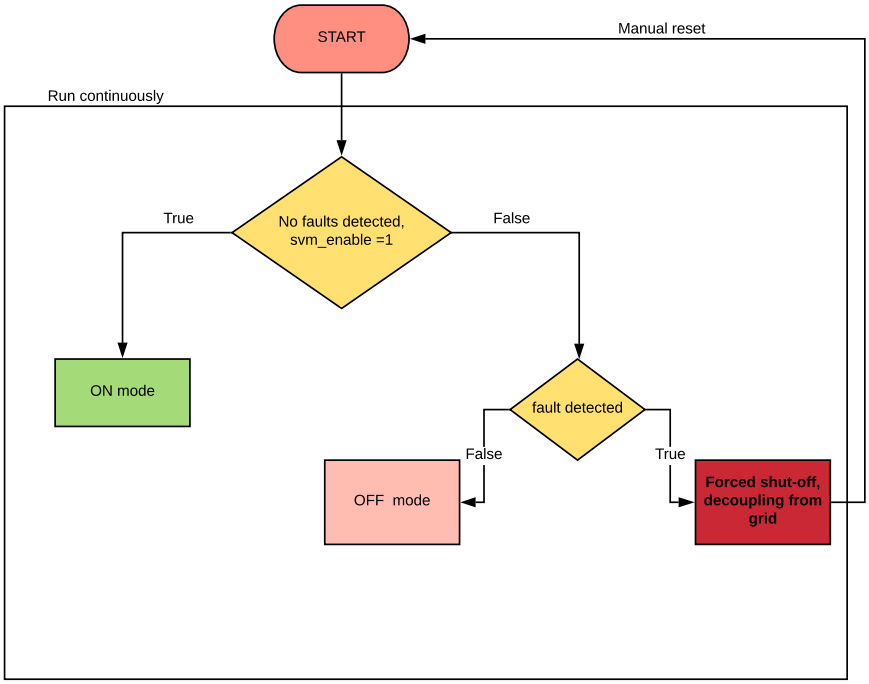

Figure 5.3: The safety concept of the converter :if *svm-enable* is high, the converter only switches if no faults are detected.

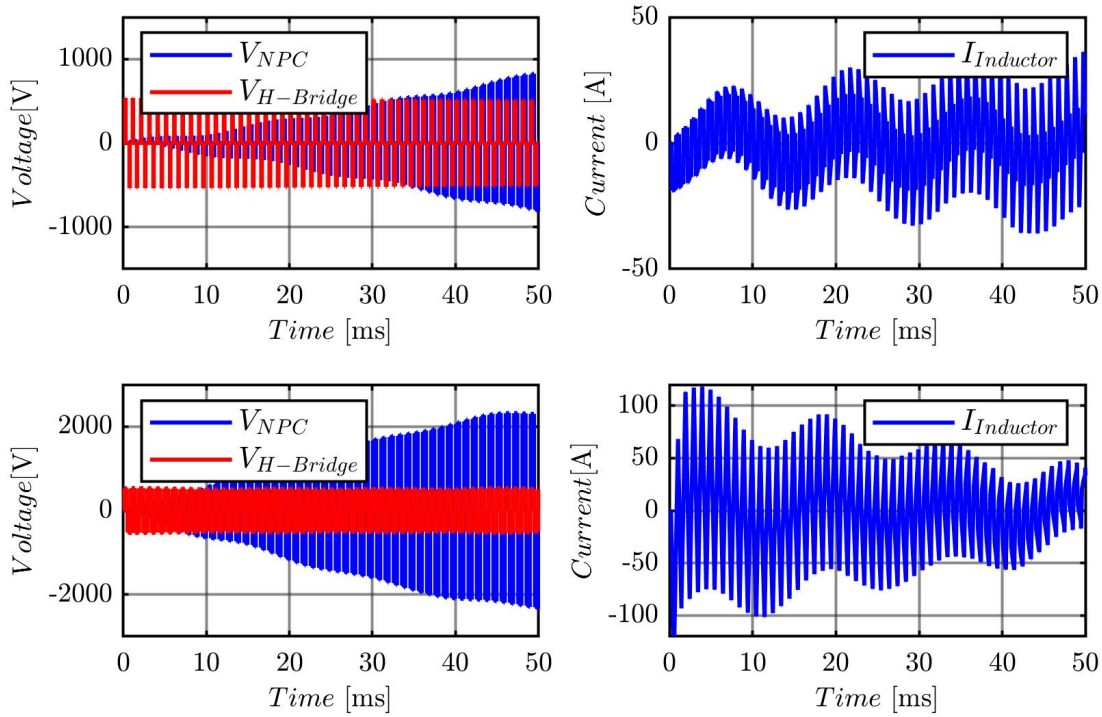

Figure 5.4: The current and voltages of the first row rapresent how effective is the reduction of inrush currents with a precharging strategy.

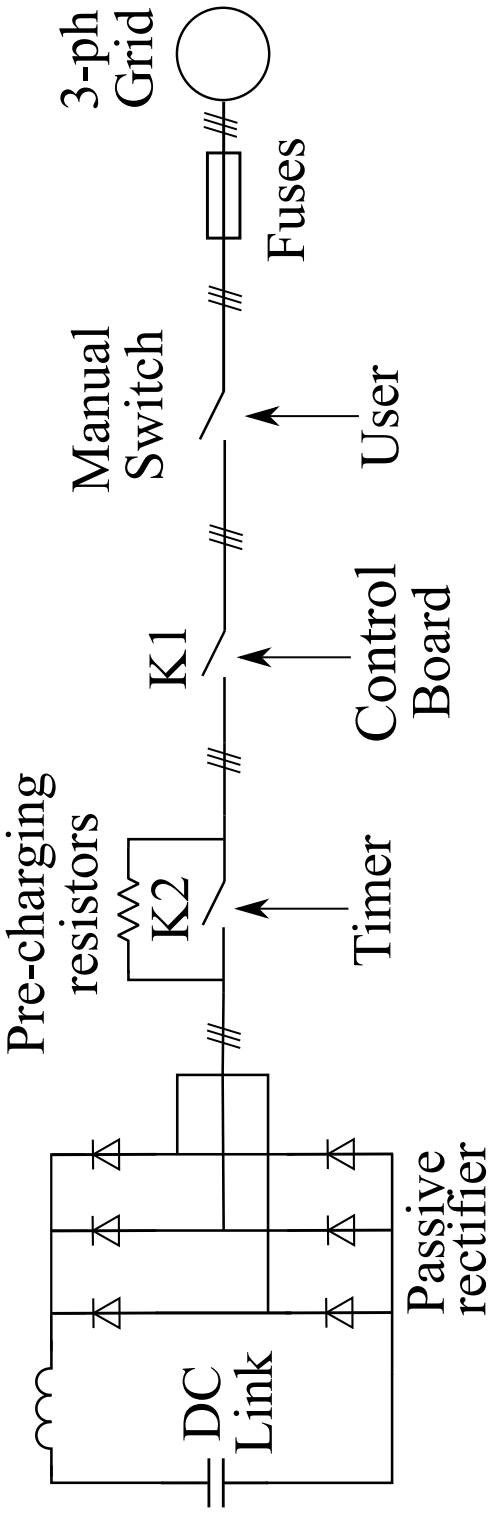

Figure 5.5: The picture illustrates the safety concept and its hardware realization, as well as the precharging circuit used to avoid high inrsuh current consequently the connection of the DC-link to the three-phase grid. The three-phase grid source in the picture is in reality a transformer, which is able to galvanically isolate the system from the grid; therefore, harsch fault will not affect the grid.

5.3 Cabinet Design

The converter is split into two cabinets as shown in Fig 5.6, the left hand side one encloses lower voltage equipment, such as the H-bridge, the control board and the diode rectifier, while medium voltage devices stand in the other cabinet.A rack. situated rightmost of the medium voltage cabinet, contains the load: it is connected to the NPC and it consists of a series of resistances with a high power rating.

Figure 5.6: The low voltage cabinet stands on the left hand side, with the H-bridge, diode rectifier and control board, while on the right hand side, the transformer, inductance and the NPC are installed.

5.3.1 Low Voltage Cabinet

In the low voltage cabinet, equipment whose voltage does not exceed 600V is installed. Obviously, splitting in two different enviroments equipment whose voltage rating is very diverse, helps the most vulnerable components to reduce any interaction with stronger sources of electromagnetic fields, which may cause disturbances and unwanted behaviour, reducing as well risks of damaging flashovers caused by insulation failure. A three phase connector (which revealed to be defected) connects the passive diode rectifier to the grid. Altough this component is defected, tests have been conducted by temporarely connecting

the system through a three-phase autotransformer, whose output can be manually regulated to enable a slow charging of the DC-link capacitors.

Whenever communication between the Labview's user interface and the DSP, and between the DSP and the FPGA is enstablished, the system is ready to operate. Initially, the FPGA sends an optical switching signal to a transducer, which closes relay K1. Once K1 allows an electrical connection, the DC-link is precharged for 5s; at the end of this interval, K2 closes, disconnecting the precharging resistors. In top left corner is situated

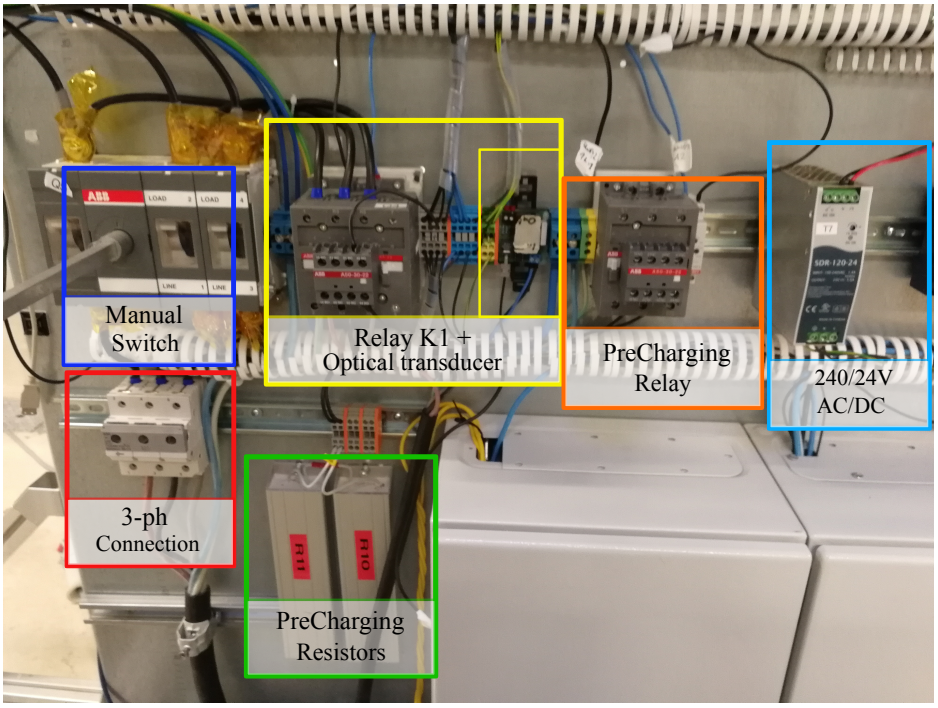

Figure 5.7: Elements installed inside the low voltage cabinet; Unfortunately, both the 3-phase connector and the precharging relay are defected. Tests were done by charging the DC-Link with an autotransformer.

a PC, through which the converter can be operated through LABVIEW's user interface. Fig.5.14 This program exchanges data with the DSP, but none with FPGA; it receives for example measurement signals, which are shown on analog displays. Checksum lightnes up whenever data is exchanged with the DSP; if this is not the case, the DSP will turn into fault mode, causing the FPGA to stop switching. This functionality has been programmed with a *watchdog*, a downcounter which is reset to its initial value whenever communication happens. If data is not received or sent anymore, the downcounter will reach a treshold, 0 in this case, that will generate the mentioned fault. *dcdc* is flicked high whenever the converter is switching, meanwhile *V ref* and *phase shift* are used to set the reference voltage or to apply a determined phase shift.

The DC-link consists of a series of two Siemens B43455-A6568-M capacitors, whose capacitance is 5.6 mF and voltage rating of 500V. The series is connected in parallel to a capacitor included in the H-bridge module, for a total capacitance of 3.3 mF and a voltage rating

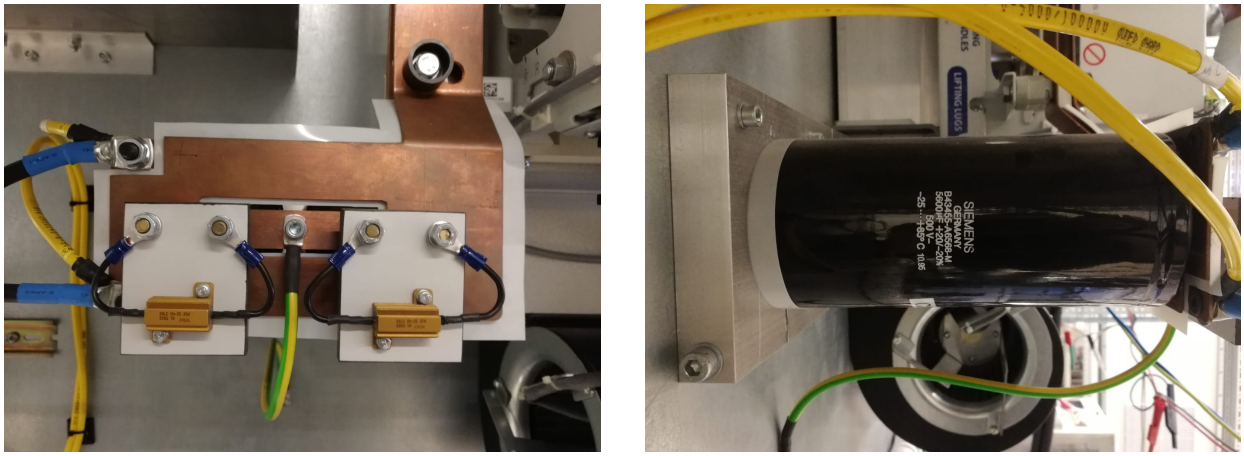

Figure 5.8: The low voltage Dc-link: two Siemens 5.6 mF capacitors are connected in series; each has in parallel a discharging resistor, as shown in left hand picture.

of 1000V. Fig. 5.8. High currents are flowing in the low voltage DC-link, that's why the terminals are connected to the H-bridge with a copper busbar. The H-Bridge is a Semikron Semikube Module, realized with oversized IGBTs with a voltage blocking capability of 1000V and current rating of 172A rms and 450A maximum, therefore the devices give margin of improvement for an higher power transmission. The module is driven through Semikube Board GD11, mounted on its cabinet, that has to receive +24V switching signals and power supply. The module is also equipped with sensors, whose output is a voltage ranging from 0 to 10V. The sampled variables are :

- DC bus Voltage
- H-bridge leg currents
- Case temperature

The switching signals, the power supply and the voltage output should be exchanged through a 17x2 pins flat cable; since the switching pulses are optical and the measurement signals are sent via LAN cables, a PCB, called "Semikron Interface", has been realized to transduce the optical pulses and to obtain measurement signals. The interface realized is rather simple, and is shown in Fig. 5.9.:

The interface PCB has a +24V DC-rail, powered from outside, that is connected in parallel to the drain of several Mosfets. The gate is instead connected to the receiver, therefore, whenever the receiver detects an high optical signal, the Mosfet commutates and the source bus assumes the drain potential. With this method, the switching optical signals sent from the control board to the interface can be transduced to electrical signals that the Semikron board requires. The PCB also has 4 RJ45 LAN cable connectors, employed to send the measurement signals to the control board. The board is also equipped with a transmitter, whose state is high whenever the Semikron control board detects a fail; this optical signal is

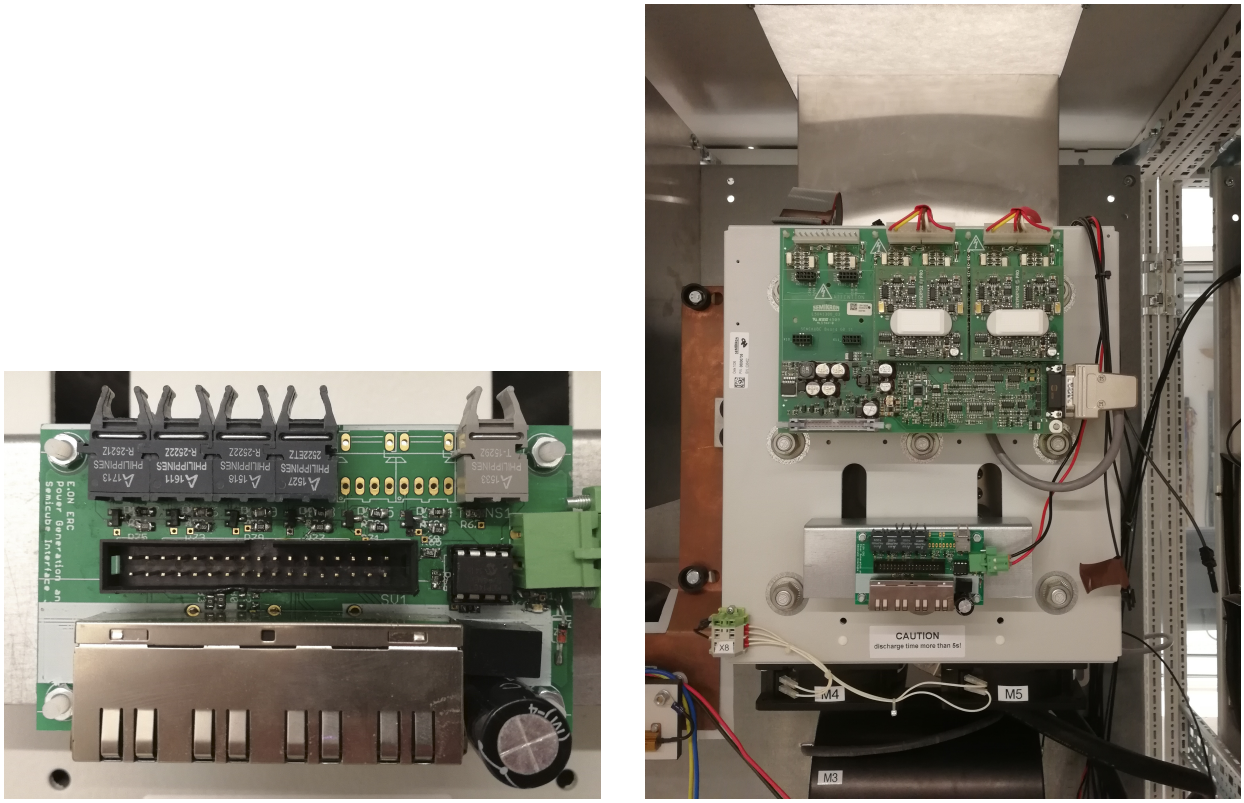

Figure 5.9: The low voltage Dc-link: two Siemens 5.6 mF capacitors are connected in series; each has in parallel a discharging resistor, as shown in left hand picture.

sent to the FPGA which trips a relay(named K1 in the previous subsection), decoupling the converter from the grid.

The control board and the diode rectifier have been both enclosed in cabinets, altough for different reasons: the diode rectified is equipped with many capacitors, and in it is flowing an high current, its failing may lead to explosions that can damage the nearby equipment, specially the control board, that has been closed mainly to shield it against high EMI generated by the switching activity of the IGBTs.

5.3.2 Medium Voltage Cabinet

Inside the right cabinet, medium voltage components are installed, such as the NPC,the transformer and inductance. The NPC has been build formerly at RWTH's Power Generation and Storage System department for HERMES project; by realizing the connection as a busbar, low stray inductance of the NPC is achieved.It is realized with 4 modules of Infineon FZ600R65KF2. Each module contains 3 IGBTs whose blocking capability is 6.5 kV and each can carry 200A, for a total of 600A. Since these devices sustain high currents and voltages, an high delay of 15 μs of the switching-pulses is applied to ensure that enough time

is given to the switches to interrupt the current and go into blocking mode, avoiding any short circuit.

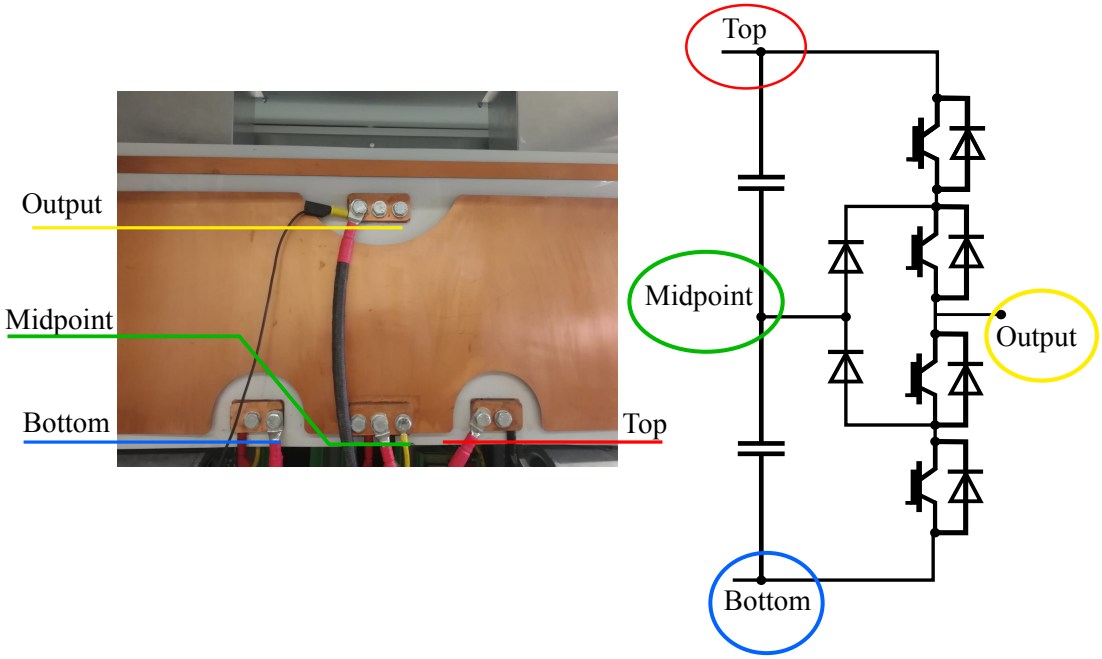

Figure 5.10: The NPC busbar covers the medium voltage DC-link and IGBT module; only the connection buses are visible from front view.

The IGBTs are driven through 4 Concept Gate Driver. Fig 5.11. Since those drivers operate in medium voltage applications, it is required they withstand high electric fields. The employed drivers insulate up to 12kV, and are therefore suitable for this application.The output given is +16V, while +15V is required as input, which is fed by 240/15 AC/DC converters.

The medium voltage DC-link is instead made of 4 medium voltage rating capacitors in total, two in parallel for top DC-link and two for the lower one; Their capacitance and voltage rating are of 120 μF and 3kV. Fig 5.12.

The load consists of four 80Ω steel grid resistors with a high power rating, able to dissipate a consistent amount of heat. With such load the converter is able to transmit up to 75 kW of power, since the resistors have a current rating of 15A DC and can insulate up to 1300V DC. Whenever tests with higher power wants to be performed, the user should shut-down the converter whenever the maximum allowed temperature of the resistors is reached, applying a short-time or an intermittent operation with regular turn-on and consequent cooling turn-off intervals. The operation time can be calculated by the use of a thermal model, that would take into consideration the convection total surface of the grids and their convection coefficient. This limitation has not been take into account since the preliminary and current setup only allows the transmission of up to 40 kW. The resistors are mounted inside a rack. Fig 5.13

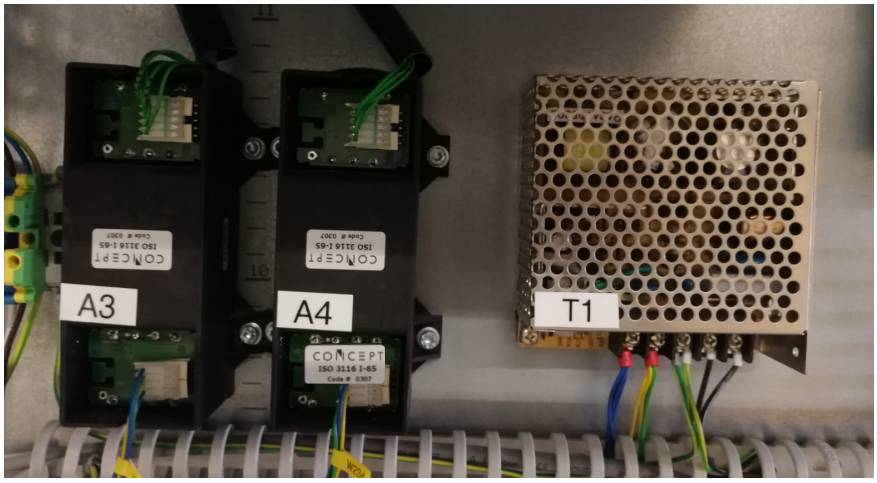

Figure 5.11: The driver module and their power supply are shown in this picture.

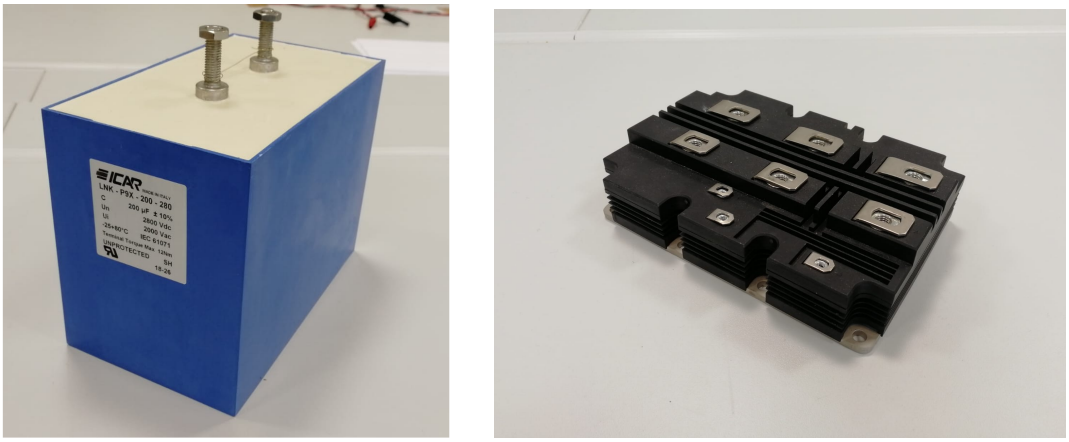

Figure 5.12: On the left, the ICAR capacitors, installed on the medium voltage DC-link, meanwhile on the right, Infineon FZ600R65KF2 IGBT array used to switch the NPC converter.

The transformer and inductance have been recomissioned, like most of this project devices; their cooling capabilities are greatly oversized for this application, therefore it is of interests only that they provide a transforming ratio of 5 and an inductance of 6.2 mH. Fig. shows other components installed in this cabinet: connected via yellow cables with 5-10kV voltage rating, self-discharging resistors whose equivalent resistance is 10kΩ, which are currently mounted but unconnected. . The load consists by now of a series of 320Ω resistors, which allow a much faster discharge of the capacitors. In red, varistors, whose resistivity depends on the voltage applied. If the voltage accross the capacitors exceeds 2800V, reaching a DC-link voltage of 5.6 kV, the varistor's resistivity drops, allowing the capacitor to quickly discharge; due to the high currents, varistors may fail and explode during unexpected operating conditions, therefore, once the full-power setup will be ready, those components will be enclosed in a small cabinet.

Figure 5.13: The load used during tests; four steel grid resistors of 80Ω are connected in series.

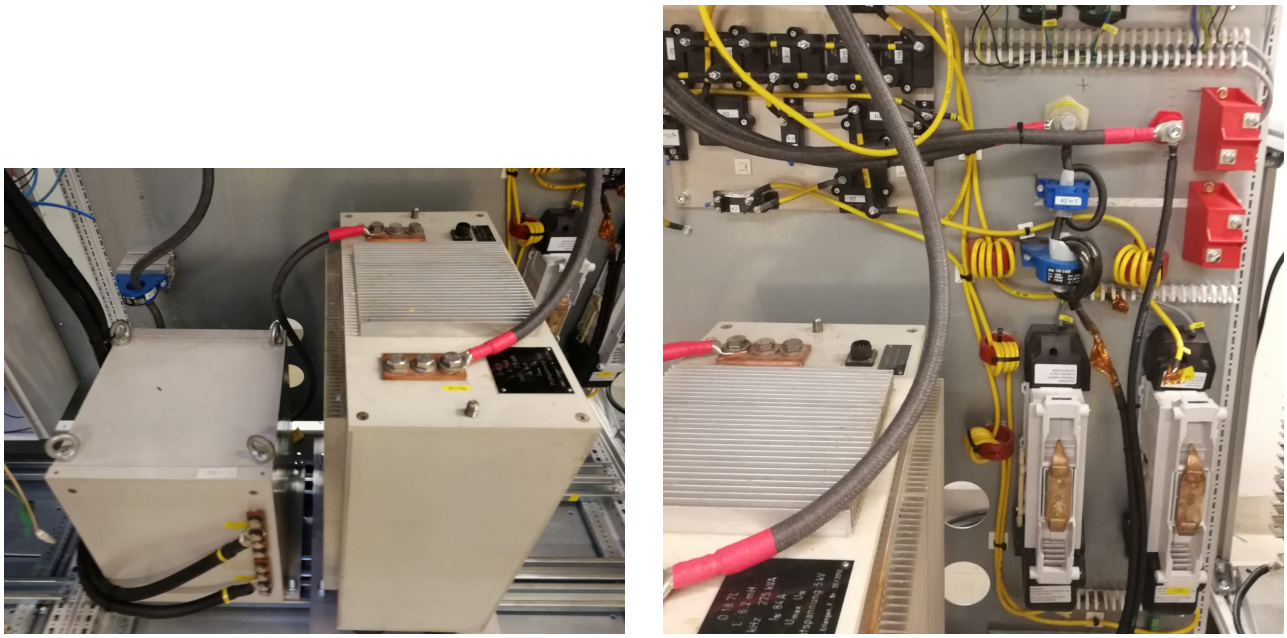

Figure 5.14: In the left picture : the transformer and the inductor; in right picture are visible two red varistors, two DC contactors, black self-discharging resistors connected by yellow cables and in blue two current sensors.

5.4 Measurement Equipment

The measurement equipment rapresent the group of devices that have been used to sample currents, voltages and temperatures of the converter; Those devices have been bought and chosen according to their current and voltage sampling range as well as their insulation rating. The analog signals as output of these devices is then conditioned, which means that

they are transduced as suitable voltage for the ADC, which can accept maximum 3 Volts as input. The digital value obtained is then filtered and rescaled to be read by the user and the DSP. The voltage measurement setup is the following :

- LEM LP-25p hall effect voltage transducer for sampling low DC-link voltage, mounted on the diode rectifier
- Semikron Module voltage sensor as a redundant DC-link voltage measurement.
- 2xLEM LP-25 sp5 for measuring both medium voltage capacitors up to 1.5kV

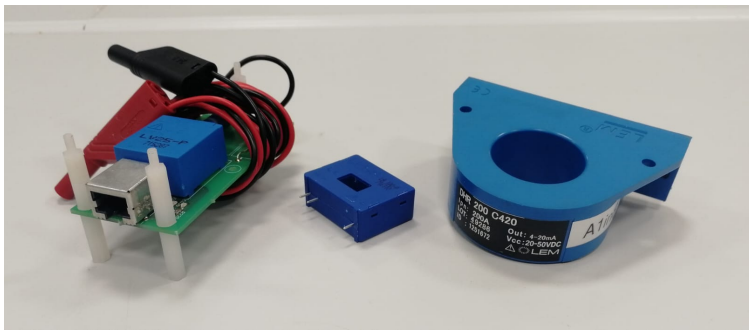

Figure 5.15: lem lv 25, la 100-p and LEM DHR 100 C420, which measure low voltage DC-link and current; the last one measures the load current.

The mentioned LEM voltage transducers work very similarly, altough the one employed on the diode rectifier has a voltage range of 0-500V while the ones used on the medium voltage side can measure up to 1,5kV; this means that the current state of the measurement setup can only allow the converter's medium voltage side to be charged up to 3kV; investments have to be made in order to buy more expensive equipment to increase the voltage working range of the converter. Fig 5.17 shows the measurement circuit. The user has to choose a measuring resistor R_{meas}, which divides the measurand voltage, generating a current flow; the maximum current allowed is 10mA, therefore a resistor of 70kΩ has been chosen and soldered in order to measure up to 700V. Lem voltage transducer acts as a current amplifier whose gain is 2.5, which means that the maximum output current is 25mA. On the right hand side, the signal is amplified and summed to a constant 1.5 V with a differential amplifier, whose output is connected to the ADC. If the relationships $R_1 = R_2$ and$R_3 = R_4$, the output of the differential amplifier is :

$$V_{\text{ADC}} = \frac{R_3}{R_1}(V_{1.5} - V_{\text{out}}) \tag{5.1}$$

The ADC can only convert an analog signal of 0-3V range, which means that V_{out} cannot exceed 1.5 Volts, because it would result in a negative output voltage and consequently, DSP failing. A differential amplifier, generally, is used when an offset wants to be applied to the input signal; in this case, the input signal is shifted of 1.5V. This solution is adopted in order to read negative values, since a zero output voltage would be measured with a an

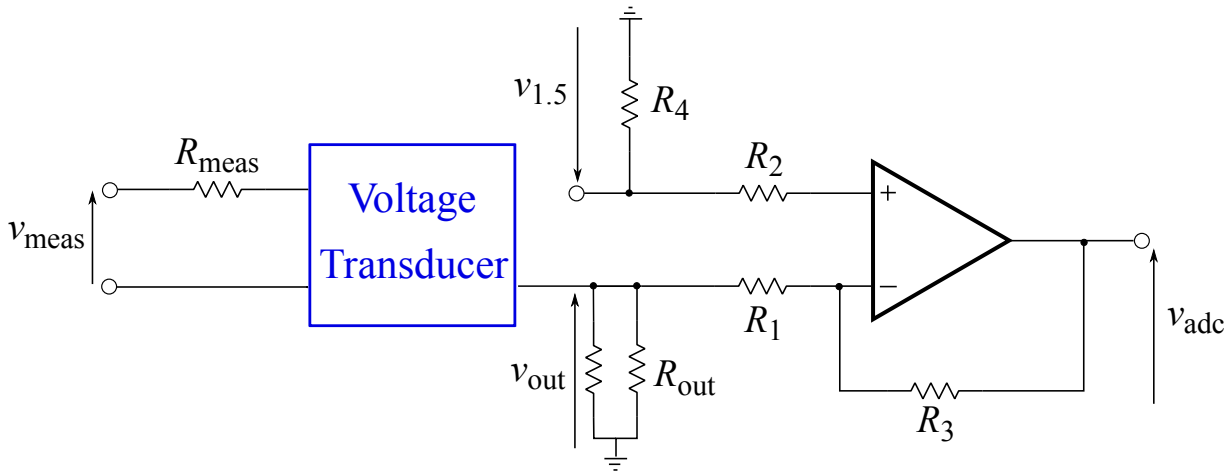

Figure 5.16: The measurement circuit for both DC-links, obtained with lv-25p and lv-25p-sp5. The user has to choose R_{meas} and R_{out} to meet the sensors specifications and increase the accuracy of the measurement. v_{out} is the input of a differential amplifier, whose output is the voltage the ADC will convert into a digital signal.

input of -1.5V. In this application this feature is not required, and only results in having an higher quantization error, since the maximum output range is halved. The reason for this setup lies behind the fact that the control board has been previously used for a different setup and has now been recommissioned. If $V_{out} = 1.5V$ at max, R_{out} has to be chosen equal to $\frac{1.5}{25mA} = 60\Omega$. As for R_1, its value is in the order of magnitude of kOhms, and can be assumed as an open circuit due to its high value. To increase accuracy, two resistances of 120Ω have been connected in parallel to reduce thermal shifting of the measurement.

As for the medium voltage measurement, a PCB has been designed, and it is shown in Fig 5.19. The size of the PCB is quite large and realized in a U shape; the higher terminals are connected to the 1.5 kV NPC buses, while the central one is the grounded mid-point of the NPC. Many resistors are connected in series to both terminals to have maximum 10 mA as LEM input, while the parallel one ensure a reduced thermal stress on each resistor, that have been chosen to dissipate around 4W. The size and shape of PCB are motivated by the fact that large distances between medium voltage and ground are needed, otherwise unwanted flashovers may happen. The U shape achieves high distance between the grounded mid-point of the NPC, as well as high distance between the upper voltage terminal and the lower part of the PCB, in which the RJ45 Lan connector are mounted.

Figure 5.17: The close cabinet: three analog sensors are mounted, a desktop through which the DSP can be debugged and Labview user interface executed.

The current measurement setup consists instead of:

- LEM lA 100-p mounted on the diode rectifier to measure its output current
- Semikron Module current sensor for both H-bridge currents
- LEM DHR 100 C420 for sampling the load current

LEM 100-p working principle is rather simple: it attenuates the signal by 2000, sending as an output maximum 5mA. LEM DHR 100 C420 is characterized by an offset of 4mA for zero measured current and a linear output until the measurand value hits 100A, which corresponds to 20mA as output. The only parameter that has been taken into account is the upper limit: In fact, the offset introduced by the sensor is compensated by the DSP, which reads the ADC values during a short start-up of the converter and eliminates the offset introduced by the differential amplifier:

$$V_{\mathrm{ADC}}(t) = V_{\mathrm{ADC}}(t) - V_{\mathrm{offset}} \tag{5.2}$$

As for the Semikron Module measurements, togheter with the two H-bridge currents and the DC-link voltage measurements, the case temperature of the module is sampled. All signals

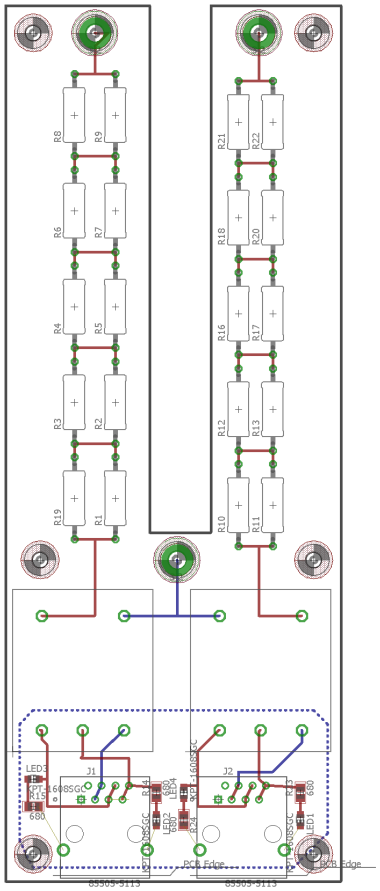

Figure 5.18: The PCB has a U shape to ensure that high distance between two 1.5kV buses and the midpoint. A large number of resistors are employed to have 10mA without exceeding their thermal capabilities. The blue devices are the LEM lv-25-p,sp5 hall effect voltage transducers, whose output is sent via LAN cables.

have range 0-10V, which means that connecting directly the Semikron Module to the ADC would cause the DSP to fail due to overvoltage. To overcome this solution, the resistors of the differential amplifier of those four channels have been adjusted, in order to meet the already discussed requirements. If $R_1 \neq R_2$ and$R_3 \neq R_4$, the differential amplifier output is the following :

$$V_{\text{ADC}} = V_{1.5}(\frac{R_4}{R_4 + R_2})(\frac{R_1 + R_3}{R_1+}) - V_{\text{Semikron}}(\frac{R_3}{R_1}) \tag{5.3}$$

Choosing for example $R_2 = R_4 = 330\Omega$ satisfies the condition $0 < V_{\text{ADC}}(t) < 3V$.

The converter is equipped as well with two analog measurement, respectively of low and the two medium voltage capacitors. The user can read the analog signals on the front panel of the converter, as shown in Fig.5.20. The full-scale value is shown by the needle whenever

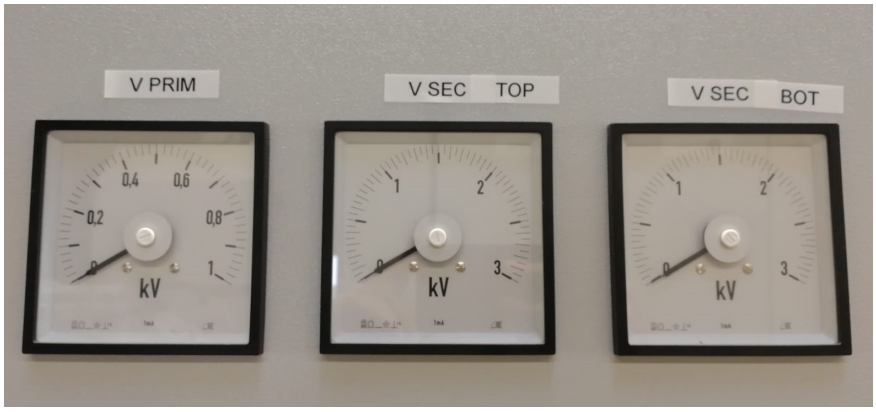

Figure 5.19: The analog meters. On the first it is possible to read the low DC-link voltage, on the other ones the two voltages on the NPC side.

the device receives 1mA, which means that 500kΩ resistors and 2.5MΩ connect the sources to the analog reader.

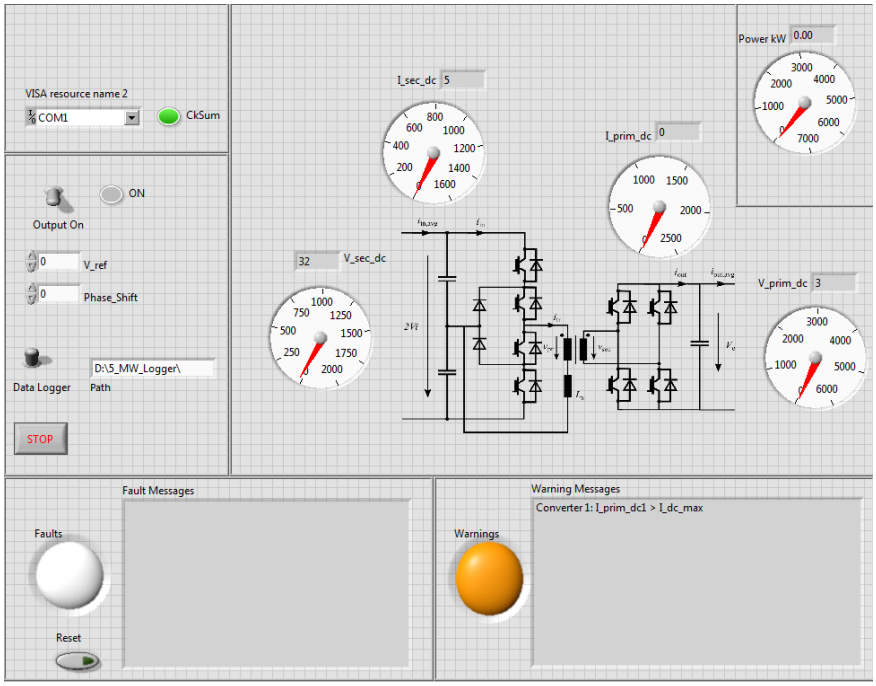

Figure 5.20: Through this Labview program, the user is able to run the converter, set reference values and read the measurement signals. If an error occurs, *svm enable* will be set automatically to zero, and a message will communicate what error has occurred.

5.5 Summary

This large section is rich in details regarding the components employed. Most of them are recomissioned, therefore economicity has been achieved. The input voltage is obtained through a passive converter, that rectifies the 380 AC into 530 DC voltage. The H-Bridge is a Semikron Semicube, with maximum voltage rating of 1kV and 132A RMS current. The transformer has transformation ratio of 5 and the inductor has a value of 6.2 mH of inductance. The NPC is instead built with 4 oversized IGBT array, each with a blocking capability of 6.5 kV and current rating of 660A. The components lie in two different cabinets, of which the leftmost one contains low voltage components, including the PC, the control board, the pre-charging circuit and relays; medium voltage components are instead situated in the other cabinet. Most tests have been conducted using resistors in series fashion, for a total value of resistance of 320Ω. Both DC-Link voltages are measured, as well as input and output currents of the converter; the voltages are also measured analogically, and the signal is displayed through meters on the front panels.

6 Experimental Results

6.1 Setup Limitations for Full-Scale Testing

The setup used for the experimental results did not allow full-scale power tests of the converter, in fact:

- Lacking of precise current measurements made possible only the implementation of a voltage controller.
- The relay employed for pre-charging of the low voltage DC-link was defected and had to be shipped to the supplier;not enough time was given to invest in a new one.
- When the output voltage reaches around 1600V, strong EMI disturb the control-board power supply and the USB cable which connects the DSP to the computer, causing a failure in either the SPI communication or Labview interface.
- The cable which currently connects the passive rectifier to the DC-link has insufficient current capability (35A).
- Lacking of voltage measurement up to 5kV (Altough it can be realized trading precision)

The current sensor employed to measure the load current needs a voltage supply ranging from +20 to +50 V. As already mentioned, though, each sensor is powered through a LAN cable connected to the control board, which is able to provide maximum +15V. Altough it has been ensured that the device can work with +15V, it has been later discovered that it suffers from low precision, powered with such insufficient voltage. A voltage booster PCB has been ordered to overcome the issue.

When relay K2 (the one used for the pre-charging of low voltage DC-link) was first tested, it has been discovered to be defected. It was later shipped to the supplier, which not yet repaired it. Lacking of a pre-charging circuit, it is impossible to connect directly the passive rectifier to the three phase grid: high inrush currents would flow and damage the equipment. The solution that has been found is to connect the converter through an autotransformer, whose output can be manually regulated. By tuning manually the transformation ratio, is it possible to increase steadily the output voltage, in order to avoid dangerous high currents. Tests up to 200V on the primary side have been executed, since the transformer is connected to the rectifier through laboratory cables, that can handle relatively small currents.

The computer installed in the converter cabinet is not provided with electromagnetic shields: if the current switched by the IGBTs is relevant , it may suffer from high EMI. So does the USB cables that connect the Xilinx programmer to the computer (which has been

Figure 6.1: The autotransformer, thanks to its ability to manually tune the output voltage, tests were conducted despite the defected relay and three-phase connector.

removed because it caused many times failing of the FPGA) and the one which allows the real time debug of the DSP on Code Composer Studio, a programming and debugging software enviroment for TI C2000 series processors. New shielded cables have been ordered, meanwhile not yet the computer has shown to heavily suffer from EMI. On the contrary, when testing up to 900 V, the DC/DC 380/24 V power supply that powers the control board has shown many times to be affected by electromagnetic emissions. Its output was, in fact, oscillating, causing insufficient power suppletion to the control board; many times the SPI communication between the DSP and the FPGA failed due to undervoltages, causing the shutting down of the converter. To overcome this problem, a new, shielded DC/DC converter has been ordered, meanwhile temporarily a 1000uF electrolitic capacitor has been soldered directly on the connector, to keep the voltage steady altough the heavy flickering of the DC/DC output.

The cables that currently connect the diode rectifier to the DC-link can only tolerate around 35A, which rapresent a really low current value given the converter capabilities. During testing, the fault code has been programmed to disable the switching whenever this value is exceeded. New cables have to be produced which allow an heightened current flow.

Voltage measurement up to 5kV is missing: LEM lv 25/sp5 hall-effect voltage transducer can measure up to 1,5kV, and since two are employed, the setup can work up to 3kV. As already mentioned, a resistor has be to chosen so that the full-scale measurand voltage creates 10mA that flow into the device. If more resistors are employed to measure 2.5kV instead, the device can still operate, since the voltage drops across the series of resistor, while the voltage across the device is almost zero; also, considering the high distance between the 2.5kV buses and

the device, it can be assumed that the sensor insulation will not fail. This solution trades off an higher precision for a wider operational range; the bandwidth of the device has also to be assumed lower than the expected, since the input resistance is increased.

Another issue that has been encountered during testing, is that if the reference output voltage is greater than the maximum voltage the converter can apply as an output, the PI will integrate the voltage error over time, causing a huge delay in the response when a new reference is set; the system has everytime to be restarted, so that the values can be reset. In future works, the DSP can be programmed with a function that returns an error whenever this happens. A value has to be defined, which is the input and output voltage ratio:

$$d = \frac{V_{\mathrm{i}}}{V'_{\mathrm{o}}} \tag{6.1}$$

This value, which depends on the phase-shift, is of course greater than 1 if the converter is working as a Boost, lower instead if it's employed as a Buck converter; its maximum value can be easily calculated, known the power transmitted by the converter to the load. In this case, since the load is a series of resistances, $d_{\max}$ can be calculated as follow:

$$P_{\mathrm{load}} = \frac{(2 \cdot V_{\mathrm{i}})^2}{R_{\mathrm{load}}} \tag{6.2}$$

$d_{\max}$ is obtained when the maximum power is transmitted, and it has been demonstrated in chapter 1 to be equal to:

$$P_{\max} = \frac{V_{\mathrm{i}} \cdot V'_{\mathrm{o}} \cdot \beta}{2fL_{\mathrm{s}}}(1 - \beta) \tag{6.3}$$

The input and output voltage ratio can be obtained from the system of equations :

$$d_{\max} = R_{\mathrm{load}} \cdot \frac{\beta}{8fL_{\mathrm{s}}}(1 - \beta) \tag{6.4}$$

This ratio then depends obviously on the phase shift, on β, and also on the load resistance. If $R_{\mathrm{load}} = 320\Omega$ and $\beta = 0.375$:

$$d_{\max} = 1.512 \tag{6.5}$$

Such result show that with such load, for a maximum power transfer, the converter acts as a Boost converter.

Figure 6.2: The testing station: Labview's interface and DSP debug enviroment running during tests, meanwhile all voltages and currents are measured and read on the oscilloscope.

6.2 Experimental Results

Several tests have been done to achieve the highest secondary voltage possible and evaluate the performances of the converter; altough the full-power setup will work as a Buck converter transmitting around 50kW power, preliminary tests see the converter as a Boost topology instead. Lower voltage tests, below 200V, have been conducted to check the efficiency of safety routines,the correct execution of the program embedded on the FPGA and DSP, and the correct functioning of Labview's user interface. Fig.6.3. shows one of the earliest tests; the low voltage DC-link is charged with 65V, while the phase shift is set to maximum power transfer to achieve the highest primary voltage, which means that $2V_{\mathrm{i}} = d_{\max} \cdot V_{\mathrm{o}} \cdot 5 = 500V$. The results show that the formulation of $d_{\max}$ is correct, and will be later implemented to achieve a safe operation of the converter. The voltage vaweforms appear to be clean, without voltage spikes during switching or any abrubt oscillations caused by stray resonant elements. The phase shift is around 110° as expected, causing the H-bridge to lead the NPC output. The currect waveform, sampled on the secondary side (H-bridge side), appear to be affected instead during each switching instant, but does not suffer between two switching instants.

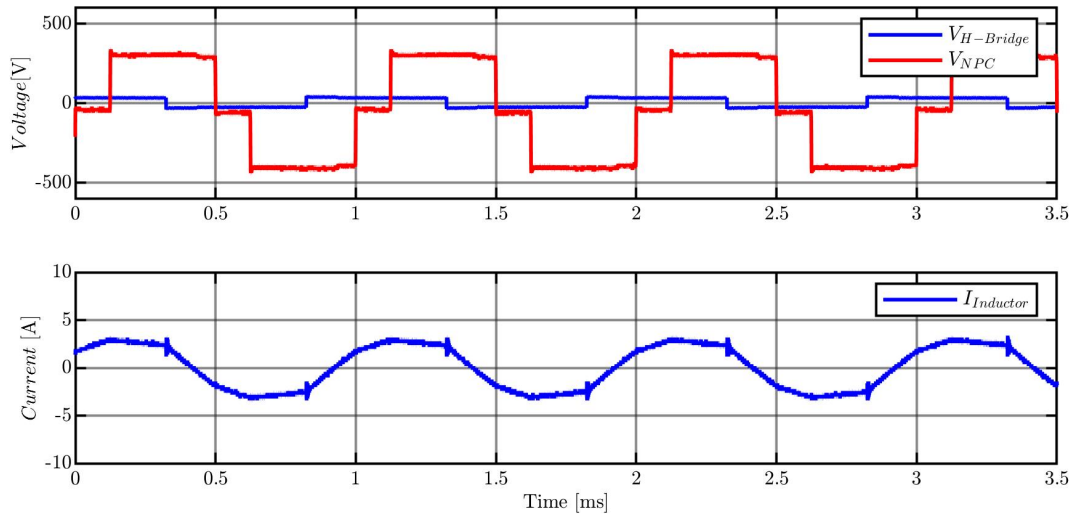

Figure 6.3: Test up to 500V

Further tests have pushed the converter to 1kV, and 2kV. The results are show in Fig.6.4,6.5.

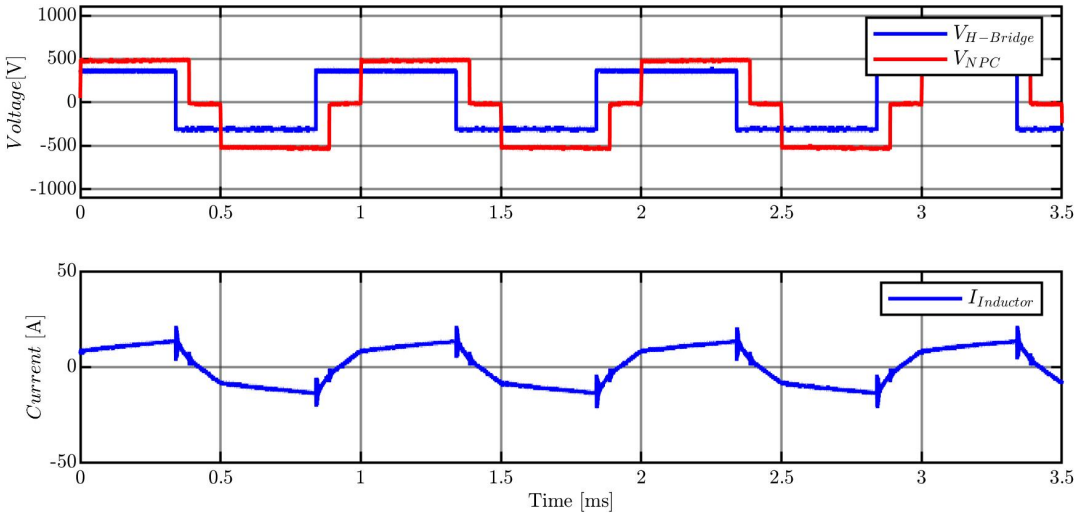

Figure 6.4: The first test in which the converter has worked in the medium voltage range: 1kV on the output side has been achieved.

Fig 6.4. shows a test conducted with 1kV : the converter worked for the first time as a medium voltage converter. The input voltage is around 400V, causing the the medium voltage DC-link to charge up to 1kV with a relatively low phase shift. The converter was able to transmit 3kW. Fig 6.5. shows instead the last test, in which the primary side is charged up to 2kV, while the secondary side at around 400V. The power transmitted is around 13 kW, which corresponds to the maximum allowable for this setup, since the low voltage DC-link cables have low current capability.

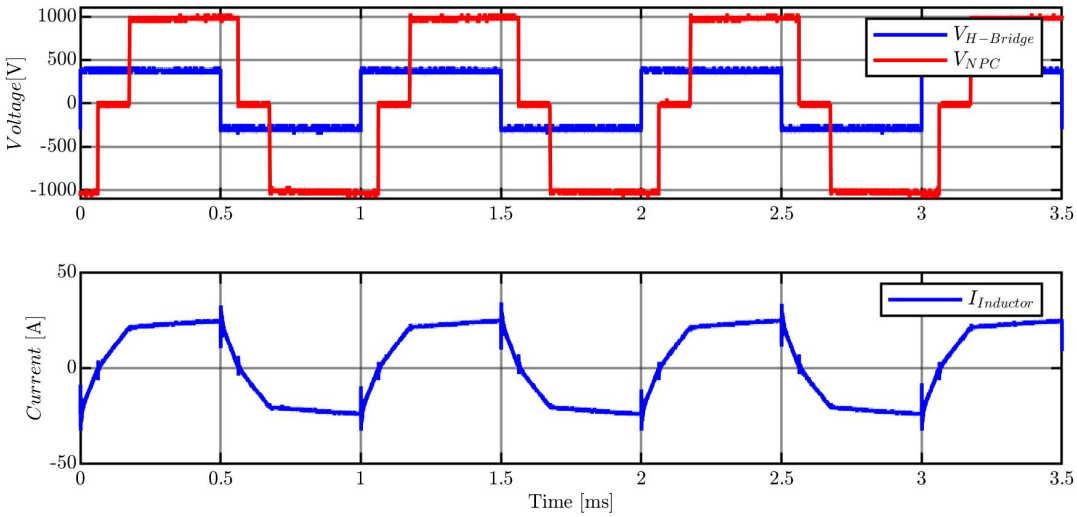

Figure 6.5: Tests conducted at 2kV on the high-voltage side and around 350V as input.

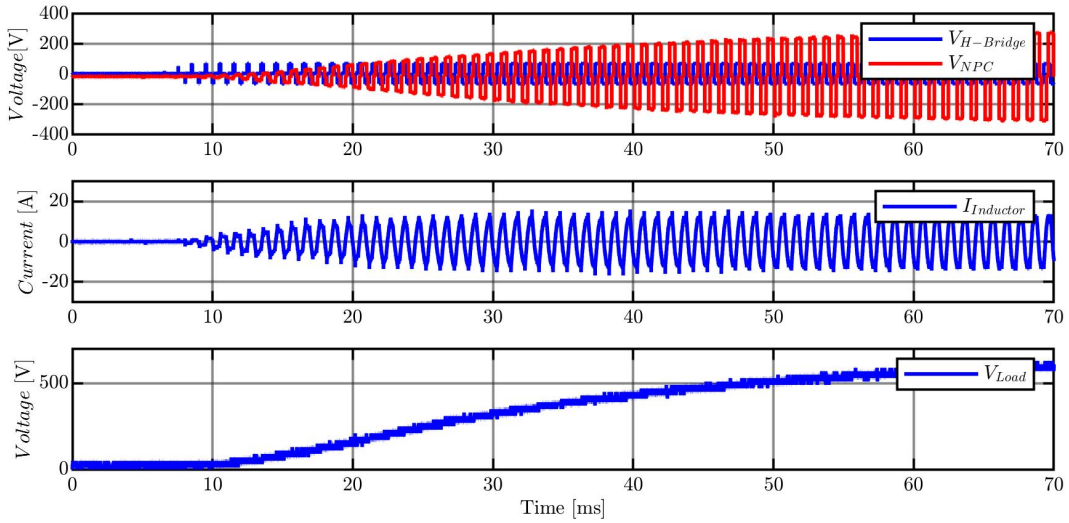

Figure 6.6: The figure illustrates the voltage response to a step of voltage reference; the response is stable. It is possible to notice the precharging strategy adopted during the initial 200ms.

Fig.6.6. shows the step response to a reference voltage step of 650V. The green waveform in the first plot rapresents the H-bridge output voltage; it can be observed the pre-charging strategy, that has been set to be really fast. After this interval, the H-bridge works with 50% duty cycle. The precharging strategy is effective, since the currents are limited and no oscillation happens. Unfortunately, with such fast precharging time, higher steps of reference voltage have shown to lead to saturation of the transformer. The precharging time has to be increased or either a reference voltage has to be fed to the control as a ramp, to avoid over stressing of the transformer. The results show a good response of the PI voltage control,

without any oscillation and with a steady state error equal to zero.

6.3 Summary

This section has brought details about the limitations of the current setup, which allowed tests at lower than the converter's potential. Lacking of thicker cables, shielded equipment against EMI and properly functioning equipment have made impossible the testing of the precharging of the low voltage DC-link capacitors and testing at higher voltages on the H-bridge side (regardlessly of the secondary output). As a temporary solution, an autotransformer has been employed to charge steadily the low voltage DC-link manually, while the limitations caused by EMI and rather thin cables have not been defeated. The results are still satisfactory : the medium voltage capacitors have been charged to 1kV each, for a maximum load voltage of 2kV. An active power of 13kW was transmitted without the converter to suffer from any unwanted behaviour; the vaweforms are clear, without oscillations or spikes, meaning that the design has achieved low stray inductances and capacitances that could have disturbed the vaweforms. As for the voltage PI controller, its response is rather fast and steady-state error free. Unfortunately, the precharging time has to be increased in order not to saturate the transformer during the converter transitory, which will cause a slower dynamic.

7 Conclusions

This work, surely ambitious given the time avaible for its achievement, has been carried out starting from unused components, with the aim to realize a medium voltage DC/DC converter, whose future application will be to feed power to experimental devices under test with a power requirement in the kW range. The work started from simulations and analytical investigations of the topology, in order to gain familiarity with its working principle, and then continued to the design and implementation of its control; the final, most challenging step, has been to physically assemble the converter and test its functionality. The FPGA executes with efficiency all the programmed tasks: generation of switching pulses, application of a delay to rising edges, DSP communication with the FPGA. The DSP has been embedded with a fault code and a PI controller, and it has been tested able to stop and protect the converter during faults. The control implemented has shown instead to be able to reach the reference voltage without overshooting, achieving a steady state error equal to zero. The converter was physically built and run, achieving tests to up to 2kV on the medium voltage side and 400V as low voltage input, realizing a DC/DC conversion at 1kHz of 13kW of transmitted power. The converter can be improved in many ways, such as:

- Improved cabling, able to lead more power.
- More efficient shielding, that prevents failures due to EMI.
- Lower self-discharging time of the medium-voltage capacitors.
- Introduction of an LED, or an alarm, that warns the user of the uncompleted self-discharge of both DC-Links.
- Implementation and simulation of a control loop that takes into account delays and non-idealities.
- More expensive passive protections that allow more power flowing.

Regardlessly, the results obtained can be considered a full success.

List of Figures

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