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Department of Electronics and Telecommunications
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Thesis

Design of an integrated DC-DC boost converter for portable biomedical devices

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Abstract

In the near past technology progress enabled electronic circuits to become smaller and denser. Moreover, scaling down of *Integrated Circuits* (ICs) fabrication processes allowed for the reduction of the supply voltage and techniques for diminishing power consumption were developed. As a consequence the use of battery-powered portable devices has grown rapidly and power electronics had to expand its coverage to permit their realization. Compact, cheap and efficient monolithycally integrated converters are of paramount importance for portability and performances need to be improved continuously, with growing challenges and problems.

Smartphones, laptops, remote sensors and controllers are just few examples of applications made possible by integration and technology progress. However, also new possibilities for enhancing directly people's life opened. One of the most interesting, attractive and fascinating is the development of biomedical implantable devices: they permit to monitor health constantly and to be a help for people's handicaps or even a substitute for physical lacks, such as limbs amputations.

The objective of this thesis is to design a power converter able to supply a portable neural stimulator, whose aim is to tackle obesity by providing patient's appetite control. It has been carried out in its entirely at the *Centre for Bio-Inspired Technology, Imperial College London, (UK)*, within the *i2MOVE* research group. The main challenge is the contemporaneous fulfillment of system reliability, high power conversion efficiency and compactness of the device.

Overall, the whole project is based on a *top-down* approach, including all the design steps of a real IC, with the exception of the layout generation. A preliminary analysis involves a quick literature review, the choice of the correct topology, based on technical specifications, and the high-level block scheme definition of the system. Then a complete description of each block is provided with a *Hardware Description Language* (HDL), specifically Verilog-AMS. Afterwards, simulations are carried out to verify the correct behavior of the entire system. Finally, each HDL block is translated into an equivalent transistor-level schematic and everything is simulated again to confirm proper functionality.

The software used for the design is *Cadence Virtuoso*©, although *MATLAB*© is exploited as well in the preliminary phase.

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Contents

Introduction **1**
Background and motivation: i2MOVE project 1
Methodology and report outline 4

1 Preliminary analysis and design **5**
1.1 Converter topology 6
1.2 Power stage 10
1.2.1 Non-integrated components selection 17
1.3 Transfer function and compensation network 19
1.4 Start-up phase 23
1.5 Critical events 25
1.5.1 Output over-voltage protection 25
1.5.2 Over-current limiting 27
1.5.3 Output short-circuit protection 28

2 Verilog-A model based design **30**
2.1 Control loop 30
2.1.1 Operational amplifier 31
2.1.2 Set-reset flip-flop 34
2.1.3 Comparators 35
2.1.4 Current sensor 36
2.1.5 Gate driver 36
2.2 System simulations 37

3 Transistor-level design **41**
3.1 Current sensor 41
3.2 Compensator 52
3.3 Comparator with hysteresis 62
3.4 Gate driver 65
3.5 Soft-start 66
3.6 Synchronous converter 74

3.6.1 Voltage reference regulation 76
3.6.2 Gate driver 79
3.6.3 Zero Current Detection 79
3.6.4 Logic control 84
3.7 Asynchronous vs synchronous design 87

4 Conclusions **90**

Appendix A Code **92**
A.1 MATLAB 92
A.2 Verilog-A modules 95

Bibliography **101**

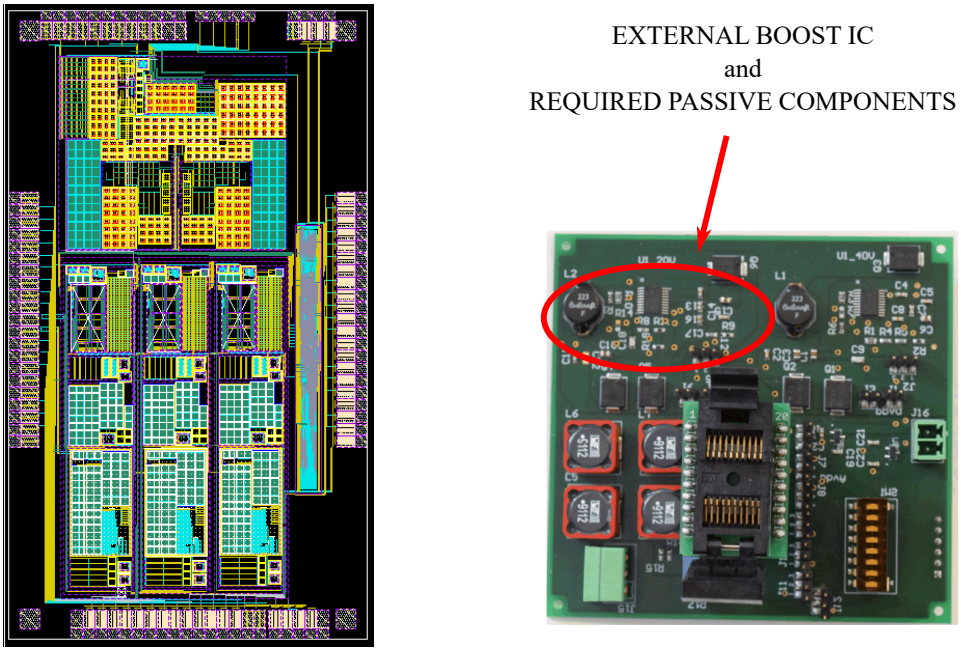
Introduction

Background and motivation: i2MOVE project

The work object of this thesis is part of a wider research project, funded by the *European Research Council* (ERC) and conducted by a cross-disciplinary research team at *Imperial College London, Centre for Bio-Inspired Technology, UK* (CBIT). i2MOVE is the acronym of "Intelligent Implantable MOdulator of Vagus nervE function for treatment of obesity" and the aim is to develop next generation neural interfaces to tackle obesity and nutritional disorders. Specifically, this can be achieved by electrically stimulating the gastric branch of the vagus nerve during meals, so that patients feel a sense of satiety even if they have eaten just small amount of food.

The novelty of the project is explained by the word "intelligent": the goal is in fact to design a closed-loop system which decides autonomously *when* and *how much* to stimulate, leading to a more accurate and effective treatment. Open-loop solutions are already available on the market [1], but they require manual settings adjustments and the optimum stimulation pattern is hard to find. Indeed tissue impedance, pH concentrations, adherence of implants on the nerve and many other characteristics are never identical in different patients and even in the same subject they could vary a lot in a short time, because they depend on a multitude of complex and unpredictable factors. The standard *Vagus Nerve Stimulation* (VNS) requires therefore a kind of human manual trial and error approach to find an effective therapy, limiting the capabilities of the treatment.

The project started in 2014 and so far few chips have been produced and tested. Moreover, a platform has been successfully developed for experiments on rats, showing yet proper functionality. A live demo [2] has been demonstrated in Turin, Italy, in 2017 during the annual *IEEE Biomedical Circuits and Systems* (BioCAS) *Conference* and the design of a complete *System-on-Chip* (SoC) solution has been finished in September 2018 and will be soon fabricated and tested. Figure 1a shows the layout of the full SoC, developed on a *Taiwan Semiconductor Manufacturing Company*© (TSMC) 0.18μm *Bipolar-CMOS-DMOS* (BCD) *6-Metal layers* (6M) *High-Voltage* (HV) process.



(a) (b)

Figure 1: (a) Layout of the last SoC. (b) Stimulator test board.

An architecture overview of the platform for tests on rats is shown in Figure 2. The whole plant can be differentiated into three subsystems, namely *signal acquisition and pre-processing*, *decision making algorithm* and *stimulation*. Two types of signal are acquired to decide *when* and *how much* to stimulate: an electrical, i.e. *Compound Action Potential* (CAP), and a chemical one (pH and K concentration). Chemical signals are converted into electrical ones with potentiometric sensors, obtained by implanting IrOx and AgCl hook electrodes directly in the nerve. They are subsequently boosted and pre-processed using analog front-end amplifiers, to increase the *Signal-to-Noise Ratio* (SNR). A machine learning algorithm is then responsible to control the neural stimulator, relying on the information collected from the acquired signals. The nerve is first classified by applying mock stimuli and recording the response, then an iterative loop finds the best stimulation pattern based on the actual nerve response and a set of parameters. The algorithm has been first developed in a software environment, but an hardware equivalent version has been designed to be integrated in the final SoC. The stimulation current is obtained with an HV H-bridge, wired connected to the nerve. Bi-phasic zero-average currents are required in order to avoid tissue damages, so a negative feedback circuitry has been added to ensure that. The amplitude, frequency and width of the pulses, which are set by the algorithm, are regulated with a 6-

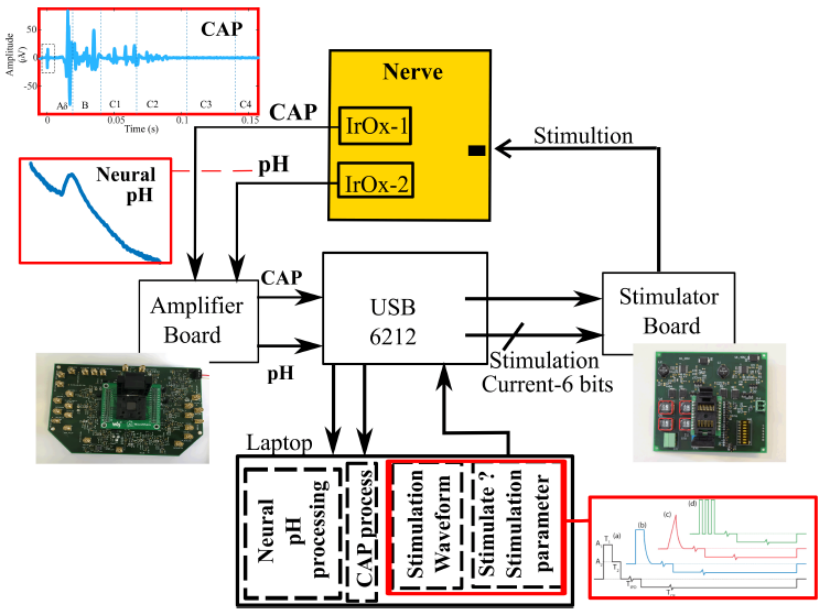


Figure 2: Platform already tested on rats

bit *Digital-to-Analog Converter* (DAC), which drives the H-bridge. More details about VNS and the system architecture are available in [3][4][5].

The objective of this thesis work is to design the step-up converter required to supply the HV neural stimulator. The typical 3V or 3.6V of coin batteries are indeed insufficient, thus a DC-DC conversion is necessary. An integrated solution in the SoC is very attractive because offers several advantages with respect to an external discrete component approach (shown in Figure 1b), adopted for the development platform previously described. A lot of area on the *Printed Circuit Board* (PCB), thus cost, can be saved and the size and weight of the whole product are reduced, with benefits for implantability. Moreover, the design is targeted to this specific application, so electrical requirements can be fitted better and performances improved.

This work covers therefore all the steps required to the realization of an integrated boost converter, following a *top-down* approach: from high-level specifications to transistor-level schematics, the layout only has not been done.

Methodology and report outline

The report structure reflects the methodology adopted for this work, which is comprehensive of literature review, paper-and-pencil calculations and *Computer Aided Design* (CAD) simulations. It is organized as follows:

- In *Chapter 1* an explanation of the high-level system specifications is first detailed. Then a quick literature review referencing similar state-of-the-art converters is presented and the choice of the topology, including the control scheme, is motivated. Afterwards, the whole design of the characteristic parameters is developed. Non-integrated components are then selected and the dynamic behavior of the power stage is investigated. Finally techniques for critical events, namely soft-start, short-circuit handling, over-current and over-voltage protection, are illustrated.

- *Chapter 2* begins with a short introduction of Verilog-AMS HDL and follows with a detailed description of every module which has built. It ends with several simulation graphs demonstrating proper functionality of the whole system and confirming that the preliminary analysis is correct. Particular attention is given to stability. The design of an asynchronous converter is reported only and is taken as reference for the next part of the thesis, where also a synchronous version is developed.

- *Chapter 3* is the heart of this work: transistor-level schematics of each block are presented with detailed explanations regarding choices, topologies and design procedures. Most of them are referenced to existing devices and papers, which is good for reliability, but some original solutions are proposed as well. Simulations and verifications, also referred to the Verilog-A based project, are carried out throughout the whole chapter. Both the asynchronous and synchronous converters are fully designed and a comparison of the two is reported, showing pros and cons. The synchronous solution is chosen as the best at the end.

- Finally, in *Chapter 4* conclusions are drawn with a brief summary of all the project's characteristics and the fulfillment of requirements is demonstrated. A possible future work to improve some performances, however, is suggested.

Chapter 1

Preliminary analysis and design

As mentioned in the Introduction, the converter to be designed has to provide a stable voltage to supply the H-bridge of the neural stimulator. The required voltage can be derived by knowing the tissue impedance and the necessary current to stimulate the nerve. Referring to experiments held on rats [5], the nominal impedance of the tissue is 10 kΩ while the minimum current needed to excite C-type fibers of the nerve is 3.2 mA, resulting in a minimum voltage of 32 V. However, human tissue impedance is expected to be lower and also the current still is not known precisely, hence a more versatile device should be built. For these reasons the DAC driving the H-bridge has been designed with an output current in the range 1 mA ÷ 20 mA, with a *Least Significant Bit* (LSB) of 50 µA, and the H-bridge supplied with 20 V. Probably a 40 V would provide a larger spectrum of capabilities for the device, but at the same time would require a much more complex design electronically speaking, thus 20 V has been considered a good trade-off. Time parameters of the bi-phasic injected current are important as well for the effectiveness of the stimulation and are listed in the following:

- number of meals per day: 3 to 10;
- pulse width: 0.2 ms to 2 ms;
- frequency of pulses: 2 Hz to 20 Hz;
- duration of the stimulation: 10 s to 120 s.

They are useful also to determine the battery lifetime, once the overall efficiency has been computed. In order to guarantee a sufficient lifetime an average efficiency η greater than 80% has been taken as a system constraint to make possible the use of small coin batteries. Finally, the peak-to-peak voltage ripple at the output should be less than 100 mV to reduce supply noise across the stimulator and

the input voltage has to be in the range $3\,\mathrm{V} \div 3.6\,\mathrm{V}$, allowing the use of both rechargeable and non-rechargeable standard batteries.

All high-level specifications are listed in Table 1.1. They are kept as a reference along the whole design process.

PARAMETER	VALUE
V_{in}	$3\,\mathrm{V} \div 3.6\,\mathrm{V}$
V_{out}	$20\,\mathrm{V}$
I_{out}	$1\,\mathrm{mA} \div 20\,\mathrm{mA}$
R_{out}^{eq}	$1\,\mathrm{k\Omega} \div 20\,\mathrm{k\Omega}$
ΔV_{out}	$<100\,\mathrm{mV}$
η_{avg}	$>80\%$

Table 1.1: Converter high-level specifications.

1.1 Converter topology

The first step in the design was the right choice of the topology. Indeed several solutions to step-up a voltage exist in literature [6]. The particular aspect of this work is the rather high conversion ratio, namely $(V_{out}/V_{in})_{max} = 6.66$, which is quite challenging to achieve with a single stage. The converters which have been investigated are listed in this section.

- Regulated charge pump. It is the best solution in terms of cost, area and power density, because everything could be integrated [7]. Nevertheless, it produces a noisy output voltage ripple with the typical sharp sawtooth shape and with high conversion ratios a lot of components are required. Moreover, if regulated and especially over wide ranges of input voltage and load current, it shows poor efficiency [8], unless complex multi-gain or multi-mode pumps are designed [9]. However, an efficiency which is comparable to inductive type converters is hard if not impossible to achieve.

- Boost converter. It is an inductive type basic converter, yet showing good characteristics in terms of efficiency and power densities. The output voltage can be regulated smoothly over wide ranges of both input voltage and load current and transient response could be very fast. It can work both in *Continuous Conduction Mode* (CCM) and *Discontinuous Conduction Mode* (DCM), but the latter is usually preferred because of stability issues due to the presence of a *Right Half-Plane Zero* (RHPZ) in the output-to-control

transfer function in CCM [10][11], even if efficiency is higher in CCM. Moreover, since the output current is low, it is tough to let the converter operate in CCM over the whole load range. Finally stresses on components are not heavy, so it is a good candidate for the purpose of this work. The challenging point is the rather high conversion gain, which possibly leads to high losses or instability. But with a good design they can be avoided. It comes either in an asynchronous fashion, if the secondary switch is a diode, or in a synchronous one, if it is an active switch: the latter demonstrates better efficiency, but the control is more complex.

- Buck-boost converter. It shows characteristics which are similar to the boost converter ones, but usually with lower efficiency. Moreover, it is more difficult to drive because the main switch is in high-side configuration, while in boost converters it is on the low-side.

- Flyback converter. Figures of merit are the same of boost and buck-boost converters, but the degree of freedom of the turn ratio can be exploited to relax the constraint on the high duty cycle required to get the high conversion gain [10]. Unfortunately, magnetic losses can be high, especially in *Surface Mounted Device* (SMD) coupled inductors and, more importantly, stresses are increased. In fact, the voltage drop across the secondary switch during the on-time of the main switch (T_{on}) is, with a reasonable $N_s/N_p = 10$, $V_{sec} = N_s/N_p V_{in} + V_{out} = 56V$, a too high value. Also current stress on the primary side is increased a lot. If the turn ratio is decreased, stresses diminish but the benefits on the duty cycle as well.

- Series combination of the previous topologies. Particularly, an unregulated charge pump in series with a boost converter can achieve good performances [12][13], because unregulated charge pumps show good efficiency, while regulation is done by the inductive converter. However, design complexity increases significantly. It could be probably the best solution for higher conversion gain, if a higher output voltage is demonstrated to be better after the last i2MOVE SoC tests.

A choice was made for a DCM boost converter because of its good performances and design simplicity. Moreover, the converter could be reused if a series combination with a charge pump is desired, with just little modifications to adapt it to the new specifications. The schematic of a boost converter is shown in Figure 1.1. Some commercial devices from *Texas Instruments*©[14][15][16] and research papers [17][18][19][20] describing converters with characteristics similar to the subject of this work are taken as references along the whole design process.

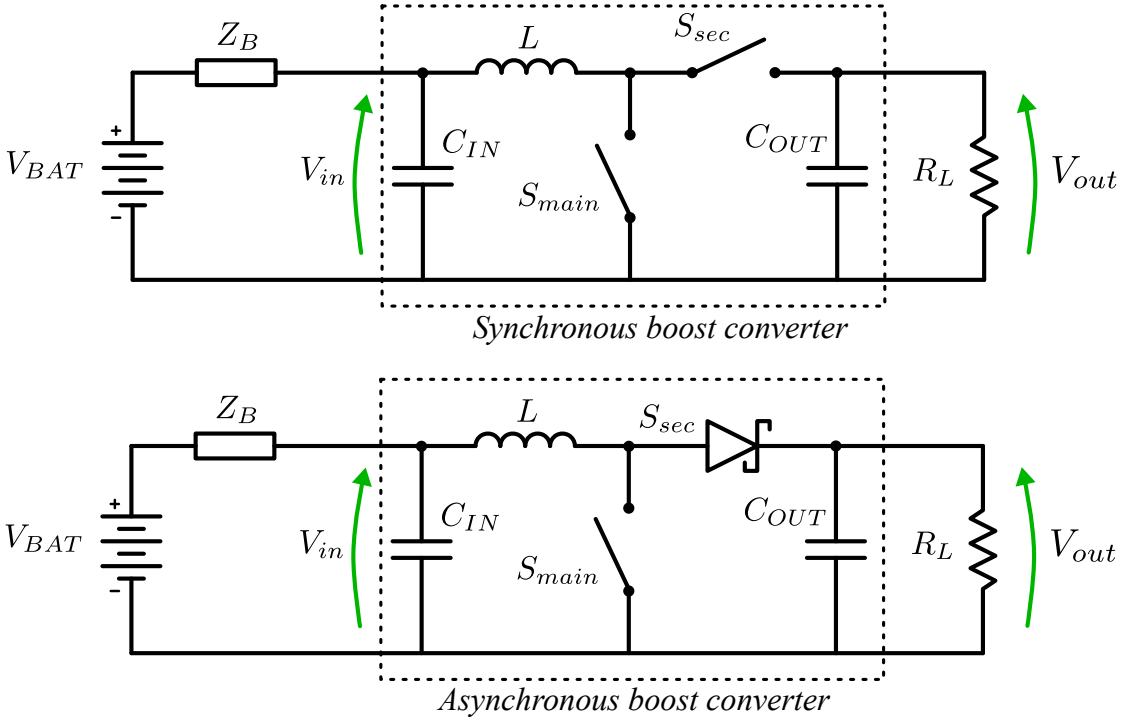


Figure 1.1: Schematic of two boost converters, synchronous and asynchronous.

As explained in the Introduction, an asynchronous boost has been first implemented and only successively a synchronous version too, even if it is well known that the latter shows better performances [10], at least theoretically, due to the lower conduction losses associated to an active switch. This choice is motivated by the fact that an asynchronous boost is simpler in terms of the control architecture, which will consume less power with respect to the synchronous one. Thus the first has been taken as reference for power conversion efficiency and power density and then efforts were made to build a driving control circuit for the synchronous converter which, combined with the power stage, is able to overtake the performances of the asynchronous, confirming theoretical results. Nevertheless, the technology offered by TSMC includes the possibility to use a Schottky diode instead of a classical pn diode. Using this kind of diode, performances could be comparable to the synchronous design, thanks to lower built-in voltage and negligible reverse recovery time. Therefore it is interesting to have both projects fully completed, so that accurate conclusions can be drawn.

Regarding the control technique, a choice was made for a *peak-current mode* control, commonly called just *Current Mode* (CM). This is motivated by the rather simple implementation of the circuit and the many advantages it offers with respect to the classical *Voltage Mode* (VM) control. A block scheme of the CM control

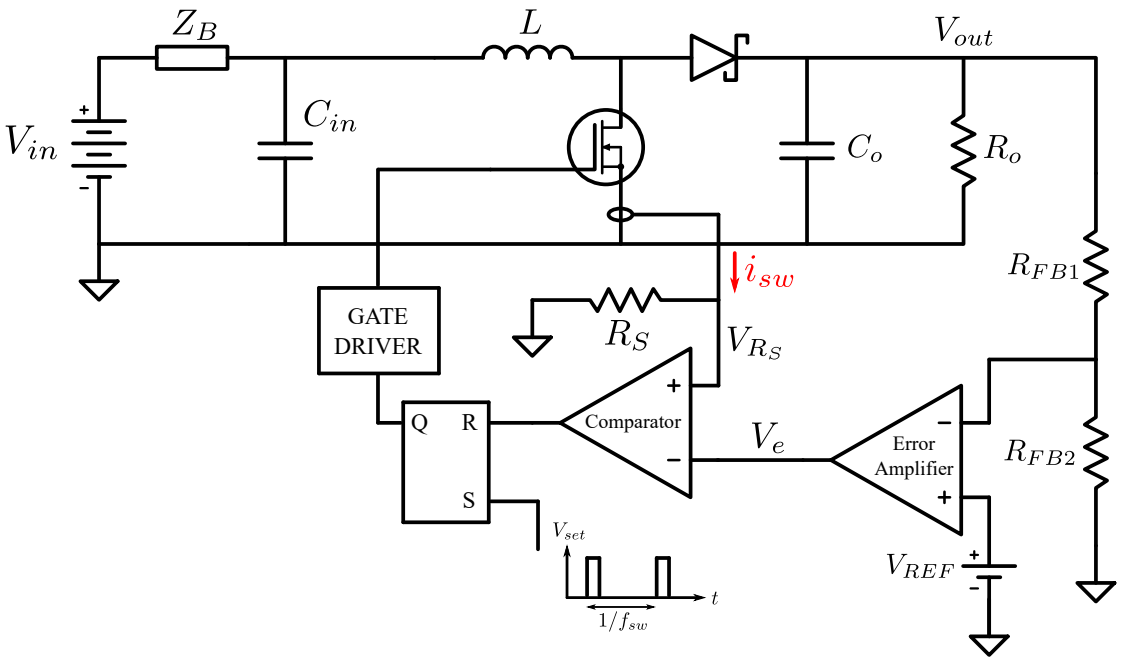


Figure 1.2: Block scheme of the Current Mode control technique.

loop is shown in Figure 1.2. Two quantities are sensed to regulate the duty cycle of the converter, namely the output voltage and the inductor current. Actually the inductor current is not sensed directly, but the active switch one instead. This is not an issue because what is important to sense is the inductor current during t_{on}, which is the very same of the switch one. The reason why it is preferred to sense it there is because the sensing circuit is referenced to ground in that case, while the terminals of the inductor are not. Thus, it is far better for the input range of the comparator. The feedback consists of two loops: an external rather slow, similar to the VM control, and an inner very fast, where the current is sensed. Without entering too much into details, the advantages of a CM control with respect to a VM are the following [10][21][22]:

- the current through the inductor, thus through any components of the circuit, is kept below an absolute maximum value, whatever happens in the converter. This is of paramount importance for reliability and safety;
- the transfer function of the output voltage with respect to the control voltage (V_e) both in CCM and DCM is simpler; specifically, it shows just one pole and one zero, i.e. the double pole associated to the LC network is suppressed. This is translated in an easier and faster realization of the compensator;
- the transfer function has the same structure both in CCM and DCM, thus,

even if the converter passes from one operation mode to the other, the compensator still works quite well;

– the converter is faster to respond to changes of the input voltage, because i_L depends on it directly.

Nevertheless, also disadvantages exist, namely:

– further circuitry to measure the inductor current is needed;

– a periodic instability occurs, known as *sub-harmonic instability*; however, it can be easiliy compensated by adding a ramp to the V_{R_S} signal and, more importantly, it appears in CCM only. Thus, since the converter object of this thesis is working in DCM, this will not be a problem.

More advanced control techniques, such as *Pulse-Frequency Modulation* (PFM), *Resonant control* or *digital control*, have been discarded because of the increasing cost in terms of needed components and complexity. However, a *pulse-skipping function* has been implemented to improve the efficiency at light load, as explained in Section 1.5.1.

1.2 Power stage

The first step in the design of a boost converter is to dimension the power stage, with all the parameters and stresses to be defined. In the first part of this section useful formulas are derived and listed, while the designer's choices on the degrees of freedom are explained and motivated in the following.

In first analysis, simplified assumptions are taken, namely:

– switches are ideal, i.e. the on-resistance (R_{on}) is null and the commutation time is zero; moreover, the inductor is ideal too, leading to an overall 100% efficiency;

– the switching frequency is much smaller than the time constants associated to the circuit, so that exponential waveforms can be approximated well by straight lines;

– output and input ripples are neglected, because they are assumed to be much smaller than the corresponding average voltages;

– the converter is in steady-state or, equivalently, cyclostationary conditions are assumed, i.e. any voltage or current has the same initial and final value.

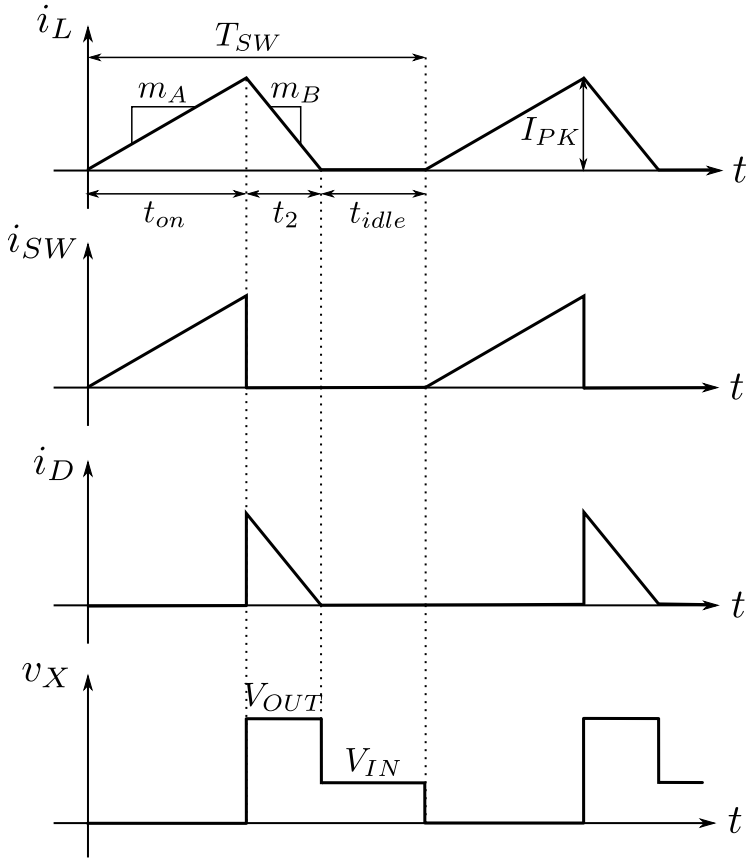


Figure 1.3: Simplified waveforms of a DCM boost converter in steady-state.

Referring to Figure 1.3, the following parameters and quantities can be defined:

$$m_A = V_{IN}/L \tag{1.1}$$

$$m_B = (V_{IN} - V_{OUT})/L \tag{1.2}$$

$$\overline{I_{out}} = \overline{i_D} = \frac{1}{2}\frac{t_2}{T_{sw}} I_{PK} \tag{1.3}$$

$$I_{PK} = \frac{V_{IN} D}{L f_{sw}} \tag{1.4}$$

Assuming that the converter is working at boundary conditions between CCM and DCM, by imposing cyclostationary conditions the value of the conversion ratio M

can be computed:

$$\frac{V_{IN}}{Lf_{sw}}D + \frac{V_{IN}-V_{OUT}}{Lf_{sw}}(1-D) = 0 \quad \Rightarrow \quad M = \frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D} \tag{1.5}$$

Thus, the peak current can be rewritten from Eq. 1.4 as:

$$I_{PK} = \frac{V_{OUT}D(1-D)}{Lf_{sw}} \tag{1.6}$$

Wth the assumption of 100% efficiency, the input current is:

$$P_{OUT} = P_{IN} \Rightarrow I_{IN} = \overline{i_L} = \frac{V_{OUT}}{R(1-D)} \tag{1.7}$$

Putting together Eq. 1.6 and 1.7:

$$\begin{aligned} I_{MAX} &= I_{IN} + \frac{I_{PK}}{2} = \frac{V_{OUT}}{R(1-D)} + \frac{V_{OUT}D(1-D)}{2Lf_{sw}} \\ I_{min} &= I_{IN} - \frac{I_{PK}}{2} = \frac{V_{OUT}}{R(1-D)} - \frac{V_{OUT}D(1-D)}{2Lf_{sw}} \end{aligned} \tag{1.8}$$

The value of the inductance (L^*) allowing the converter to work in DCM in every load condition can be computed by imposing $I_{min} \leq 0$ at heavy load, i.e. R_{min}, inverting Eq. 1.8 and evaluating the worst condition (at D=1/3):

$$L^* = \left.\frac{R_{min}D(1-D)^2}{2f_{sw}}\right|_{D=1/3} \tag{1.9}$$

Once f_{sw} is defined, L^* can be computed. Notice that both the switching frequency and the value of the inductance are degrees of freedom and they should be chosen considering a trade-off among size of the components, losses and speed. Indeed, the higher the switching frequency, the faster will be the transient response because the RHPZ is at higher frequency (see Section 1.3), hence the crossover could be set at higher frequency as well, and size of components will be smaller. Unfortunately, switching losses increase at the same time, so a trade-off should be found, as explained later on in this section.

Coming back to design formulas, the relationship among duty cycle, load resistance and conversion ratio in DCM can be derived by imposing cyclostationary conditions (Eq. 1.10) and by expliciting the output average current (Eq. 1.11):

$$\frac{V_{IN}}{L}t_{on} + \frac{V_{IN}-V_{OUT}}{L}t_2 = 0 \tag{1.10}$$

$$I_{OUT} = \frac{V_{OUT}}{R} = \frac{f_{sw}}{2} \frac{t_2^2 \left(V_{OUT} - V_{IN}\right)}{L} \tag{1.11}$$

Putting on system Eq. 1.10 and 1.11:

$$M = \frac{1 + \sqrt{1 + \frac{RD^2}{Lf_{sw}}}}{2} \tag{1.12}$$

and, by inversion of Eq. 1.12:

$$D = \sqrt{\frac{Lf_{sw}}{R} \left[(2M-1)^2 - 1\right]} \tag{1.13}$$

By knowing D, I_{PK} can be calculated from Eq. 1.4 and next D_2 from Eq. 1.3. All the other current stresses on each component can be evaluated now, but for the sake of brevity they are not reported. They are easy to calculate and can be found in [10] or [11].

All the design equations are now determined. However, the assumption of ideal switches is unrealistic and should be removed in order to design the converter correctly. Indeed, the switching frequency is chosen also according to switching and conduction losses, thus the turn-on and turn-off times and the on-resistance should be defined. Moreover, losses due to the parasitics of inductor and input and output capacitors and due to the resistive sensing of the output voltage (see Section 3.2) should be considered as well. Equations describing these losses are required, hence listed in the following:

$$P_{C_{in,out}} = ESR \times I_{RMS}^2 \tag{1.14}$$

$$P_{FB} = \frac{(V_{OUT})^2}{R_{FB}} \tag{1.15}$$

$$P_{sw_{(SW)}} \approx \frac{f_{sw} \tau_{on,off} V_{OUT} I_{PK}}{2} \tag{1.16}$$

$$P_{cond_{(SW)}} = R_{on} I_{RMS}^2 \tag{1.17}$$

$$P_{sw_{(DIODE)}} \approx \frac{f_{sw} \tau_{on,off} V_{OUT} I_{PK}}{2} \tag{1.18}$$

$$P_{cond_{(DIODE)}} = V_{on} \overline{i_D} \tag{1.19}$$

Losses due to parasitics of the inductor are evaluated using manufacturer's available tool (see Section 1.2.1). Measurements at corner situations are taken, i.e. at the lightest and heaviest loads, and all the losses in between are obtained by linear interpolation of those two points.

Since there are a lot of variables entering into the design and there are several degrees of freedom (L, f_{sw}, R_{FB}, $\tau_{on,off}$, R_{on}, V_{on}), all linked together, an optimum solution in a closed form cannot be found. Thus, an Excel spreadsheet and a MATLAB script have been written to help to achieve a good trade-off among sizes, efficiency and speed. Specifically, the spreadsheet has been used to quickly control all the stresses, the power losses and the frequency behavior (see Section 1.3) by implementing all the design formulas. On the other hand the MATLAB script has been used basically to obtain a good graphical design tool to choose the right switching frequency. The code of the script can be found in the Appendix A.1 of this thesis. Formulas have been rewritten as functions of the output current and the voltage drop across the main switch has been taken into account to compute a more accurate duty cycle.

A good design should have comparable switching and conduction losses. Iterative simulations have been run to obtain such a goal, letting the design parameters vary into reasonable intervals. A satisfactory result has been found with the parameters listed in Table 1.2, with $V_{IN} = 3.3\,\mathrm{V}$, i.e. at the middle of the interval given as specification (see Table 1.1). Figure 1.6 shows one of the output of the MATLAB code: switching and conduction losses are comparable with the chosen parameters. The expected efficiency as a function of the output current range

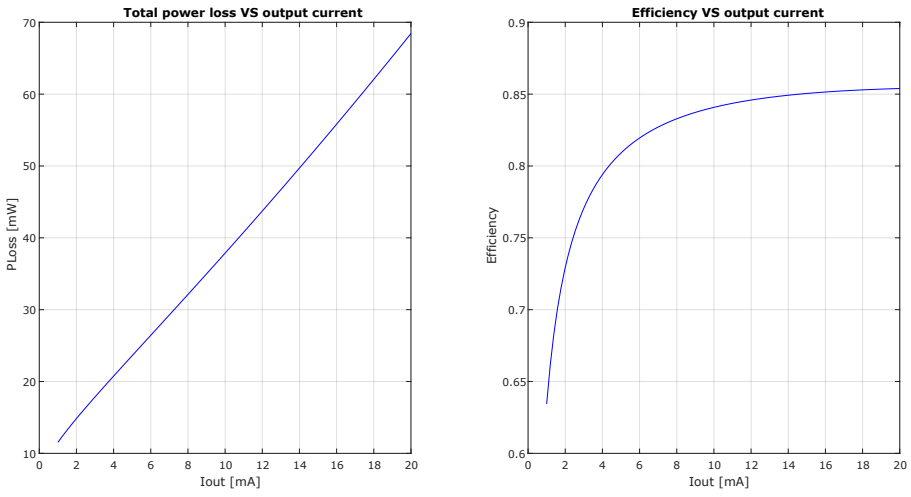


Figure 1.4: Expected losses and efficiency, calculated with the MATLAB script.

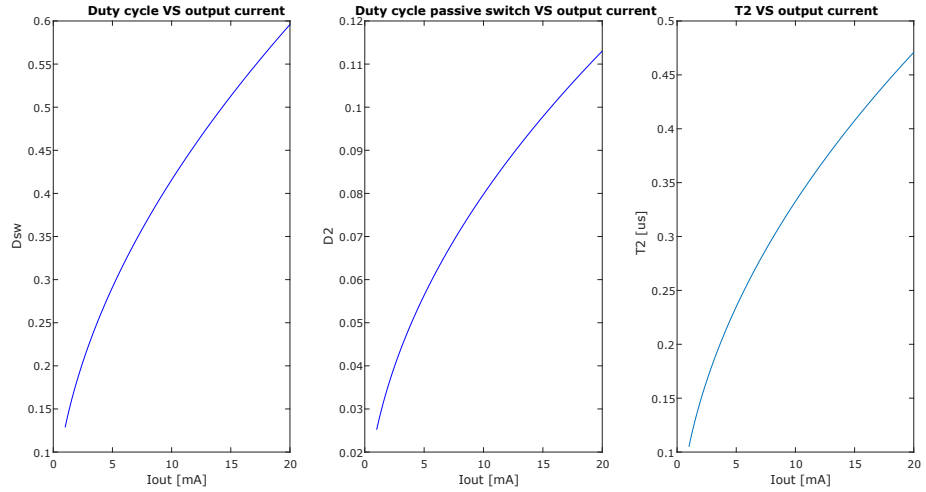


Figure 1.5: Expected duty cycle, as a function of the load current.

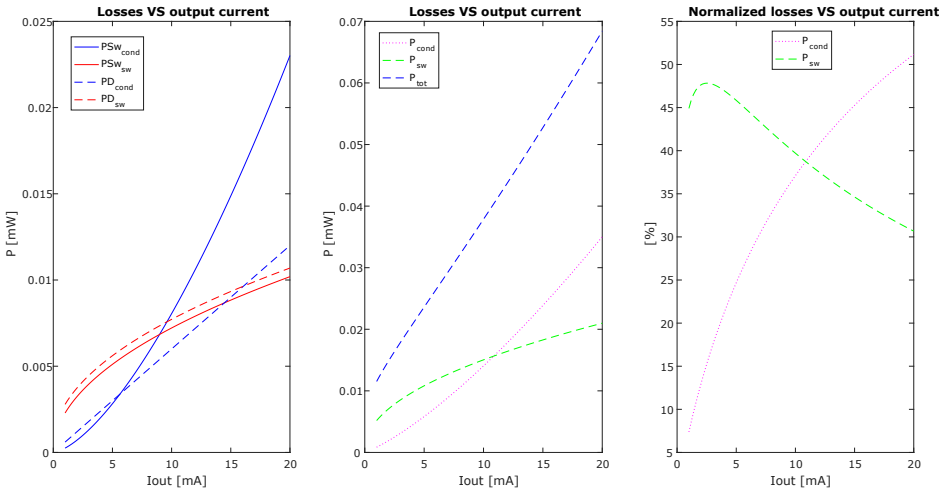


Figure 1.6: MATLAB script result: switching vs conduction losses.

PARAMETER	VALUE
f_{sw}	240 kHz
L	22 µH
R_{on}	0.925 Ω
V_{on}	0.6 V
$\tau_{on,off}$	12 ns
R_{FB}	100 kΩ
R_S	2 Ω

Table 1.2: Converter design parameters.

is reported in Figure 1.4 and the average efficiency is 82.36%. In Figure 1.5 the computed duty cycle over the whole load current interval is reported.

Finally, the size of the switches have been considered as well. An on-resistance of 0.925 Ω can be obtained in the given technology with an n-type MOSFET whose aspect ratio is:

$$\left(\frac{W}{L}\right) = \frac{6\,\text{mm}}{1.8\,\mu\text{m}}$$

which is a reasonable value. Regarding the dimensiond of the Schottky diode, needed to have $V_{on} = 0.6\,\text{V}$, they have been obtained by implementing an equivalent layout cellview in Cadence, whose dimensions are approximately 272 µm × 295 µm. The layout of the n-type MOSFET has been implemented as well, resulting, together with the diode, in an overall area of $0.114\,756\,\text{mm}^2$. Finally, in order to do a valid comparison between synchronous and asynchronous designs, a layout view of an n- and a p-type MOSFET, occupying the same area, has been done. Notice that the dimensions of the n-type MOSFET are increased because the benefit for efficiency is more effective if the on-resistance of the main switch is decreased, rather than the secondary one. This can be seen both with formulas or from Figure 1.6. For the synchronous converter, the dimensions of the n-MOSFET and the p-MOSFET are respectively

$$\left(\frac{W}{L}\right)_n = \frac{12\,\text{mm}}{1.8\,\mu\text{m}}$$

and

$$\left(\frac{W}{L}\right)_p = \frac{8\,\text{mm}}{0.5\,\mu\text{m}}$$

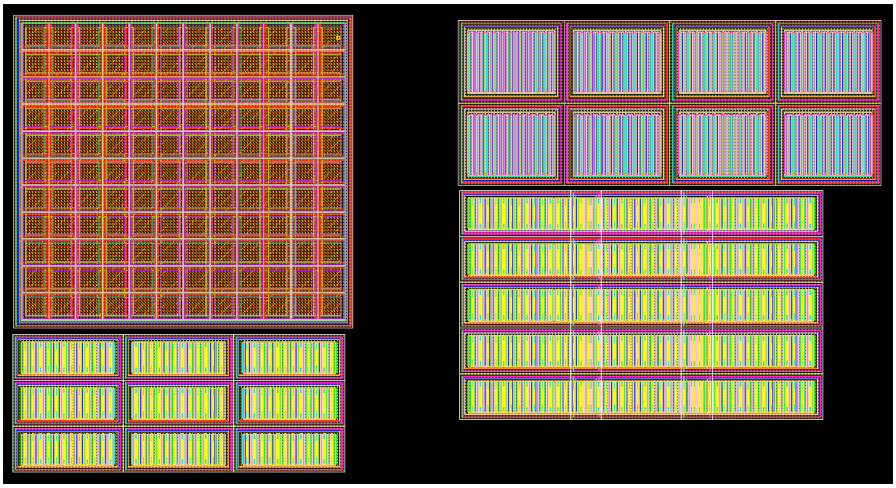


Figure 1.7: Layout cellview of power switches, on the left with Schottky diode, on the right with p-type MOSFET.

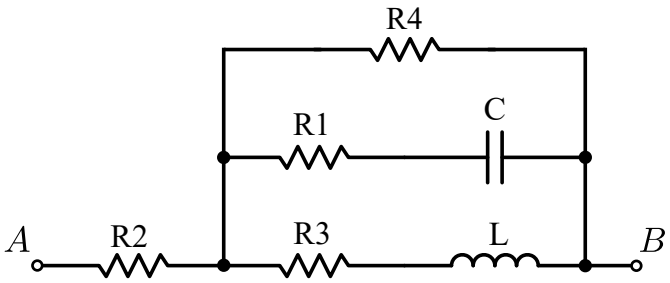
1.2.1 Non-integrated components selection

Inductor

The use of integrated inductors shows several advantages for converters to be used in portable applications, especially in terms of PCB area saving. Nevertheless, performances in efficiency are far worse than discrete components ones and the design of the converter becomes more complex: big values of inductance cannot be obtained, thus the switching frequency must be dramatically higher [23]. Since extreme integration is not required for the converter object of this work, a choice was made to use an external off-chip inductor, with SMD lead-less package to save area.

There are several companies which produce discrete inductors. A selection has been based on reliability and available documentation of their products. Among Vishay©, Murata Manufacturing Co.© and Coilcraft© the last one offers a well-documented catalogue, an online tool to estimate power losses of the inductors rather accurately [24] and equivalent models to be used in circuit simulators like Spectre. A family of low profile shielded power inductors has been selected, LPS6235, because of the small SMD package (6.6 mm × 6.6 mm) and the compliance with the specifications for inductance value and current ratings (saturation current 1.6 A) [25]. Power losses at 240 kHz at full load (peak current of 0.5 A) are estimated to be less than 10 mW, acceptable for the efficiency.

The equivalent circuit used in simulations is shown is Figure 1.8. It includes series DC resistance, resonances and leakage current and the parameters are set on the basis of the document provided by the manufacturer [26].



R1	45 Ω
R2	145 mΩ
R3	127 mΩ
R4	3.272 kΩ
C	3.32 pF
L	21.79 μH

Figure 1.8: Inductor LPS6235-22 µH equivalent circuit.

Input capacitor

The input capacitors bank should provide the AC current required by the converter, allowing a small voltage ripple across it. In order to decouple both high frequency (f_{sw}) ripple and low frequency transients, due to load changes, a parallel of ceramic and bulk capacitors is usually adopted. Regarding the ceramic one, as a rule of thumb the maximum allowed peak-to-peak voltage should be lower than 75 mV, or equivalently the maximum RMS voltage lower than 22 mV [27]. This yields to:

$$I_{PP} = CV_{PP}f_{sw} \Rightarrow C > \frac{I_{PP}}{V_{PP}f_{sw}} = \frac{V_o D(1-D)}{V_{PP}Lf_{sw}^2}\bigg|_{D=0.5} = 52.6\,\text{nF}$$

A 82 nF ceramic capacitor could be picked to be conservative regarding the voltage ripple. The bulk capacitor is instead responsible to control the voltage deviation at the input during output load transient changes. The maximum input step current is given by:

$$\Delta I_{IN} = M\Delta I_{OUT} = \frac{20V}{3V}\,20\,\text{mA} = 133\,\text{mA}$$

According to [27], the minimum required bulk capacitance can be approximated by (L_{st} is the stray inductance associated to PCB traces and representing the finite bandwidth of the supply):

$$C = \frac{1.21\,(\Delta I_{IN})^2 L_{st}}{(\Delta V)^2} \sim \frac{1.21 \times (0.133\,\text{A})^2 \times 200\,\text{nH}}{(0.1\,\text{V})^2} \approx 428\,\text{nF}$$

To be conservative, a 5V 1 µF low-ESR electrolytic or ceramic capacitor could be picked, X7R to be able to work also at high-temperature.

Output capacitor

A ceramic capacitor has been chosen for the output section because it offers the best cost over size trade-off. Moreover, the ESR of ceramic capacitors is negligible and the self-resonance is well above the switching frequency, typically beyond MHz's range. Its capacitance should be high enough to allow a voltage ripple lower than ΔV_o. According to the received system specifications (see Table 1.1):

$$\Delta V_o < 0.1\,\mathrm{V} \Rightarrow C_o > \frac{I_{o_{max}}}{\Delta V_o}\frac{D_{max}}{f_{sw}} = \frac{20\,\mathrm{mA}}{100\,\mathrm{mV}}\frac{0.85}{240\,\mathrm{kHz}} = 708\,\mathrm{nF}$$

A 35V X7R 820 nF ceramic capacitor should be picked to be conservative.

1.3 Transfer function and compensation network

The transfer function of a current-mode boost converter operating in DCM is the following [10][11]:

$$\begin{gathered}\frac{\tilde{v_o}}{\tilde{v}_{ctrl}} = \frac{R_o}{R_S}\frac{\sqrt{MK(M-1)}}{2M-1}\left(\frac{1+sC_o\,ESR}{1+s/\omega_p}\right) \\ M = \frac{V_o}{V_{in}}, \quad K = \frac{2Lf_{sw}}{R_o}, \quad \omega_p = \frac{2M-1}{R_oC_o(M-1)}\end{gathered} \tag{1.20}$$

Nevertheless, in the design a ceramic capacitor has been chosen at the output and its series equivalent resistance is negligible, thus the LHP zero is not present. On the other hand, the above equation has been derived with a simplified analysis. Particularly, the RHP zero associated to the boost converter in CCM has been neglected because it is at rather high frequency, usually around or slightly above half the switching frequency. However, it is very important to know the exact one in order to design a reliable compensator, with a well known phase margin. Taking into account these considerations, Eq. 1.20 can be rewritten as:

$$\begin{gathered}\frac{\tilde{v_o}}{\tilde{v}_{ctrl}} = \frac{R_o}{R_S}\frac{\sqrt{MK(M-1)}}{2M-1}\left(\frac{1-\frac{sL}{R_oD_2^2}}{1+s/\omega_p}\right) \\ M = \frac{V_o}{V_{in}}, \quad K = \frac{2Lf_{sw}}{R_o}, \quad \omega_p = \frac{2M-1}{R_oC_o(M-1)}\end{gathered} \tag{1.21}$$

The transfer function shows one RHP zero and one pole: a type 2 PI lead compensator is therefore needed to ensure high DC gain and good transient response, adding a zero and a pole to the power stage transfer function. The closed-loop transfer function should exhibit in fact ideally infinite DC gain and bandwidth,

with a good phase margin, i.e. a single pole response. This is translated practically in the highest possible DC gain, with a bandwidth much lower than the switching frequency (around one-tenth) and, as a rule of thumb, below one-third to one-fifth of the RHPZ frequency, to ensure good phase margin [28]. However, the DC gain and the frequency of the RHPZ and the pole both depend on the load. Thus, a worst case condition should be found in order to design an effective compensator. While the frequency of the pole is linearly proportional to the inverse of the load resistance, the DC gain depends on its square root: therefore the lower the load resistance, the higher the crossover frequency. Regarding stability, the highest closed-loop crossover frequency, i.e. the lowest phase margin, is reached consequently at minimum R_{out}. Figure 1.9 demonstrates graphically the asymptotic analysis. Plots are obtained using Matlab from Eq. 1.21, with all the parameters set according to previous design (see Table 1.1 and 1.2).

G_0	max
f_{p1}	origin
f_z	422 Hz
G_{comp}	4.24
f_{p2}	150 kHz

Table 1.3: Compensator specifications on the transfer function.

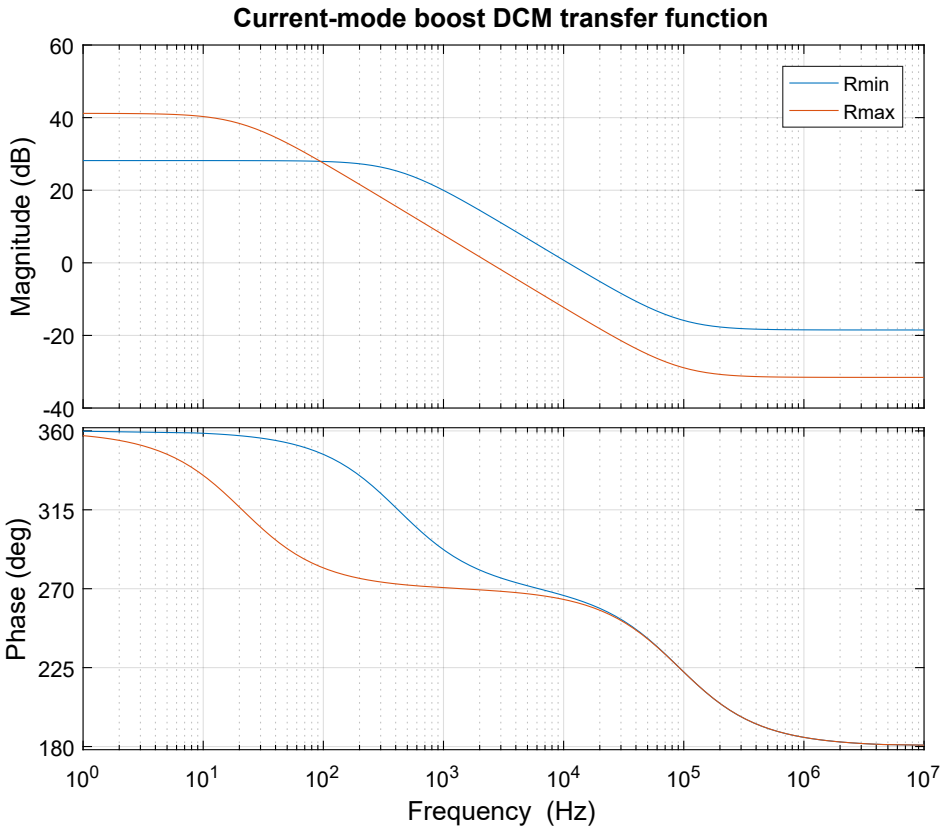
The compensator must provide then a very high DC gain, a pole in the origin, a zero at $f_p = 422\,\text{Hz}$ and possibly a second pole at high frequency to cutoff switching noise. A reasonable trade-off between stability and bandwidth should be first taken to set the closed-loop crossover frequency. Choosing $f_c = 30\,\text{kHz}$, i.e. one-third of f_{RHPZ} and about one-tenth of f_{sw}, and assuming that the second pole of the compensator is at $f_{p2} = 150\,\text{kHz}$, the phase margin will be:

$$\phi_m = 90^\circ - \arctan\left(\frac{f_c}{f_{RHPZ}}\right) - \arctan\left(\frac{f_c}{f_{p2}}\right) = 90^\circ - 18.4^\circ - 11.3^\circ \approx 60^\circ$$

This is a good trade-off because a phase margin of 60° is enough for stability, just few ringings in the step response will appear. Moreover, phase margin increases with increasing load resistance, thus 60° is the worst case, at mimimum R_o. In order to get a crossover at 30 kHz, the compensator must provide a flat gain above f_p, whose value is (see Section 1.5.2 for the explaination of the term $G_{R/R}$):

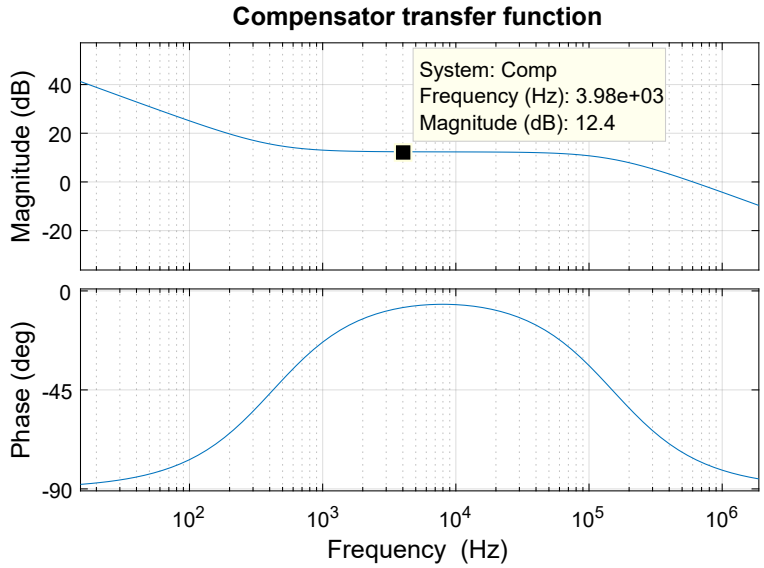
$$G_{comp} = \frac{f_c}{f_p}\ \frac{1}{G_{DC}\,G_{R/R}} = \frac{30\,\text{kHz}}{422\,\text{Hz}}\ \frac{1}{25 \times 0.67} \approx 4.24$$

Figure 1.10 shows Bode plots of the compensator and the closed-loop gain while specifications are listed in Table 1.3.

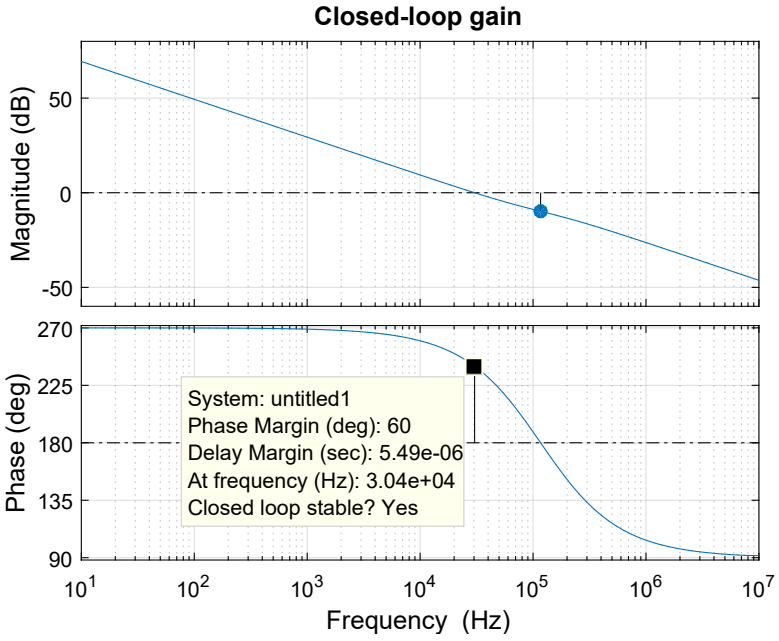


Load resistance	1 kΩ	20 kΩ
f_{RHPZ}	90 kHz	90 kHz
f_p	422 Hz	21 Hz
G_{DC}	25	114

Figure 1.9: Current-mode boost DCM transfer function.



(a)



(b)

Figure 1.10: Compensator (a) and closed-loop gain (b) transfer functions.

1.4 Start-up phase

In this phase the load is disconnected or, equivalently, the H-bridge of the neural stimulator is fully off. The control circuitry should provide a way to charge the output capacitor from a low voltage up to the high steady-state value without damages or high stresses. For efficiency reasons, in fact, the converter is turned on only when the stimulator is active, otherwise is kept off.

When the boost converter is off the output voltage equals the input voltage minus the diode's threshold. If the converter is then turned on and the normal feedback loop is used to control the duty cycle, until the output voltage reaches its steady-state value the error amplifier's output will be maximum, thus the duty cycle too. During T_{on} the inductor charging slope is V_{in}/L, while during T_{off} $(V_{in} - V_{out})/L$. This means that during the first cycles the inductor is charged also during T_{off} and only when V_{out} is high enough the inductor current can reach again zero. In other words, in the first periods the converter operates in CCM and the inductor current increases cycle by cycle, possibly also a lot; only when V_{out} reaches a sufficiently high value the converter goes in DCM, working as it should. This phoenomenon is called *in-rush current* and could lead to damages to the devices because the current could reach values higher than the maximum ratings. Obviously this must be avoided.

A possible approach is to break the feedback loop during start-up imposing a predefined increasing duty cycle, so that the maximum current can be controlled. Although it is a simple solution, it is not so reliable because the converter would operate with an open-loop control. The output voltage would not be sensed indeed.

A better solution is to impose a non-constant reference voltage to the error amplifier of the normal control circuitry. The feedback loop is closed, which is far better in terms of reliability. Specifically, the reference voltage should start from zero and increase up to the steady-state value in a defined time τ_{SS}, as shown in Figure 1.11. First of all, with this technique the current is kept below a given threshold thanks to the current mode inner feedback loop (see Section 1.5.2). It is possible that the converter operates in CCM, but at least it is ensured that the current will not overcome a certain prefixed value. Nevertheless, although the peak ratings are the most critical, also the average current should not be too high. In order to guarantee this the soft-start time τ_{SS} should be long enough.

Assuming ideal lossless components, a simplified computation of the mimimum soft-start time can be carried out by imposing the energy conservation principle. Supposing an average duty cycle D_{avg} over the whole soft-start period, the energy stored in the inductor in each cycle, if current reaches zero before the end of each

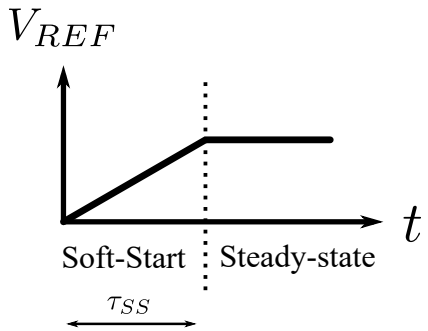


Figure 1.11: Time waveform of the compensator reference voltage during start-up.

switching period, is:

$$\varepsilon_L = \frac{1}{2}L(I_{PK})^2 = \frac{1}{2}L\left(\frac{D_{avg}V_{in}}{Lf_{sw}}\right)^2 \tag{1.22}$$

The required energy to charge the output capacitor from 0V (simplified but conservative computation, because V_{out} starts actually for $V_{in} - V_D$, not 0V) to its steady state value V^*_{out} is:

$$\varepsilon_{C_{out}} = \frac{1}{2}C_{out}(V^*_{out})^2 \tag{1.23}$$

The minimum number of cycles required to charge the output capacitor is therefore:

$$N_{min} = \frac{\varepsilon_{C_{out}}}{\varepsilon_L} \tag{1.24}$$

By choosing a reasonable value of $D_{avg} = 0.5$ (too high duty cycle means fast start-up but high stress, while too low duty cycle slow start-up but no stress):

$$N_{min} = \frac{\frac{1}{2}C_{out}(V^*_{out})^2}{\frac{1}{2L}(\frac{D_{avg}V_{in}}{f_{sw}})^2} = \frac{LC_{out}(f_{sw}V^*_{out})^2}{(D_{avg}V_{in})^2} =$$
$$= \frac{22\,\mu\text{H} \times 820\,\text{nF} \times (240\,\text{kHz} \times 20\,\text{V})^2}{(0.5 \times 3.3\,\text{V})^2} \approx 153$$

Finally:

$$\tau_{SS} \geq \frac{N_{min}}{f_{sw}} = \frac{153}{240\,\text{kHz}} = 637.5\,\mu\text{s}$$

In order to be safer and to take into account also losses, a greater time should be chosen. A good solution could be $\tau_{SS} = 1\,\text{ms}$.

Nevertheless, in the previous analysis the first phase of start-up has not been considered. When the chip is not supplied, i.e. when the battery is not inserted in the holder that will be mounted on the PCB, the output voltage is really zero. But once the battery is placed, an uncontrolled current spike will appear, due to the fact that a voltage drop is present across the inductance. The circuital topology is basically an LC filter with a step voltage provided at input, but with a diode letting the current flowing in one direction only, namely towards the output. According to circuit theory, the peak current is:

$$I_{PP} = V_{PP}\sqrt{\frac{C_{out}}{L}} = 3.3\,\mathrm{V} \times \sqrt{\frac{820\,\mathrm{nF}}{22\,\mu\mathrm{H}}} = 637\,\mathrm{mA}$$

and the sinusoid period:

$$T_{sin} = 2\pi\sqrt{LC_{out}} = 2\pi\sqrt{22\,\mu\mathrm{H} \times 820\,\mathrm{nF}} \approx 26.7\,\mu\mathrm{s}$$

Since the current in unidirectional, only half-period will be present, whose duration is 13.35 µs. Even if these values are really yet safe for the components (they are designed to operate up to 1A), this computation is valid only with ideal lossless components and the voltage drop across the diode has not been considered. With real components and including diode's drop, the peak current will be lower. Hence, this phase of the soft-start transient can be safely neglected.

1.5 Critical events

1.5.1 Output over-voltage protection

When the H-bridge of the stimulator is turned off, an open circuit load appears at the output of the converter. Particular care should be provided in this part of the design in order to avoid over-voltages at the output, which can lead to faults possibly, if junction breakdown voltage maximum ratings are not satisfied (24 V for Schottky diodes and p-MOSFETs, from TSMC PDK). Actually, the control loop is sufficient to guarantee that the voltage does not overcome its steady-state value, excluding a negligible tolerance due to non-infinite gain and bandwidth of the compensator. Indeed, if the sensed scaled output voltage goes higher than the reference voltage, the negative feedback will decrease the duty cycle, ideally to zero. The main switch will be kept open until the output voltage reaches again a value close enough to the steady-state value, then the error amplifier output increases and the duty cycle as well. The practical effect is that for some cycles the duty cycle is zero, thus some pulses are skipped: that is why this kind of function is commonly called *pulse-skipping* [29] and it is similar to another type of

modulation used in power electronics, *Pulse Frequency Modulation* [30]. Another very important benefit of these techniques is the improvement of efficiency at light load. Indeed, if the duty cycle is very low, the energy transferred to the output will be very low as well, but switching and quiescent losses still remain unchanged, resulting in poor efficiency. A pulse-skipping modulation, on the contrary, lets switching losses decrease because the skipped pulses do not contribute. As a drawback, the output voltage ripple will be higher because the actual switching frequency is reduced.

Regarding practical implementation, focusing on over-voltage protection only, the normal control loop cannot provide the desired function: the problem resides in the fact that the output of the error amplifier cannot reach exactly zero in real designs. Thus the main switch could be turned on for an even very short time, but enough to transfer some energy to the output and increase the output voltage consequently. A possible solution could be to introduce an offset between the output of the error amplifier and the comparator, as shown in Figure 1.12. This

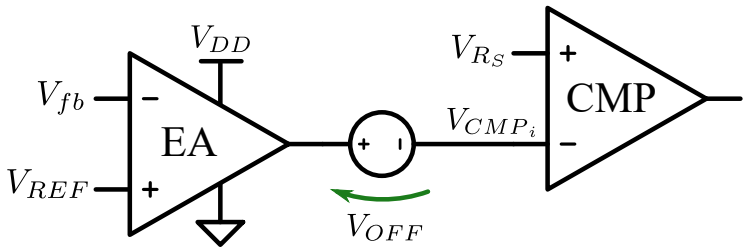


Figure 1.12: Possible over-voltage protection implementation.

solution works because the high DC gain of the error amplifier compensates the introduced offset. It is very simple to implement (a diode-connected MOSFET could be used for instance), but has two drawbacks: the output range of the error amplifier is reduced significantly and, more important, efficiency is not improved because pulse-skipping is present in over-voltage situations only, not at light load.

To solve the issues, a comparator with hysteresis is placed instead of a simple one. It provides both over-voltage protection and pulse-skipping mode to improve light load efficiency. This solution is used also in commercial devices, such as Texas Instruments boost LM5122 [14]. Assuming for the sake of simplicity that the positive and negative threshold voltages are the same, namely V_{hyst}, when the comparator state passes from '0' to '1', the effective voltage to be compared (V_{CMP}) is the output of the error amplifier (V_{EA}) minus the threshold, i.e. $V_{CMP} = V_{EA} - V_{hyst}$. If V_{EA} is low enough, V_{CMP} can become negative, thus the output of the comparator will be always '1', since the minimum voltage at the positive input (V_{R_S}) is zero, cannot go below. In the feedback loop it is therefore sufficient

to design the *Set-Reset* (SR) flip-flop with "reset priority" to ensure that any pulse is skipped under the condition $V_{EA} < V_{hyst}$. Figure 1.13 explains the concept graphically.

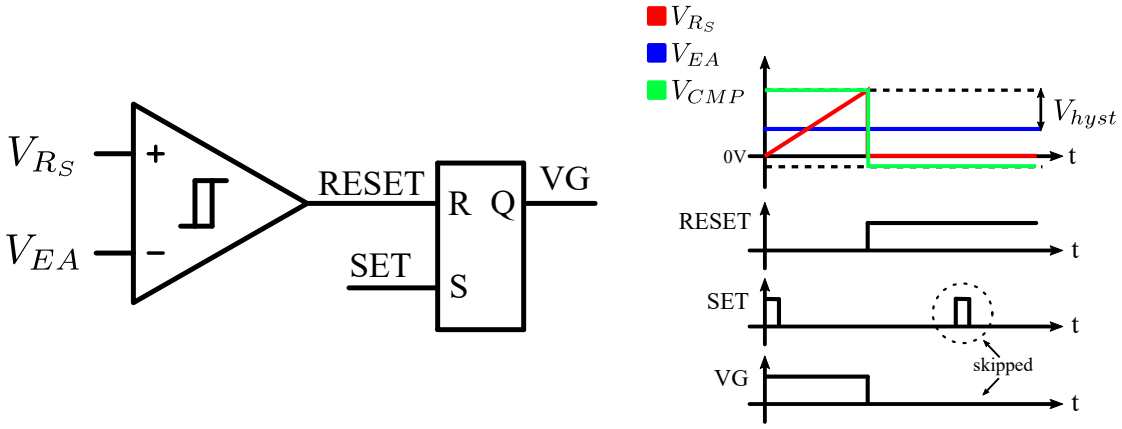


Figure 1.13: Pulse-skipping mode waveforms.

With this techniques both over-voltage protection (duty cycle is zero for $V_{EA} < V_{hyst}$) and pulse-skipping mode at light load are achieved, with a very simple design. Moreover, adding hysteresis to the comparator improves reliability because any input noise whose amplitude is lower than the hysteresis threshold will be cut off [31].

1.5.2 Over-current limiting

The over-current limiting protection is ensured by designing the feedback loop in such a way that the voltage at the input of the comparator does not exceed a certain value, corresponding to the desired maximum current. Indeed, once the R_S factor is fixed, if at the negative input of the comparator the voltage does not overcome a value V^*, the maximum current will be:

$$I_{MAX} = \frac{V^*}{R_S} \tag{1.25}$$

Both R_S and V^* are degrees of freedom in the design. Regarding the latter, it can be set by scaling down the output of the error amplifier with a resistive divider, whose factor is called $G_{R/R}$. Indeed, by referring to Figure 1.14, if the amplifier is supplied with a voltage V_{DD}, the maximum value of the error amplifier output voltage will be $V_{EA}^{max} = V_{DD}$ and thus $V_{comp}^{max} = V^* = V_{DD}\frac{R_2}{R_1+R_2}$. Since V_{DD} is precise, because it is the output of a linear regulator (it is the supply voltage

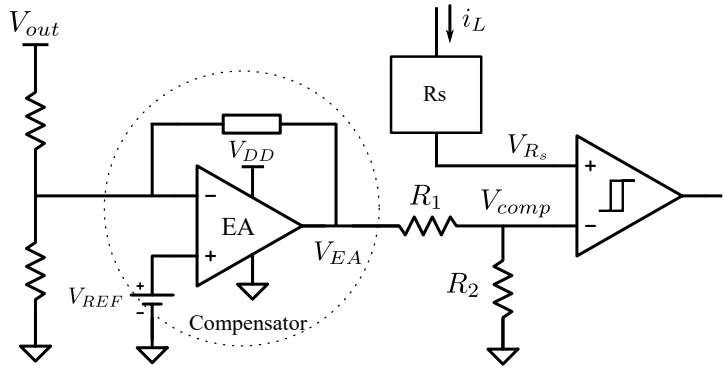


Figure 1.14: Block scheme of the current limiting function.

of the whole digital and analog low power circuitry), and ratios of resistances in ICs are accurate too, the maximum current is fixed with a good tolerance. With $V_{DD} = 1.8\,\text{V}$, $R_2 = 100\,\text{k}\Omega$, $R_1 = 50\,\text{k}\Omega$ and $R_S = 2\,\Omega$, the maximum current is:

$$I_{MAX} = \frac{V_{DD} G_{R/R}}{R_S} = \frac{1.8\,\text{V}\,\frac{100\,\text{k}\Omega}{50\,\text{k}\Omega + 100\,\text{k}\Omega}}{2\,\Omega} \approx 600\,\text{mA}$$

In this way, whatever happens in the system, a maximum voltage of 1.2 V at the input of the comparator is ensured, which is translated into an absolute maximum current of 600 mA. This is paramount for safety in a power converter.

1.5.3 Output short-circuit protection

Load short-circuit protection is a very important feature, especially in terms of reliability: it avoids faults and damages to devices at the expense of some added circuitry, but usually it is worth it. However, in boost converters obtaining that is not easy because one of the terminals of the inductor is always connected to the input voltage. If at the load a short-circuit happens, both switches connects the common node V_X to the reference 0 V. The Schottky diode will conduct and offer a path for the inductor current, which increases until the voltage drop across the diode equals the input voltage. This results in a huge current typically, able to destroy the device. Even if a p-MOSFET is used instead of the Schottky diode and it is kept open, the body diode will conduct as well.

A possible solution could be to connect the cathode of the diode (Schottky or body) either to the output, in normal operation, or to the input, in protection mode, as shown in Figure 1.15. In this way a reverse polarity voltage can be applied across the inductance, enabling a way to discharge it safely. The voltage applied

is in fact the series of the voltage drops across the diode and the on-resistance of the switch used to select the cathode connection point. The energy stored in the inductor is released to the input capacitor: that is not a problem because it is a small amount of energy, thus it generates a negligible voltage drop across C_{IN}.

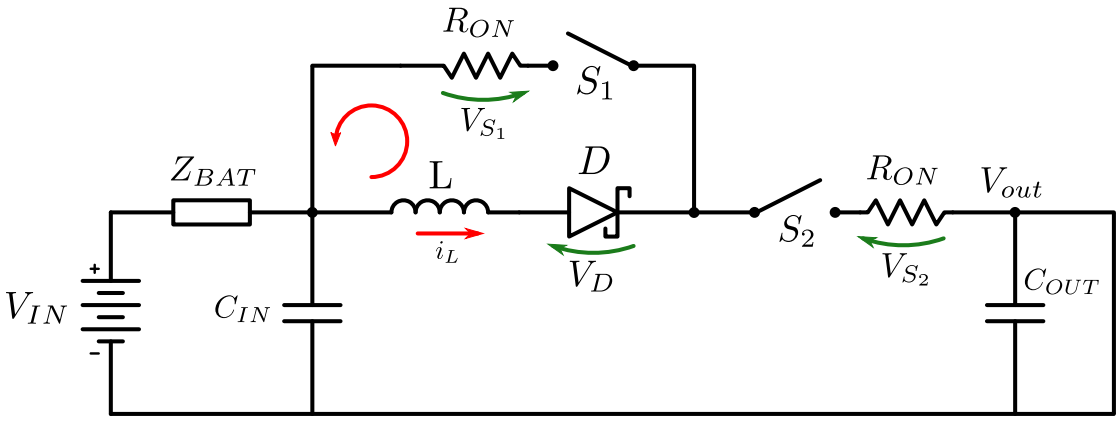


Figure 1.15: Possible short-circuit protection circuit.

Although the proposed solution is effective, it is very expensive in terms of area. During normal operation, indeed, all the current going to the load passes through the on-resistance of S_2, if the Schottky diode design is adopted. The efficiency will be therefore dramatically reduced, unless S_2 (i.e. a MOSFET) is big enough to guarantee $V_{S_2} << V_D$. The dimensions of the switch S_2 in such case could be comparable to the power MOSFETs ones. Regarding the p-MOSFET design, the current passes through the on-resistance of S_2 during the body diode conduction period only, in the order of 20 ns. The efficiency drop could be therefore smaller, but simulations show that they are still non-negligible, more than 5% still for a high occupation of area.

Therefore a choice was made not to protect the converter from output short-circuit, because it is worthless in terms of benefits over costs. A short-circuit could happen if either the H-bridge of the stimulator is damaged, and then the whole chip has to be substituted, or the output is shorted unintentionally during mounting and testing. Particular care should be taken thus during the aforementioned activities.

Chapter 2

Verilog-A model based design

Verilog-AMS is a Hardware Description Language which lets the designer create modules, systems and subsystems, implementing also complex analog or mixed signals functions. The behavior of each module can be described mathematically and can be parameterized to adapt it to specific applications. The power of such kind of design approach is that overall system functionality of complex systems can be verified rather easily by simply writing some lines of code. This lets the designer save a lot of time in the transistor-level design process. In fact, Verilog-A HDL permits basically a higher level of abstraction. For instance, if an op-amp is needed but the required minimum gain bandwidth product and gain are not known exactly, some parametric simulations could be run and constraints extracted from the results. By doing this, only the parameters of the model change, thus the user avoids many redesign of transistor-level schematics. A complete and exhaustive manual for Verilog-AMS language modelling is available online [32], provided by Accellera Organization©.

For the sake of brevity and for reading fluency, in the following sections only relevant code lines are reported. The full code of each Verilog-A module is reported in the Appendix A.2 of this thesis.

2.1 Control loop

Since the power stage presents only single component elements, namely power MOSFETs, capacitors and inductor, Verilog-A modules are not necessary for simulating its behavior. On the contrary, in the control loop, shown in Figure 2.1, several blocks need to be described, namely:

- operational amplifier, used in the type 2 compensator;
- current sensor;

- comparator without and with hysteresis;
- set-reset flip-flop;
- gate driver, including the lever shifter.

Any voltage or current reference has not been designed because a bandgap reference already exists in the SoC of the i2MOVE project. Also the low-voltage supply $V_{DD} = 1.8\,\mathrm{V}$ is already regulated linearly. At the moment an external oscillator is used to generate the switching frequency of the machine learning engine, but in the future it will be integrated as well, once the SoC will be successfully tested. For this reason, also the design of the oscillator is not object of this thesis and will not be treated. For simulation purposes, a simple ideal voltage generator is used to produce the pulses which set the switching frequency of the converter, while ideal current or voltage DC sources are exploited as references.

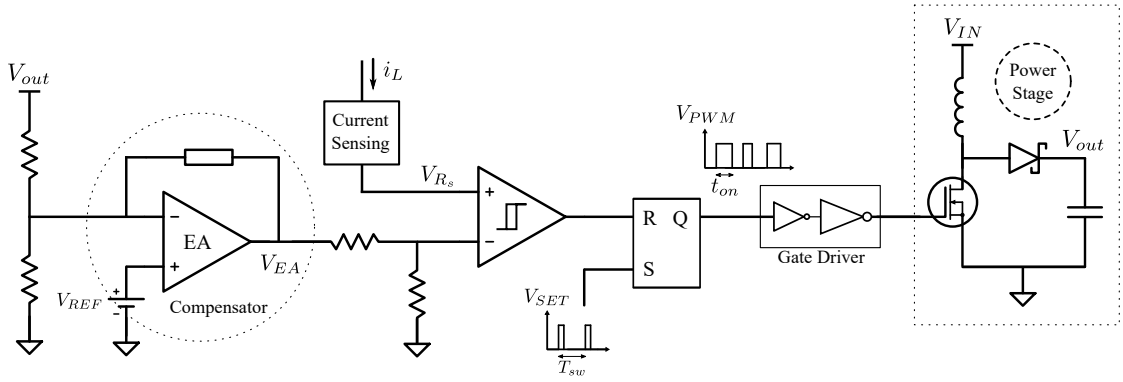


Figure 2.1: Control loop block diagram.

2.1.1 Operational amplifier

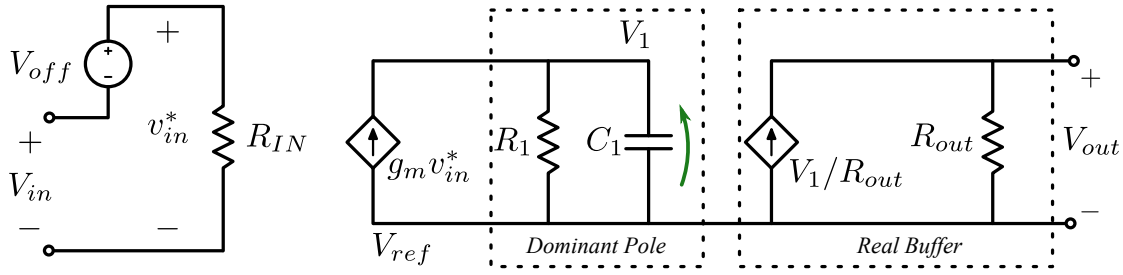


Figure 2.2: Op-amp Verilog-A circuit equivalent model.

The op-amp equivalent circuit is shown in Figure 2.2. It is basically the model of a compensated real operational amplifier, with one dominant pole, finite input and output resistances, input offset voltage and limited transconductance and current driving capabilities.

The initial parameters of the model are the input offset voltage (`Vin_offset`), the input resistance (`Rin`), the gain (`gain`), the gain-bandwidth product (`GBW`), the maximum driving current (`Imax`), the slew rate (`SR`), the output resistance (`Rout`) and finally the output drop voltage (`Vsoft`). From these parameters the transconductance `gm`, the RC network defining the dominant pole (`r1`,`c1`) and the maximum input voltage (`vmax_in`) causing op-amp's saturation are calculated according to conventional amplifiers analysis:

```
1     @ ( initial_step or initial_step("dc") ) begin
2         c1 = Imax/(SR);
3         gm = 2 * `PI * GBW * c1;
4         r1 = gain/gm;
5         vmax_in = Imax/gm;
6     end
```

The input stage is modeled as a real transconductor, with input offset voltage, finite input resistance and limited maximum output current:

```
1     //
2     // Input stage.
3     //
4     vin_val = V(vin_p,vin_n) + Vin_offset;
5     I(vin_p, vin_n) <+ vin_val/ Rin;
6
7     //
8     // GM stage with limited output current.
9     //
10    if (vin_val > vmax_in)
11        I(vref, cout) <+ Imax;
12    else if (vin_val < -vmax_in)
13        I(vref, cout) <+ -Imax;
14    else
15        I(vref, cout) <+ gm*vin_val;
```

In parallel to the transconductor, i.e. to the *Voltage-Controlled Current Source* (VCCS) an RC network is added to emulate the dominant pole typical of a compensated op-amp. The values of `r1` and `c1` are calculated as shown before, ac-

cording to `SR`, `gain`, `Imax` and `GBW` parameters. The voltage across this stage (V_1) is then buffered with another VCCS with finite parallel resistance `Rout`. Thus, if the amplifier drives a capacitive load, a second pole associated to the output will be present. Finally a voltage drop due to non rail-to-rail output swing is modeled by adding an opposite current on the transconductance stage as following:

```
1       //
2       // Soft Output Limiting.
3       //
4       if (V(vout,vref) > (V(vsppply,vref) - Vsoft))
5           I(cout, vref) <+ gm*(V(vout, vsppply)+Vsoft);
6       else if (V(vout,vref) < Vsoft)
7           I(cout, vref) <+ gm*(V(vout,vref)-Vsoft);
```

The model is accurate and realistic because it includes the main non-idealities and non-linearities typical of a real ap-amp. Some simulations have been carried out to verify the correct behaviour of the cell.

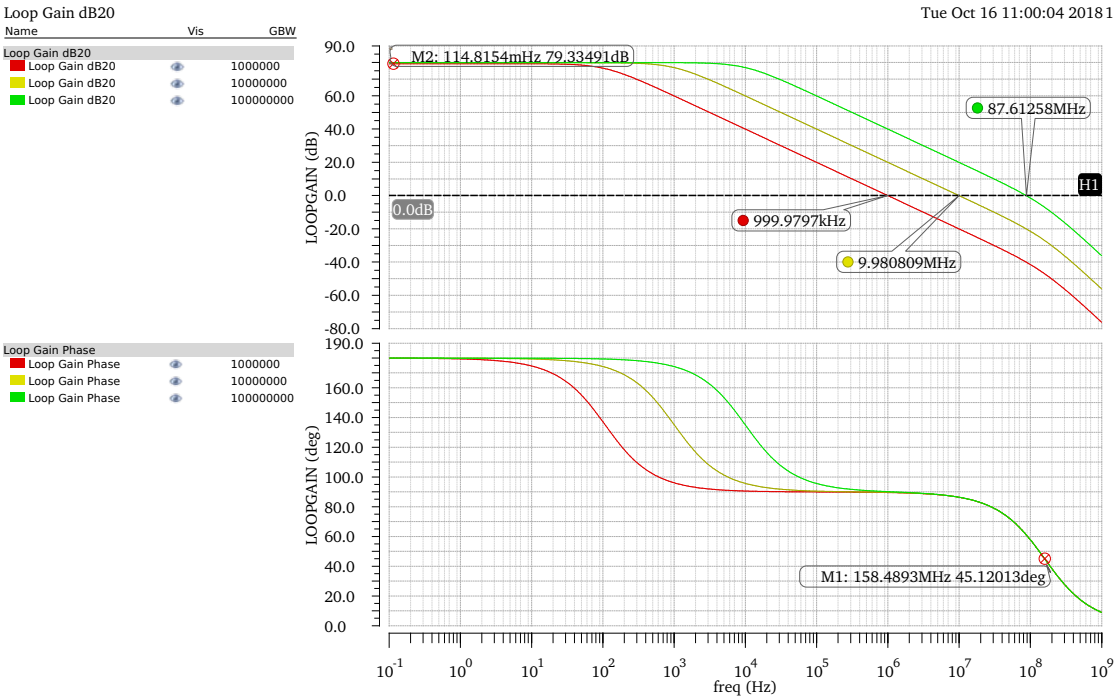


Figure 2.3: Verilog-A op-amp module stb analysis simulations.

In Figure 2.3 graphical results of stability analysis are shown. The Verilog-A module with parameterized gain-bandwidth product has been simulated with

the "Parametric Analysis ADE L" tool. The DC gain is set to 10000 (equivalent to 80dB), the output resistance 1 kOhm and the load capacitance 1 pF, leading to a second pole at frequency 159 MHz, and the gain-bandwidth product 1 MHz, 10 MHz and 100 MHz. Simulation shows the correct behavior of the module.

2.1.2 Set-reset flip-flop

The main code for the SR flip-flop is reported in the following:

```
1     @(initial_step) begin
2         memory = 0;
3     end
4
5     if (V(reset,vref) >  thresh)
6         memory = 0;
7     else if (V(set,vref) > thresh)
8         memory = 1;
9
10    V(q,vref) <+ transition(memory*V(vsupply,vref),
11                  delay_, rf_time, rf_time);
```

The parameters of the model are the threshold voltage for the set and reset signals (`thresh`), typically at half the supply voltage, the delay time for the output to reach the right value (`delay_`) and the rise and fall delay times (`rf_time`), assumed to be equal for the sake of simplicity. In order to implement the memory function of the flip-flop, an internal integer variable `memory` is defined: at the beginning it is initialized at value '0' and then it is determined according to the amplitude of the set and reset voltages. The reset signal has a higher priority with respect to the set one, avoiding in this way conflicts if for any reason both signals are asserted at the same time. The transition filter is used to smooth the strict square wave signal given by `memory`, thus a more realistic output voltage is obtained, helping software convergence as well. The output voltage will be therefore the `memory` signal delayed by a time `delay_`, with rising and falling edges slope `rf_time`.

Although the model is valid and functional in transient simulations, in other types of analysis, such as *periodic steady state* (pss), *periodic ac* (pac) or *periodic stability* (pstb), Spectre returns some errors due to the use of so called *hidden state variables*. Basically time derivatives `ddt` or time integrals `idt` are the only way to implement a memory function, while temporary variables, such as `memory`, are classified as *hidden state variables* and cannot be used in the aforementioned analyses. Since redefining the model by using the allowed operators only is not

trivial at all, a choice was made to use in this design step yet a transistor-level cell. The schematic of a flip-flop is in fact really very simple, i.e. two cross-coupled `NOR` gates. In order to avoid the forbidden combination of set and reset signals both asserted, leading to meta-stability, a `NOT` and an `AND` gate are added as shown in Figure 2.4. Doing so, the reset signal has a higher priority because when `RESET='1'` the `AND` gate disables the `SET` signal.

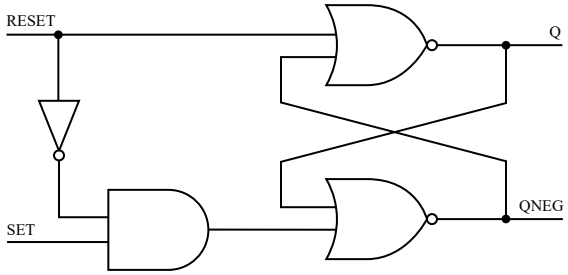


Figure 2.4: SR flip-flop, with reset priority.

2.1.3 Comparators

Although the model of the op-amp could work also for a comparator, a simpler one has been adopted to speed up simulations, implementing simple mathematical functions. For a comparator without hysteresis, the model is a hyperbolic tangent function with the input voltage boosted with a gain G:

$$V_{out} = A \times \tanh(GV_{in}) \tag{2.1}$$

Regarding the comparator with hysteresis, the model is a bit more complex because it needs some memory to keep trace of the state of the comparator, in order to set the threshold at the right value. Nevertheless, this implies the use of a *hidden state variable* causing the problems described in section 4.2.2. This model has been used therefore in transient analysis only; in other type of simulations the simple comparator model has been chosen. The main code is reported in the following. `offset` is the hysteresis threshold offset, `state` is the variable used to keep memory, `t_delay` is the time delay applied to the `state` square wave to emulate processing delays using the transition filter, while `t_rf` is the rising and falling time delay.

```
1     state = V(in_p,vref) > (V(in_n,vref) + (state ?
2         -offset : offset)) ? 1:0;
3     V(out,vref) <+ transition(state*V(vsup,vref),
4         t_delay, t_rf, t_rf);
```

2.1.4 Current sensor

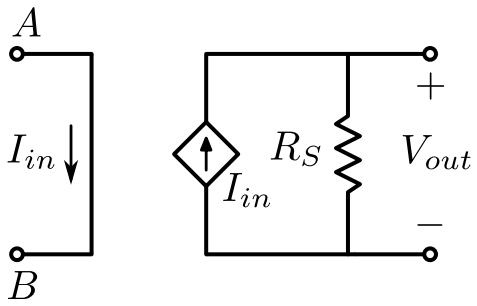


Figure 2.5: Ideal current sensor Verilog-A circuit equivalent model

The model of the current sensor is a *Current-Controlled Voltage Source* (CCVS). It is an ideal current sensor, thus not very realistic, especially for the input stage, but for the purpose of system functionality verification it is sufficient. The equivalent circuit is shown in Figure 2.5. The only parameter of the model is the conversion factor R_S. The output voltage is therefore:

$$V_{out} = R_S I_{in} \tag{2.2}$$

A delay is not added in the model, but could be easily implemented inserting a capacitance in parallel to the resistance R_S.

2.1.5 Gate driver

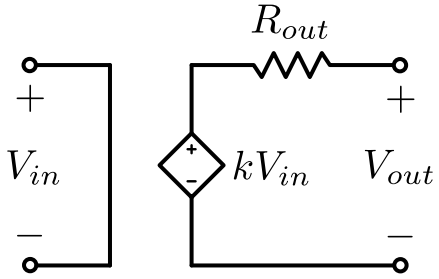


Figure 2.6: Level shifter and gate driver Verilog-A circuit equivalent model.

The model of the gate driver is a real *Voltage-Controlled Voltage Source* (VCVS), i.e. a real buffer. The non-zero series output resistance ensures that the voltage at the output will not follow instantaneously the input, if the load has a capacitive component. Since the load is the gate of the power n-MOSFET (or p-MOSFET), which is purely capacitive, the model is accurate and paper and pencil calculations

for gate delay and driving current can be verified. Moreover some headroom to the voltage swing is included to model a non rail-to-rail behavior.

The parameters of the model are the input maximum voltage ($V_{MAX}^{(in)}$), the output drop voltage (V_{drop}) and the maximum output current (I_{MAX}). The conversion gain k is calculated as:

$$k = (V_{sup} - 2V_{drop})/V_{MAX}^{(in)} \tag{2.3}$$

where V_{sup} is the supply voltage of the gate driver, i.e. the battery voltage. The output resistance is obtained as:

$$R_{out} = V_{sup}/I_{MAX} \tag{2.4}$$

so that the maximum current is limited to I_{MAX}. The output voltage will be given therefore by the series combination of the VCVS and the output resistance, as shown in Figure 2.6. In the following the Verilog-A code is reported (`temp` is the node between the VCVS and R_{out}):

```
1     V(temp,Vref) <+ drop_out + gain*V(Vin,Vref);
2     I(temp,Vout) <+ V(temp,Vout)/rout;
```

2.2 System simulations

In this section some graphs showing simulations and proper functionality of the converter are presented.

In Figure 2.7 input in-rush current during the first phase of the start-up is depicted. As expected (see Section 1.4), the current does not exceed dangerous values: the peak is at approximately 370 mA, thus it can be safely neglected and further protection circuitry is not needed.

In Figure 2.8 the improvement due to pulse-skipping function in terms of efficiency is reported. It is relevant, especially at very light load: when the output current is 1 mA an almost 4% improvement is achieved, but at 0.5 mA it is even higher, more than 7%.

A transient simulation is shown in Figure 2.9: output voltage (V_{out}), error amplifier output (V_{ea}), load current (I_{load}) and inductor current (I_L) are plotted in the time domain. The converter is subject to a train of output current high frequency pulses, whose width is 200 µs. As can be seen from both V_{out} and V_{ea}, the system is stable and regulates the output voltage successfully around 20 V. Looking at the inductor current, it is evident the pulse-skipping function at light load. Also, the output voltage ripple is approximately 100 mV at the highest load, as required from specs.

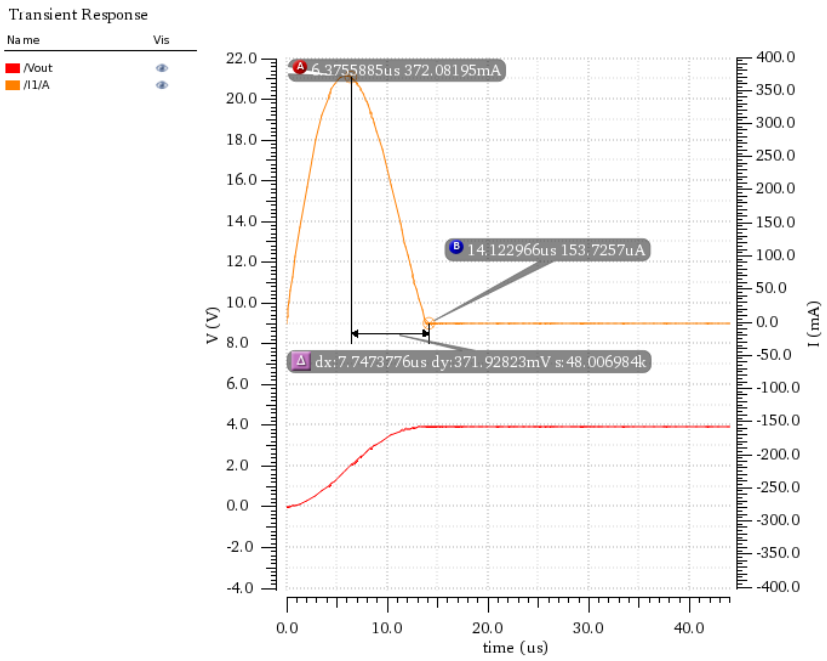


Figure 2.7: Input in-rush current during the first phase of the start-up.

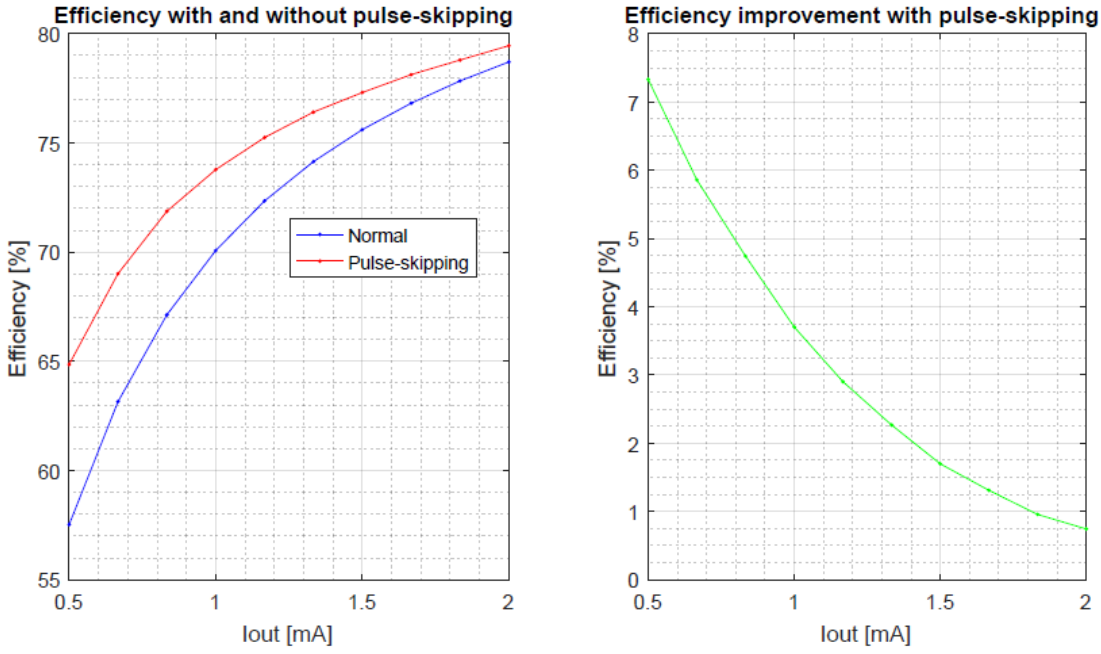


Figure 2.8: Improvement in efficiency due to pulse-skipping function.

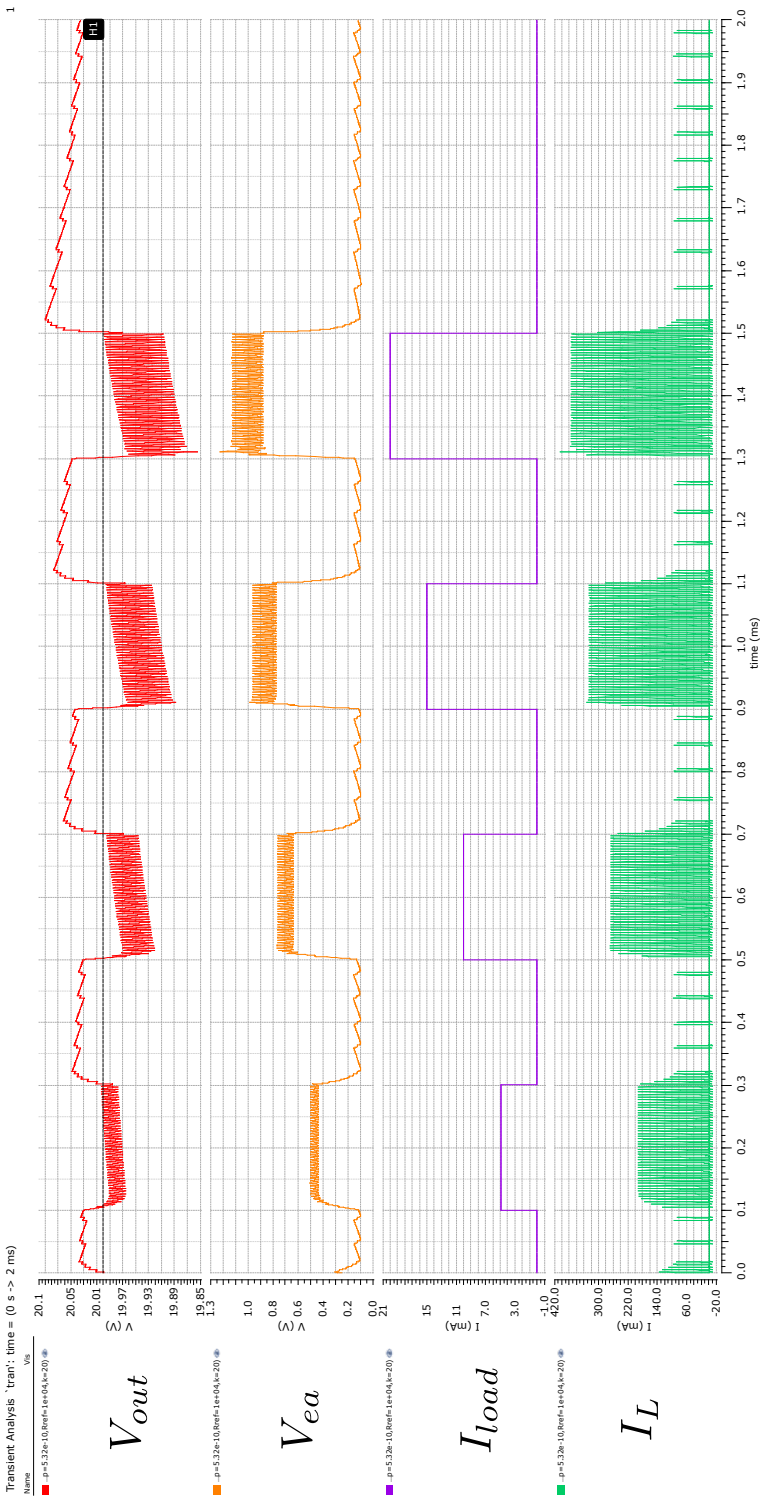


Figure 2.9: Transient simulation.

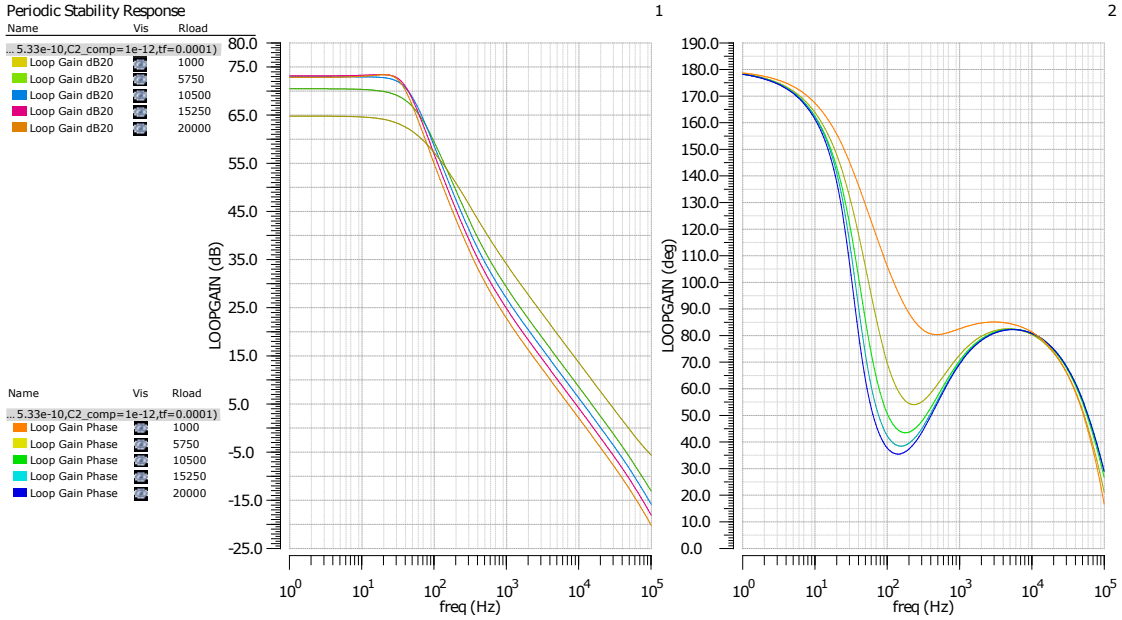


Figure 2.10: Stability plots with parameterized output resistance.

In Figure 2.10 stability plots with parameterized output resistance are finally reported: the frequency response of the closed-loop system behaves as expected. The crossover in fact decreases as the output resistance increases, or, equivalently, as the output current diminishes (see Section 1.3).

Chapter 3

Transistor-level design

In this chapter, each block of the control loop, simulated in Verilog-A, has been translated into an equivalent transistor-level schematic. The design is *full-custom*, i.e. every transistor has been dimensioned on the basis of the given or extracted requirements. Throughout the whole chapter simulations are carried out to prove the correctness of the design and the achieved matching with the respective HDL module. As a good trade-off between area and performances (to avoid short channel effects) the length of every transistor has been usually set to minimum 1 µm, unless specific goals needed to be pursued. In Table 3.1 typical main parameters of the process are listed and they are used for paper-and-pencil computations.

N-type		P-type	
V_{TH_n}	0.37 V	V_{TH_p}	−0.44 V
K_n	300 µA/V^2	K_p	70 µA/V^2
$2\phi_f$	0.65 V	$2\phi_f$	0.65 V
γ_n	0.22 V$^{1/2}$	γ_p	0.25 V$^{1/2}$

Table 3.1: Process typical parameters for 1.8 V devices.

3.1 Current sensor

As previously described (see Section 1.1), the best branch to sense the peak current is between the power transistor and the reference node, because there the common mode voltage is fixed during every working phase.

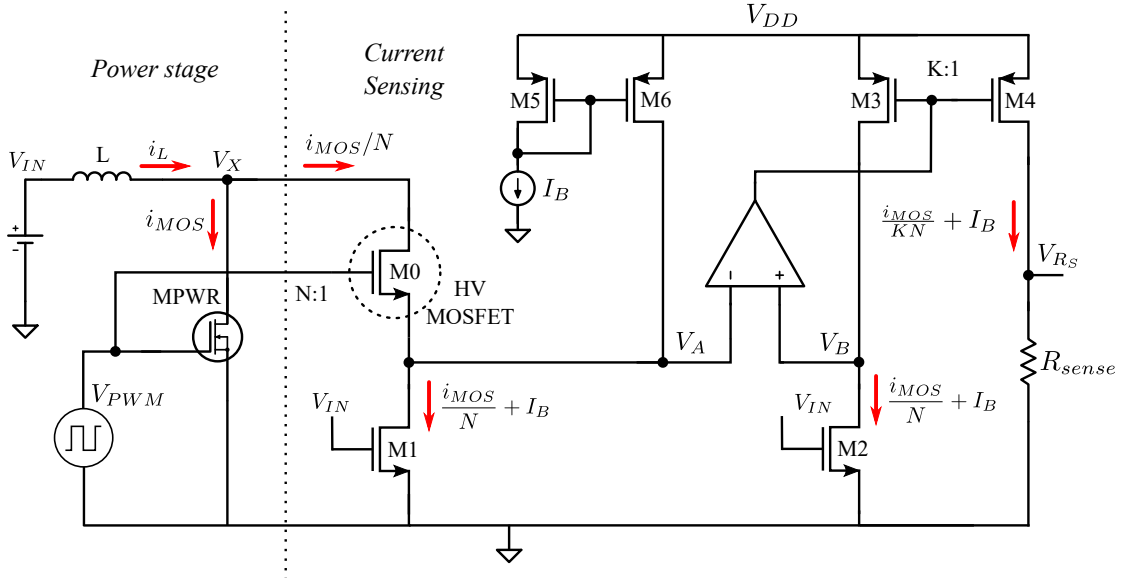
Many current-sensing methods have been presented in literature: the most straightforward way is to put a sensing resistor in series to the power transistor, with the drawback of power efficiency reduction. Typically the power loss in efficiency due to this resistor should be less than some percentage points, leading

to a very small resistor, in the order of $10\,\mathrm{m\Omega} \div 100\,\mathrm{m\Omega}$. This method is easy to implement in discrete components converters, but would be tougher in integrated ones because it is quite difficult to realize precise small resistors able to handle high currents. Another popular method is to use a current-sensing transformer [33], yielding better performances in terms of efficiency. However, this is not an appropriate solution for the converter object of this work, because of the constraint of reduced size, cost and weight: another magnetic component in the circuit should be in fact avoided. Focusing on fully integrated solutions only, several techniques have been proposed. In [34] instead of inserting a series shunt resistor, the on-resistance of the power MOSFET is used to sense the current: the advantage is that no further power losses are added, at the price of a lower accuracy. Indeed the R_{on} of the MOSFET depends on temperature and cannot be controlled precisely. Moreover, the voltage across it during the off period swings a lot, from 0 V to 20 V, possibly exceeding sensing circuitry maximum ratings. A sensorless method is proposed in [35]: it is based on the voltage-current relationship of an inductor, i.e. the current is the integral over time of the voltage multiplied by the inductance value. By knowing the input voltage and the duty cycle the peak current can be easily derived. Although this technique is completely lossless, it is quite complex to implement and the value of the inductance is assumed to be known exactly, a rather unrealistic supposition. Finally, a quite popular technique [36][37][38] and very attractive for the purpose of this work, is to insert a sensing MOSFET in parallel to the main power transistor, with a size ratio of the order 1:100 to 1:1000. The R_{on} of the sensing MOSFET will be therefore much higher than the power one, leading to low and controllable power losses, and the current will be scaled down and sensed precisely, supposing to have well-matched devices. This technique has been adopted because it is fully integrated, quite easy to design, power efficient (losses can be less than 1 mW at full load) and exhibits a good accuracy.

The schematic of the current-sensing circuit is shown in Figure 3.1.

Intuitive analysis

MPWR is the main power MOSFET, while M1 is the parallel sensing one. M0 is an HV transistor, whose purpose is to keep maximum ratings at node V_A safe and to connect the sensing circuitry during the useful period only, i.e. when MPWR is on. The gate of M0 is therefore directly connected to the gate of MPWR, they need to be synchronously switched on and off. Since the voltage at node V_X is low for efficiency requirements, M1 will operate in triode region and can be simplified as a resistor for an intuitive approach. In order to obtain a voltage which is proportional to the current flowing through MPWR (that is equivalent to say through M1, since $i_{M1} = i_{MPWR}/N$), the drain current of M1 should be



M0	90/1.8
M1	16/2
M2	16/2
M3	60/1.5
M4	30/1.5
M5	4/1
M6	4/1
R_{sense}	2.7 kΩ
I_B	5 µA

All transistors dimensions are in $\mu m/\mu m$.

Figure 3.1: Current sensing circuit schematic.

somehow mirrored and then a voltage can be obtained applying such a current on a resistor. M1 and M2 form the aforementioned current mirror. Unfortunately, a conventional topology cannot be used, because the drain current in triode region depends strongly on the drain-source voltage. Using a long channel transistor approximation the current can be expressed as:

$$I_D = \mu_n C_{OX} \left(\frac{W}{L}\right) \left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{3.1}$$

According to equation 3.1, the drain currents of M1 and M2 are equal if and only if both the gate-source and the drain-source voltages are the same. $V_{GS_{M1}} = V_{GS_{M2}}$ can be easily satisfied applying the same voltages on the two gates, namely V_{IN}. $V_{DS_{M1}} = V_{DS_{M2}}$ requires on the contrary a more complex circuitry: a high gain amplifier can be exploited in a negative feedback configuration to enforce the drain voltages to be equal. Specifically, the output of the amplifier is connected to the gate of M3, thus it regulates the current flowing through M3 and consequently

also M2. Assuming to have a high loop gain, the voltage V_B follows V_A, so $i_{D_{M2}} = i_{D_{M1}} = i_{D_{M3}}$. The current through M3 can be further mirrored by M4 and applied to R_S to obtain V_{R_S}. Notice that this last mirror can be a conventional one, because M3 and M4 operate in saturation region. Transistor M5 and M6 are added to provide a small bias current through M1, ensuring that V_A does not become negative during T_{off}, protecting the input stage of the amplifier. Nevertheless, this introduces an offset in the output current and thus on V_{R_S}, leading to a systematic error. However, since I_B is much smaller than i_{MOS}/N, the error will be very small compared to the useful signal. Moreover, and more importantly, the high DC gain of the compensator in the control loop adjusts for any DC offset introduced: this error can be therefore safely neglected.

Design

A good trade-off between accuracy and power consumption needs first to be chosen. In fact, the higher is $i_{D_{M1}}$ the more precise is the mirrored current, because the signal is bigger in amplitude; but at the same time the higher is the power consumed by the sensing circuitry. As a reasonable starting point, the overall power consumption has been set to be lower than 1 mW at full load, namely $I_{PK} \approx 0.5A$, so that efficiency will be reduced by approximately 0.25%.

Firstly, notice that the critical branch for power consumption is the series of M2 and M3, because there both current and voltage are the highest, respectively $\frac{i_{MOS}}{N} + I_B$ and V_{DD}. Since the latter is fixed, the mirroring factor N is the degree of freedom. The R_S parameter on the other hand should be set to $2\,\Omega$ (see Table 1.2). The design formulas linking dimensions with power consumption are the following:

$$P_{M1} = \frac{(I_{PK})^2/R_{DS_{on}}}{N}\,\frac{D_{MAX}}{3} \tag{3.2}$$

$$P_{M2+M3} = \frac{1}{2}\,\frac{I_{PK}V_{DD}D_{MAX}}{N} \tag{3.3}$$

$$P_{M4} = \frac{1}{2}\,\frac{I_{PK}V_{DD}D_{MAX}}{KN} \tag{3.4}$$

With fixed quantities $I_{PK} = 0.5\,\mathrm{A}$, $V_{DD} = 1.8\,\mathrm{V}$ and $D_{MAX} = 0.75$, by assuming that half of the power is consumed by the series of M2 and M3, i.e. $500\,\mu\mathrm{W}$, the mirroring ratio can be obtained by inverting Eq. 3.3:

$$N = \frac{1}{2}\,\frac{I_{PK}V_{DD}D_{MAX}}{P_{M2+M3}} = \frac{0.5\,\mathrm{A} \times 1.8\,\mathrm{V} \times 0.75}{2 \times 0.5\,\mathrm{mW}} = 675$$

By knowing that R_{on} of MPWR is $0.925\,\Omega$, the on-resistance of M1 should be then 675 times $R_{DS_{on}}$, i.e. $\approx 625\,\Omega$. Using 5V devices, this is translated in a form factor of 8. In order to have a precise ratio, the length of M2 and M3 is set to $2\,\mu$m, leading to $(W/L)_{M2} = (W/L)_{M3} = (16\,\mu\text{m}/2\,\mu\text{m})$. By substitution in Eq. 3.2 the power consumed by M1 will be:

$$P_{M1} = \frac{(0.5\,\text{A})^2/(0.925\,\Omega)}{675}\,\frac{0.75}{3} = 100\,\mu\text{W}$$

By choosing K=2:

$$P_{M4} = P_{M2+M3}/K = 250\,\mu\text{W}$$

The overall power consumption is thus $850\,\mu$W: lower than 1 mW, as desired.

In order to guarantee that the R_S factor is $2\,\Omega$, the value of the resistance R_{sense} must be designed. The absolute maximum values, according to Subsection 1.5.2, should be imposed: when $I_{PK} = 0.6\,\text{A}$ the voltage at the input of the comparator must be 1.2 V. This is translated in a proper value of R_{sense}, namely:

$$V_{R_S} = R_{sense} I_{sense} \Rightarrow R_{sense} = \frac{K N V_{R_S}}{I_{PK}} = \frac{2 \times 675 \times 1.2\,\text{V}}{0.6\,\text{A}} = 2.7\,\text{k}\Omega$$

Finally the aspect ratio of transistors M3 and M4 should be defined. The latter can be obtained imposing the constraint that it must operate in saturation region, a necessary requirement for the correct current mirroring. In other terms the drain-source voltage of M4 must be greater than the overdrive in the worst condition, that is when the current is maximum (thus the overdrive) and, consequently, the drain-source voltage is minimum, because it is given by Ohm's law on R_{sense}. Expressing it with equations:

$$V_{DS_4} > V_{OD_4} = \frac{I_{D4}}{K_n (W/L)_4}$$

$$\Rightarrow \left(\frac{W}{L}\right)_4 > \frac{I_{D4}}{K_n V_{OD_4}^2} = \frac{444\,\mu\text{A}}{70\,\mu\text{A/V}^2 \times (1.8\,\text{V} - 1.2\,\text{V})^2} = 17.6$$

A bigger value should be chosen to be more conservative, for instance 20. Also, longer devices are used to improve current matching both in terms of geometrical errors and output resistance. The final aspect ratios are the following:

$$\left(\frac{W}{L}\right)_4 = \frac{30\,\mu\text{m}}{1.5\,\mu\text{m}} \quad , \quad \left(\frac{W}{L}\right)_3 = 2\left(\frac{W}{L}\right)_4 = \frac{60\,\mu\text{m}}{1.5\,\mu\text{m}}$$

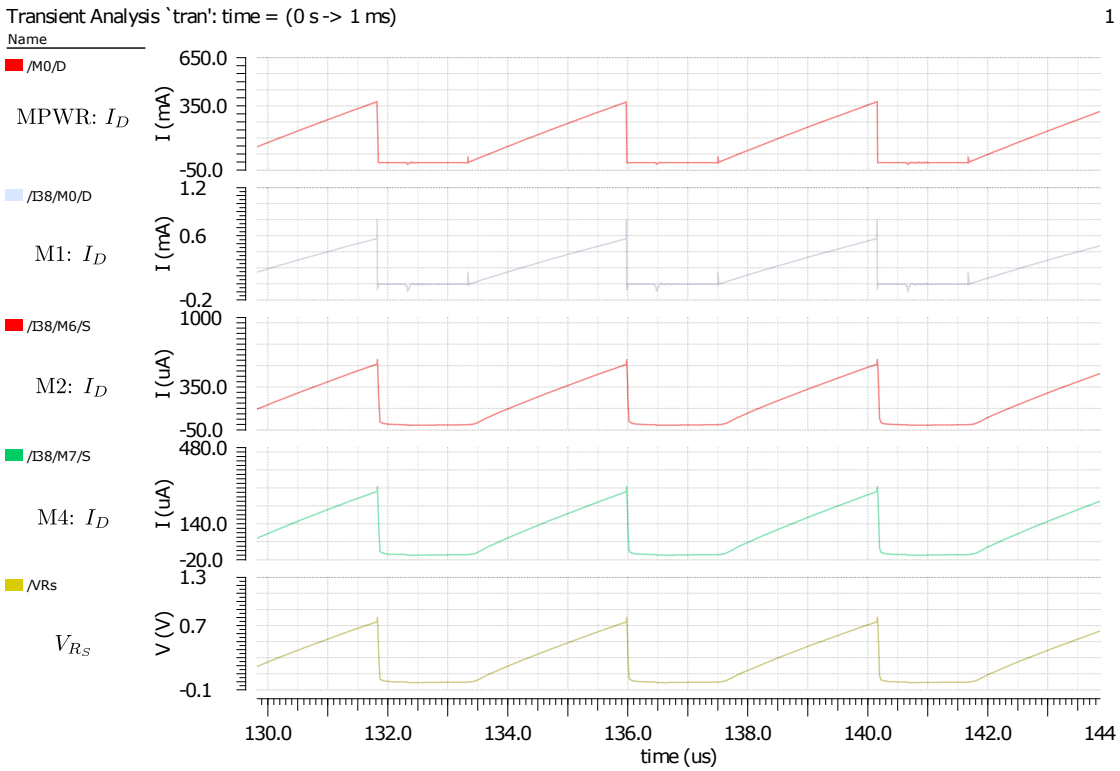


Figure 3.2: Transient waveforms of the current sensing circuitry.

The circuit has been simulated using an almost ideal Verilog-A described op-amp (very high bandwidth and gain), to verify overall functionality before its design. In Figure 3.2 transient waveforms are shown and measurements have been extracted from them. For the sake of clearness they are listed in the following: $I_{PK} = 372\,\text{mA}$, $I_{D1} = 559\,\mu\text{A}$, $I_{D3} = 561.7\,\mu\text{A}$, $I_{D4} = 281.3\,\mu\text{A}$ and $V_{R_S} = 757.3\,\text{mV}$, which lead to $N = 665$, $K = 1.996$ and $R_S = 2.033\,\Omega$. Paper-and-pencil design is therefore verified.

The op-amp described in Verilog-A needs to be translated finally into an equivalent transistor-level schematic. However, prior simulations of the Verilog-A module have been carried out to extract requirements to be imposed on the op-amp, such as minimum gain, minimum gain-bandwidth product, load capacitance and slew rate. Specifications are:

- $CMIR = [0\,\text{V}, 0.6\,\text{V}]$, because the voltage at the drain of the power MOSFET does not exceed $V_x = I_{PK} R_{DS_{on}} = 0.6\,\text{A} \times 0.925\,\Omega = 0.555\,\text{V}$;
- $V_{DD} = 1.8\,\text{V}$;
- $G_{DC} > 3000$;
- $\text{SR} > 1\,\text{V}/\mu\text{s}$;
- $\text{GBW} > 10\,\text{MHz}$;
- $C_L \approx 1\,\text{pF}$, obtained in ADE L environment, as the parallel of the gate capacitances of M3 and M4, respectively 417 fF and 210 fF (a bigger value is used for a more conservative phase margin);
- $OR = [1\,\text{V}, 1.5\,\text{V}]$, to be able to drive M3 and M4 from off state to the overdrive required to generate the output current.

Since particular performances are not required, a classical two-stages op-amp has been chosen for its simplicity and the available documentation. A p-type stage should be used because of CMIR requirements, to-rail at the low side while well below the rail at the high side. The schematic of the module is shown in Figure 3.3 and the design procedure is well illustrated in Allen and Holberg [39]. Process parameters are listed at the beginning of this chapter, in Table 3.1. Design formulas, taken from [39], are listed in the following:

$$SR = I_B / C_c \tag{3.5}$$

$$A_{v1} = \frac{-g_{m1}}{g_{ds3} + g_{ds5}} = \frac{-2g_{m1}}{I_B(\lambda_3 + \lambda_5)} \tag{3.6}$$

$$A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6(\lambda_6 + \lambda_7)} \tag{3.7}$$

$$GBW = g_{m2}/2\pi C_c \tag{3.8}$$

$$f_{p2} = g_{m6}/2\pi C_L \tag{3.9}$$

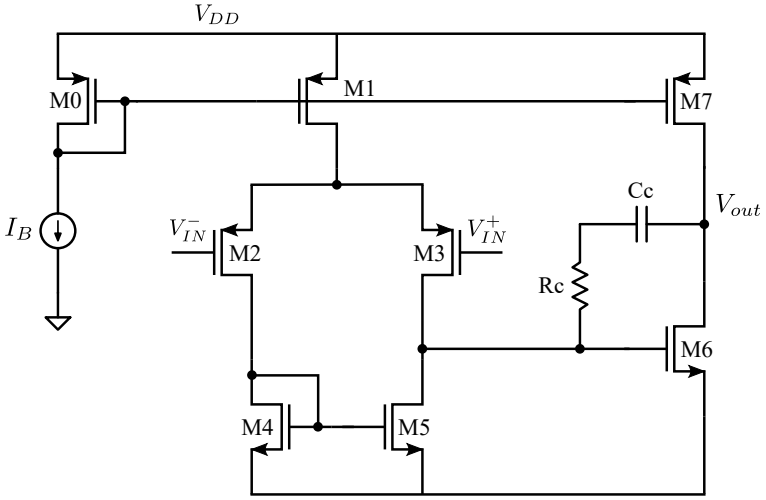
$$f_{RHPZ} = g_{m6}/2\pi C_c \tag{3.10}$$

$$CMIR^{+} = V_{DD} - |V_{TH2}| - V_{OD1} - V_{OD2} \tag{3.11}$$

$$CMIR^{-} = V_{TH4} - |V_{TH2}| + V_{OD4} \tag{3.12}$$

$$V_{ODi} = |V_{GSi}| - |V_{THi}| = \sqrt{\frac{2I_i}{K_{n,p}(W/L)_i}} \tag{3.13}$$

$$R_z = \frac{1}{g_{m6}} \frac{C_L + C_c}{C_c} \tag{3.14}$$



M0	3/1
M1	6/2
M2	3/1
M3	3/1
M4	3/1
M5	3/1
M6	13/1
M7	6.15/1
Rc	8.5 kΩ
Cc	400 fF

All transistors dimensions are in $\mu m/\mu m$.

Figure 3.3: Two stages op-amp, used in the current sensing circuit.

The first step is the choice of a proper value of the compensating capacitance C_C in order to have a sufficiently large phase margin. If $f_{p2} = 2.2\,GBW$, by assuming

that $f_{RHPZ} \approx 10\,GBW$, the phase margin will be 60°. With substitution in Eq. 3.8 and 3.9, the value of the compensation capacitance can be derived:

$$C_c > \frac{2.2}{10}\,C_L = \frac{2.2 \times 1\,\text{pF}}{10} = 220\,\text{fF}$$

A value $C_c = 400\,\text{fF}$ has been selected in order to have a higher phase margin. Then the slew rate specification should be imposed to obtain the minimum amplitude of the bias current:

$$I_B > SR\ C_c = 1\,\text{V}/\mu\text{s} \times 400\,\text{fF} = 0.4\,\mu\text{A}$$

The resulting bias current is very small: it cannot provide correct operation for the transistors, because they would be biased in weak inversion, not in saturation. Thus, a bigger current has been selected, namely $I_B = 10\,\mu\text{A}$, providing a correct bias and transient response with a reasonably low power consumption. The aspect ratio of M3 can be determined now by using the requirement for negative input common-mode range. However, M2 suffers from body effect, thus the threshold voltage should be computed more accurately:

$$|V_{TH2}| = |V_{TH_p}| + \gamma_p(\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}) \approx$$
$$\approx 0.44\,\text{V} + 0.25\,\text{V}^{1/2} \times (\sqrt{0.65\,\text{V} + 1.5\,\text{V}} - \sqrt{0.65\,\text{V}}) = 0.605\,\text{V}$$

By substitution in Eq. 3.12:

$$\left(\frac{W}{L}\right)_4 > \frac{2I_4}{K_n(V_{TH2} - V_{TH4})} = \frac{10\,\mu\text{A}}{300\,\mu\text{A}/\text{V}^2 \times (0.605\,\text{V} - 0.37\,\text{V}^2)} = 0.6$$

A choice was made to use a bigger ratio, i.e. $(W/L)_{4,5} = (3\,\mu\text{m}/1\,\mu\text{m})$, in order to improve matching, due to the fact that a bigger device means a smaller geometrical error. The input transconductance can be derived from Eq. 3.8:

$$g_{m2,3} > 2\pi C_c\ GBW = 2\pi \times 400\,\text{fF} \times 10\,\text{MHz} = 25.1\,\mu\text{S}$$

To be more conservative, a bigger value $g_{m2,3} = 40\,\mu\text{S}$ was selected. The aspect ratio of M2 and M3 can be derived now:

$$\left(\frac{W}{L}\right)_{2,3} > \frac{g_{m2,3}^2}{2K_pI_{3,4}} = \frac{(40\,\mu\text{S})^2}{2 \times 70\,\mu\text{A}/\text{V}^2 \times 5\,\mu\text{A}} = 2.28$$

thus $(W/L)_{2,3} = (3\,\mu\text{m}/1\,\mu\text{m})$. The form factor of M1 can be obtained by reversing Eq. 3.11 (neglecting body effect, reasonable because $V_{BS} = V_{OD1}$ is small):

$$\left(\frac{W}{L}\right)_1 > \frac{2I_1}{K_p\left(V_{DD} - |V_{TH2}| - CMIR^+ - \sqrt{\frac{2I_2}{K_p(\frac{W}{L})_2}}\right)^2} = \frac{10\,\mu\text{A}}{70\,\mu\text{A/V}^2 \times \left(1.8\,\text{V} - 0.44\,\text{V} - 0.6\,\text{V} - \sqrt{\frac{10\,\mu\text{A}}{70\,\mu\text{A/V}^2 \times 3}}\right)^2} = 0.97$$

A value of 3 was chosen to decrease geometrical errors. The length has been increased as well to 2 µm to improve current matching, thanks to the higher output resistance of M1. The overall dimensions are thus $(W/L)_1 = (6\,\mu\text{m}/2\,\mu\text{m})$. Now the design of the first stage is complete and the output stage is next considered. The transconductance of M6 can be derived according to the initial assumption that the second pole is at least at a frequency ten times higher than the gain-bandwidth product. The relationship is the following:

$$g_{m6} > 2.2\,g_{m2}\frac{C_L}{C_c} = \frac{2.2 \times 40\,\mu\text{S} \times 1\,\text{pF}}{400\,\text{fF}} = 220\,\mu\text{S}$$

A value $g_{m6} = 400\,\mu\text{S}$ was selected to be more conservative and to enhance load driving capability. Knowing that $g_{m4} = \sqrt{2K_n(W/L)_4 I_4} \approx 95\,\mu\text{S}$, by imposing $V_{GS5} = V_{GS6}$ for the systematic offset compensation:

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_5 \frac{g_{m6}}{g_{m4}} = 3 \times \frac{400\,\mu\text{S}}{95\,\mu\text{S}} = 12.6$$

thus $(W/L)_6 = 13$. The current through M6 will be:

$$I_6 = \frac{(g_{m6})^2}{2K_n(W/L)_6} = \frac{(400\,\mu\text{S})^2}{2 \times 300\,\mu\text{A/V}^2 \times 13} \approx 20.5\,\mu\text{A}$$

The form factor of M7 should then defined to have the correct current mirroring, i.e.:

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_1 \frac{I_7}{I_1} = 3 \times \frac{20.5\,\mu\text{A}}{10\,\mu\text{A}} = 6.15$$

In order to move the feedforward zero from the RHP to the LHP and place it on top of the second pole, a resistor R_z can be inserted in series to C_c. The value of the resistance is, by substitution in Eq. 3.14:

$$R_z = \frac{1}{400\,\mu\text{S}} \times \frac{1.4\,\text{pF}}{0.4\,\text{pF}} = 8.75\,\text{k}\Omega$$

Regarding the output voltage swing, the constraint is verified since transistors

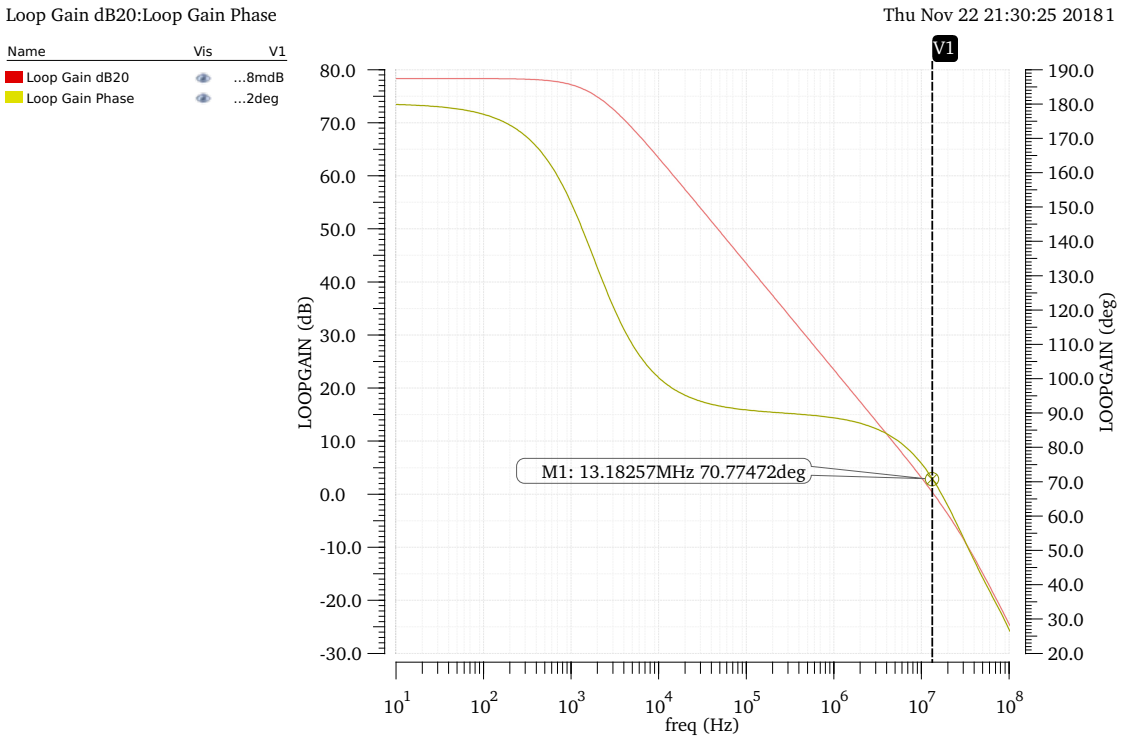


Figure 3.4: Stability analysis of the op-amp used in the current sensing circuit.

M6 and M7 are certainly in saturation within that range. Requirement on gain is instead verified by simulations (see Figure 3.4).

A transient simulation has been carried out again with the transistor-level block, confirming proper functionality. Waveforms are shown in Fig. 3.5.

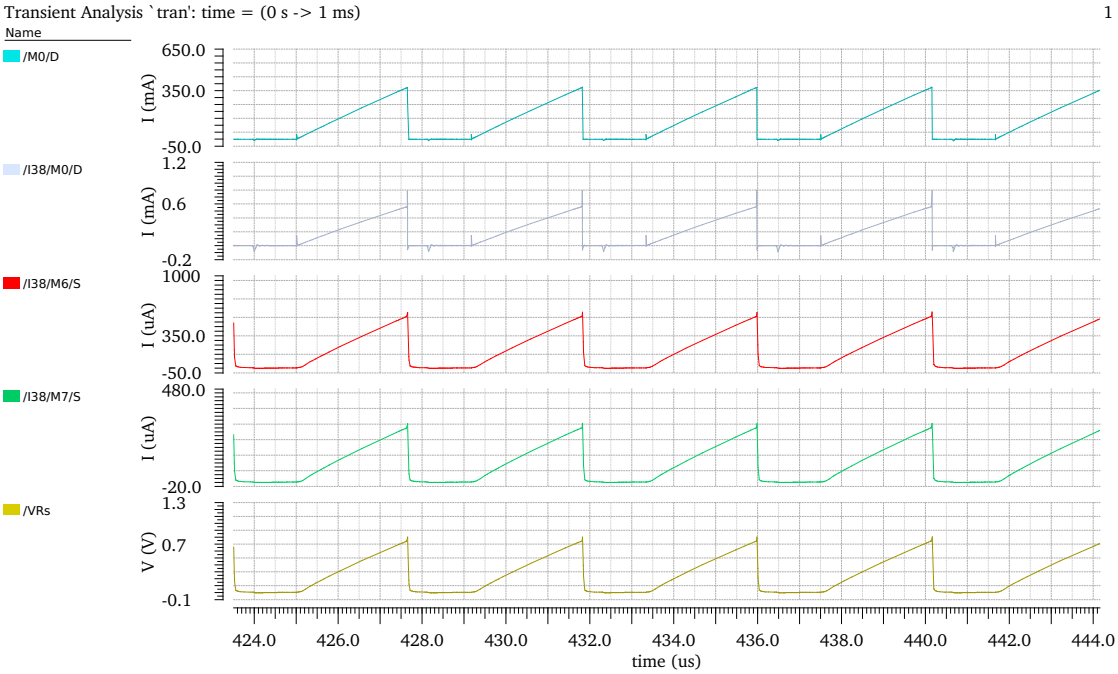


Figure 3.5: Transient waveforms of the current sensing circuit, with whole transistor-level design.

3.2 Compensator

The required transfer function for the compensator is shown in Figure 1.10. The classical implementing circuit is depicted in Figure 3.6 [11][10], whose transfer function is:

$$H(s) = \frac{V_{ea}(s)}{V_{out}(s)} = -\frac{1 + sR_2C_1}{sR_1(C_1 + C_2)[1 + s\frac{R_2C_1C_2}{C_1+C_2}]} \tag{3.15}$$

By assuming $C_2 << C_1$ (correct, because $f_z = 442\,\text{Hz} << f_{p2} = 150\,\text{kHz}$ and f_z is related to C_1 while f_{p2} to C_1, see Table 1.3), Eq. 3.15 can be approximated as:

$$H(s) \approx -\frac{1 + sR_2C_1}{sR_1C_1(1 + sR_2C_2)} \tag{3.16}$$

It has therefore a pole in the origin, a zero at:

$$f_z = \frac{1}{2\pi R_2C_1} \tag{3.17}$$

a pole at:

$$f_{p2} = \frac{1}{2\pi R_2 C_2} \tag{3.18}$$

and a constant gain between the zero and the pole of:

$$G_{comp} = -\frac{R_2}{R_1} \tag{3.19}$$

The resistor R_{DC} is placed just to scale down the output voltage with a partition with R_1, so that it can be sensed within the low voltage supply range, i.e. 1.8 V. Hence:

$$R_{DC} = R_1 \, \frac{V_{REF}/V_{OUT}}{1 - V_{REF}/V_{OUT}} \tag{3.20}$$

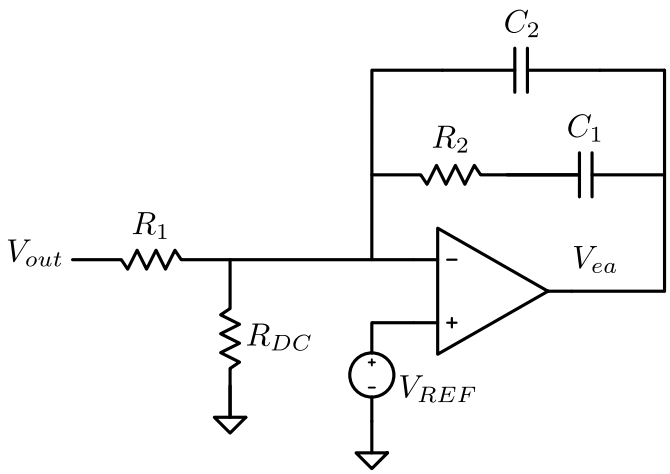


Figure 3.6: Schematic of a standard type 2 compensator.

R_{DC} has no effect on the transfer function: virtual short circuit holds, thus the negative input of the op-amp is at ground in small-signal analysis. Since we have four equations but five variables in the design, a degree of freedom is present. The goal is to have not too big and not too small resistances, because of noise or gain issues and power consumption respectively, and not too big capacitances, in order not to consume a lot of area on the die. Special care should be taken for the value of the series of R_1 and R_{DC} because it contributes to a relevant DC power consumption (see Table 1.2, R_{FB}). By choosing $C_2 = 1.5\,\text{pF}$, the parameters listed in Table 3.2 are obtained. Notice that the ratio of the resistances R_1 and R_{DC} is

very important because it sets the average output voltage of the boost converter. Thus, they need to be well-matched in the layout of the chip.

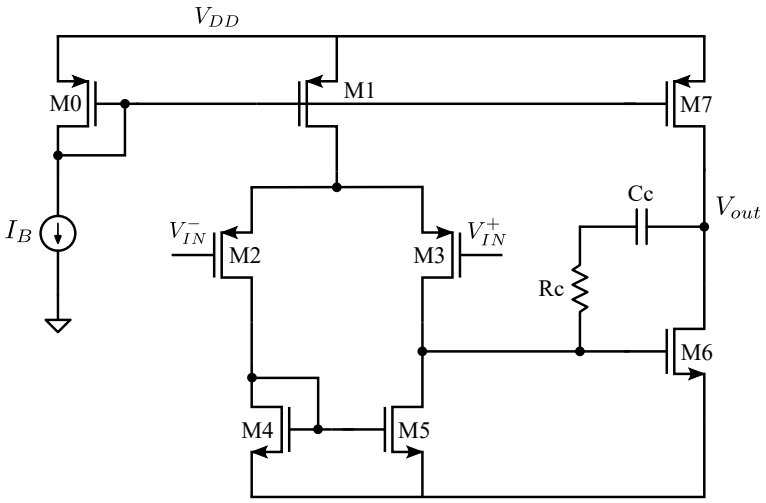
C_1	533 pF
C_2	1.5 pF
R_1	170 kΩ
R_2	707 kΩ
R_{DC}	9 kΩ

Table 3.2: Parameters of the compensation circuit (Figure 3.6).

The op-amp used as error amplifier is a classical two-stages op-amp. Requirements of such an amplifier are listed in the following (some of them have been obtained by parametric simulations on a Verilog-A block):

- $CMIR = 0\,\text{V} \div 1.1\,\text{V}$, because $V_{REF} = 1\,\text{V}$ in steady-state but the start-up phase has to be accounted;
- $G_{DC} > 5000$;
- $SR > 5\,\text{V}/\mu\text{s}$;
- $GBW > 20\,\text{MHz}$, in order not to introduce a further pole in the compensator transfer function, which would erode the phase margin;
- $C_L = 2\,\text{pF}$;
- rail-to-rail output range.

The design procedure has been already described in Section 3.1 and it is not reported again for the sake of brevity. The resulting schematic with the related dimensions of transistors and components is represented in Figure 3.7. A p-type stage is adopted because the CMIR^- is towards the bottom rail. Stability analysis results can be seen in Figure 3.8: the phase margin is 60° at 24 MHz.



M0	10/1
M1	10/1
M2	40/1
M3	40/1
M4	5/1
M5	5/1
M6	86/1
M7	44/1
Rc	3.3 kΩ
Cc	0.5 pF
I_B	10 µA

All transistors dimensions are in $\mu m/\mu m$.

Figure 3.7: Error amplifier schematic.

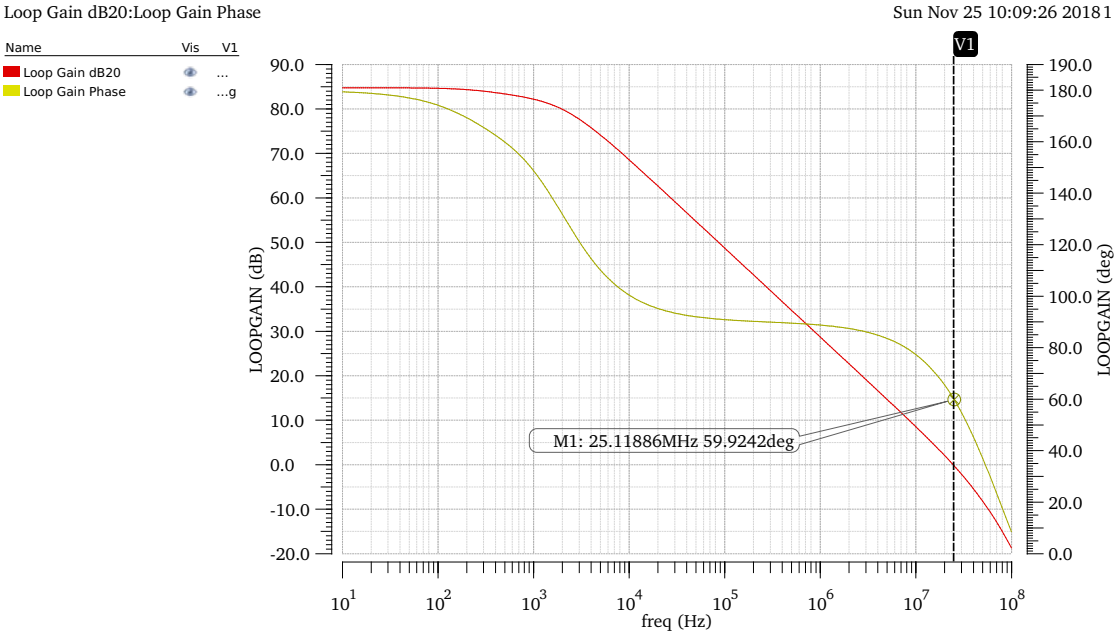


Figure 3.8: Error amplifier stability analysis.

The designed circuit is functional and simple, but has a critical drawback: the capacitance C_1 is very big, thus its on-chip integration is a problem. To solve the issue, capacitance multiplication techniques can be adopted.

Generally speaking, they can be subdivided in two main categories [40], namely *voltage mode* and *curent mode*, depicted in Figures 3.9(a) and 3.9(b) respectively. The first approach is based on the Miller theorem, which proves that if a capaci-

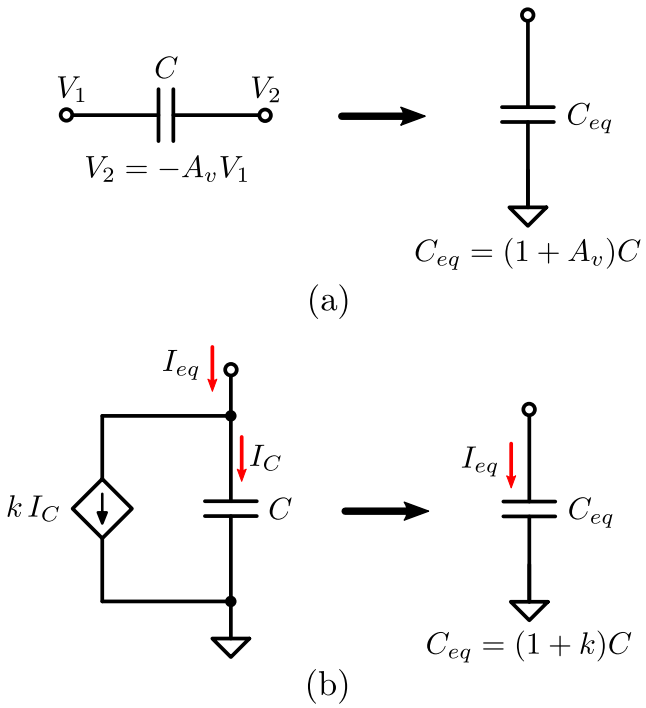


Figure 3.9: Voltage mode (a) and current mode (b) capacitance multiplication principles.

tance C is placed across an inverting amplifier circuit, whose gain is $-A_v$, at the input that capacitance looks bigger. More precisely, the equivalent capacitance is:

$$C_{eq} = (1 + A_v)C$$

Current-mode techniques are based on a sort of feedback regulating the current flowing through a capacitor. The principle is to sense somehow the current through a capacitor and subtract a fraction of it from the terminal of the capacitor itself. Or, equivalently, to sense it, amplify it and add it to the current sunk at the capacitor's terminal. Using equations, by defining the overall current entering the circuit I_{eq}, while I_C is the current effectively flowing through the capacitor C, the equivalent capacitance can be expressed as:

$$I_{eq} = C_{eq}\frac{dV_c}{dt}, \quad \frac{dV_c}{dt} = \frac{I_C}{C}, \quad I_{eq} = I_C(1 + k) \quad \Rightarrow \quad C_{eq} = (1 + k)C$$

The first method is widely used in op-amps for the compensation network but has a critical drawback: high multiplication factors may cause the amplifier to

saturate, thus gain compression. Indeed, if the input voltage swings just a little, the output of the amplifier will be obviously amplified, hence the amplitude of the input voltage which does not cause saturation is very small typically. On the contrary, current-mode techinques have not this problem, so they can be used without limitations on the input swings. However, the main drawback is that power consumption is increased a lot with high multiplication factors, because all the extra current drawn (kI_c in Figure 3.9(b)) is wasted, dissipated. But the power is AC only for the use in the compensator, thus the contribution is probably negligible, to be verified anyway with simulations. Several examples of application of the latter method are available in literature [41][42][43][44].

Nevertheless, the main difficulty in using current mode techniques in the compensator is that the current must flow through the capacitor in both directions and neither of the terminals is fixed to ground, hence most of the proposed circuits do not work. An effective solution for bidirectional multipliers is presented in [45] and has been designed successfully in this work, with some modifications.

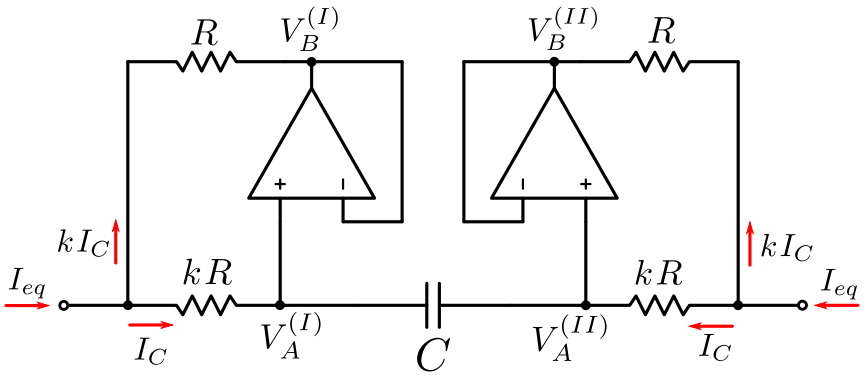
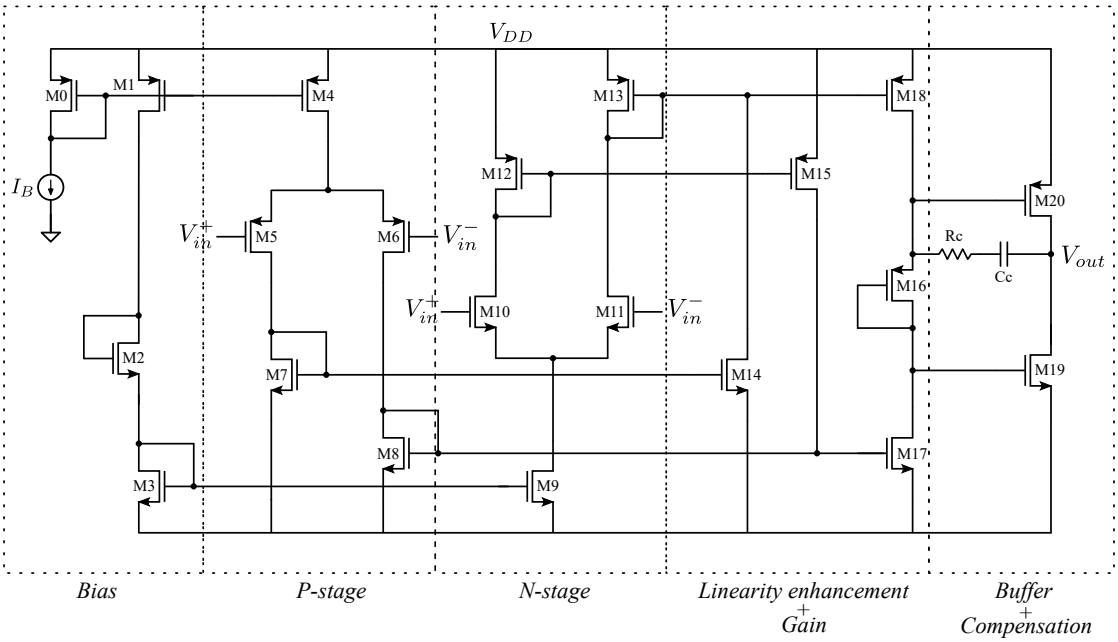


Figure 3.10: Schematic of the implementation of the capacitance multiplication technique.

In Figure 3.10 the schematic of the circuit implementation is illustrated. The current is sensed and splitted via two virtually paralleled resistors, whose resistance values are in a ratio of k. Op-amps are indeed in voltage-follower configuration, thus $V_B^{(I)} = V_A^{(I)}$ and $V_B^{(II)} = V_A^{(II)}$. By calling I_C the current flowing through the capacitor and the bigger resistances (kR), the current flowing through the smaller ones (R) is kI_C, hence $I_{eq} = (k+1)I_C$. But since I_C only flows through C, the equivalent capacitance is $C_{eq} = (1+k)C$. The presence of symmetric current splitters on both sides makes possible to use this circuit for bidirectional multipliers. In fact, the direction of the current does not matter: it is always splitted correctly. As mentioned before, the drawback of such approach is that power consumption is increased, but can be worth it (to be verified with simulations).

However, this technique is valid only if $R_{out} >> R$ and $g_m R >> 1$, where

g_m is the overall transconductance of the voltage-follower amplifier and R_{out} its output resistance. Particular care in the design of such op-amps should taken to accomplish these requirements. Moreover, rail-to-rail operation must be guaranteed because the voltage across the capacitor in the compensator circuit could vary within the whole supply range. Also, the current flowing through R (kI_C) is provided by the voltage-followers: if k is high, they should be buffered in order to be able to sink or inject it.



M0	16.4/1	M1	16.4/1	M2	16.4/1	M3	4/1
M4	16.4/1	M5	16.4/1	M6	16.4/1	M7	4/1
M8	4/1	M9	4/1	M10	4/1	M11	4/1
M12	16.4/1	M13	16.4/1	M14	4/1	M15	16.4/1
M16	1/0.5	M17	16/2	M18	64/2	M19	16/0.5
M20	64/0.5	Rc	8 kΩ	Cc	1 pF	I_B	5 µA

All transistors dimensions are in $\mu m/\mu m$.

Figure 3.11: Schematic of the voltage-follower used in the compensator with capacitance multiplier technique.

Topologically speaking, these op-amps need to be wide CMIR rail-to-rail buffered amplifiers. The schematic of the proposed amplifier is shown in Figure 3.11. Rail-to-rail CMIR is obtained using both a p- and an n- transconductance stage [31]: when the common-mode input voltage is low, the p-stage only is active, when it is high the n-stage only is on while in the middle both are operating. A second stage is inserted to improve linearity (the gain changes according to the operating region, i.e. if n-, p- or both stages are on) and to provide some gain: M17 and

M18 are in fact in a common source configuration with active load. Finally, the buffer is realized with an inverter, formed by M19 and M20. Class A or AB buffers are not suited for this application indeed, because they cannot provide rail-to-rail output. M16 has been added to dampen the cross-conduction current and the compensation is done between the output node and the drain of M18 (or M17) in order to exploit Miller effect, using a smaller capacitance (C_C). Recalling that $g_m R >> 1$, a good trade-off in the design with the size of transistors M20 and M19 has been reached with a value of the spitting resistance (R in Figure 3.10) of 8 kΩ.

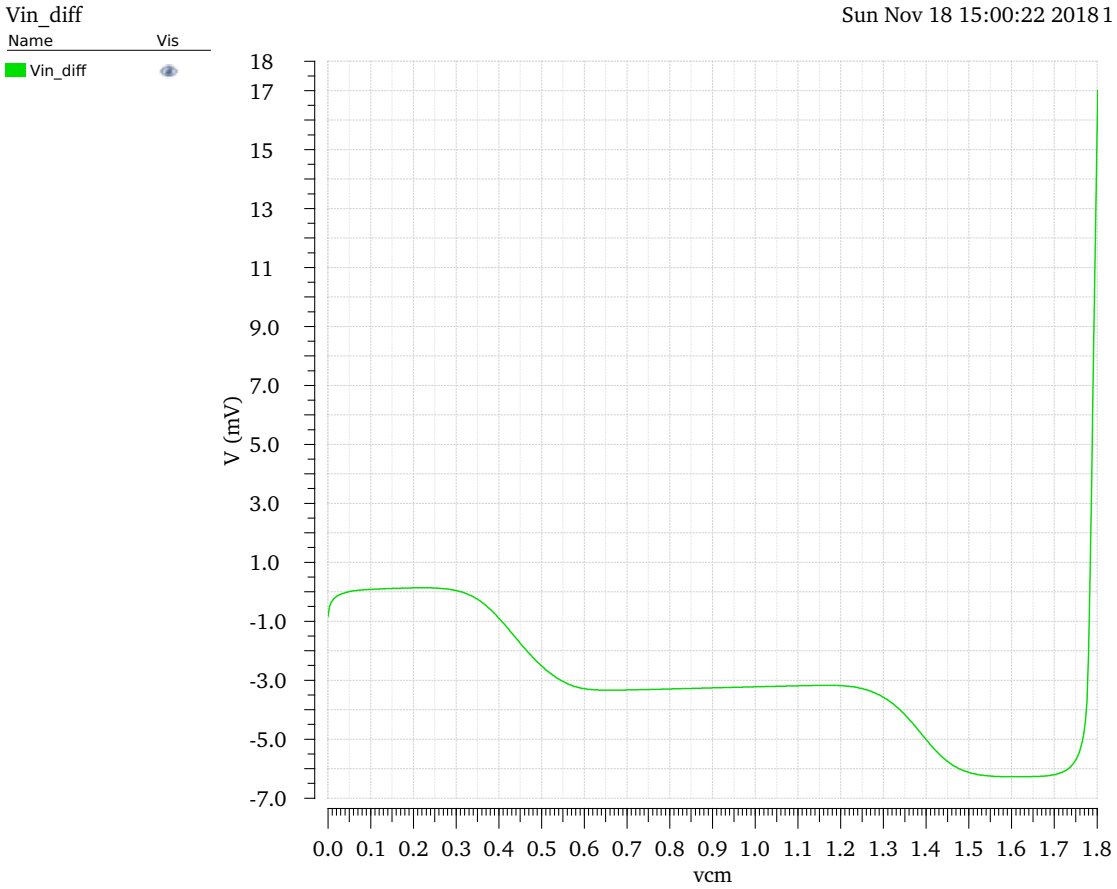


Figure 3.12: Voltage follower: differential input voltage as function of the output.

In Figure 3.12 the input differential voltage as a function of the output is plotted. The characteristic is not perfectly linear, but it is sufficient for the purpose of voltage following, since high DC gain is achieved. With voltages approaching 1.8 V the amplifier begins to have problems to drive the low resistance load (8 lΩ):

the input voltage, indeed, increases rapidly. However, this is not a problem because the gain is high anyway (more than 100). This could be solved by increasing the sizes of M19 and M20, at the price of a bigger area occupation: a trade-off has been found therefore with the proposed design.

Stability plots are shown in Figure 3.13. The crossover frequency is at approximately 25 MHz, with a phase margin of 72°.

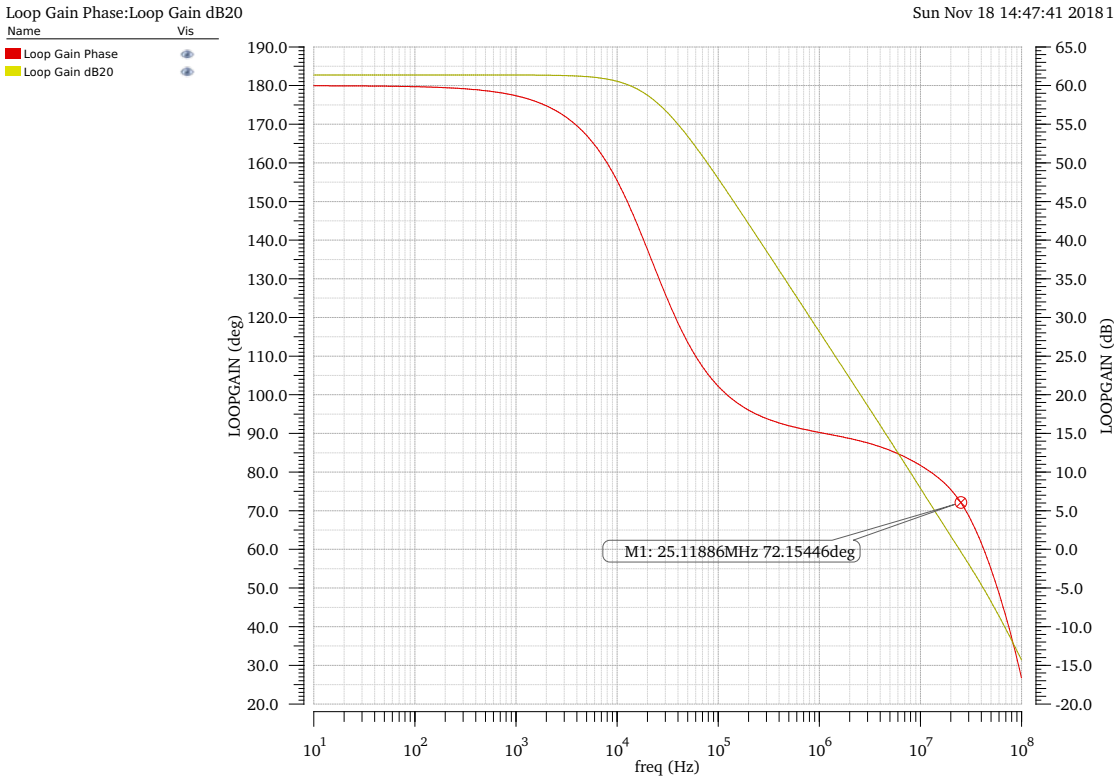


Figure 3.13: Voltage follower: stability plots.

The schematic of the whole compensator is shown in Figure 3.15, while the parameters of the various components and parameters are listed in Table 3.3. The op-amp used as error amplifier is the same of Figure 3.7: the design constraints are the same of the previous analysis indeed, the only difference is on the current sunk by the load, which is higher. However, by simulations, it has been demonstrated that it has sufficient driving capabilities.

Figure 3.14 shows that the transfer function of the two compensators, standard and with capacitance multiplier, is basically the same. In terms of closed-loop stability they are therefore equivalent. With this technique a capacitance of 11.5 pF can be used instead of a 533 pF one, enabling its integration as a result. Nevertheless, power consumption is increased, but with transient simulations a quantitative

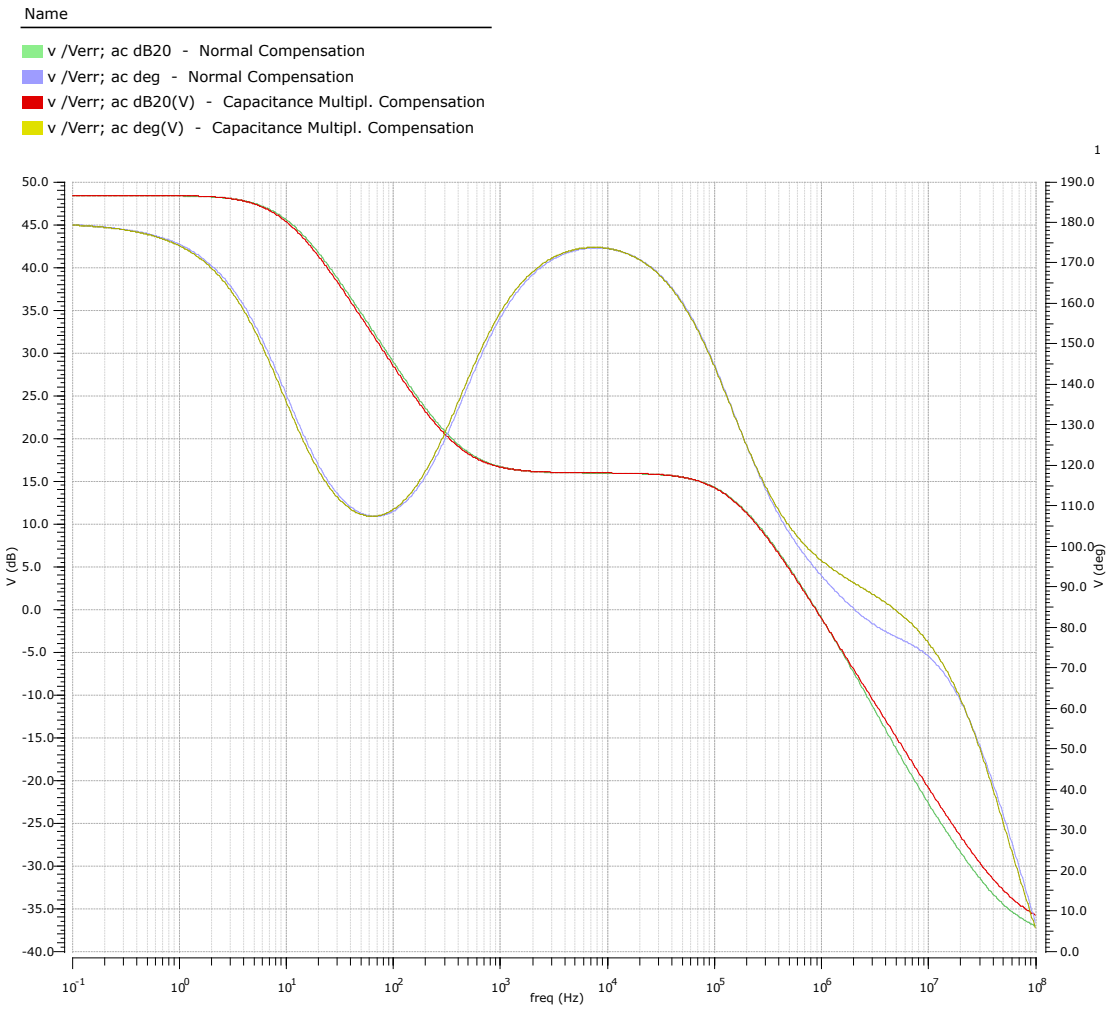


Figure 3.14: Comparison of the transfer functions of the compensators, standard and with capacitance multiplier.

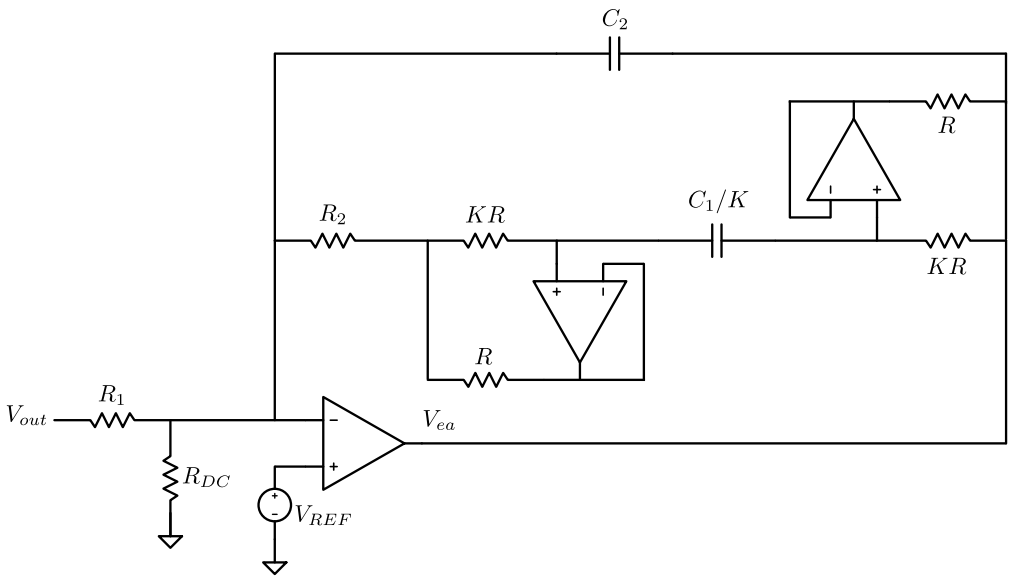


Figure 3.15: Schematic of the compensator with capacitance multiplier technique.

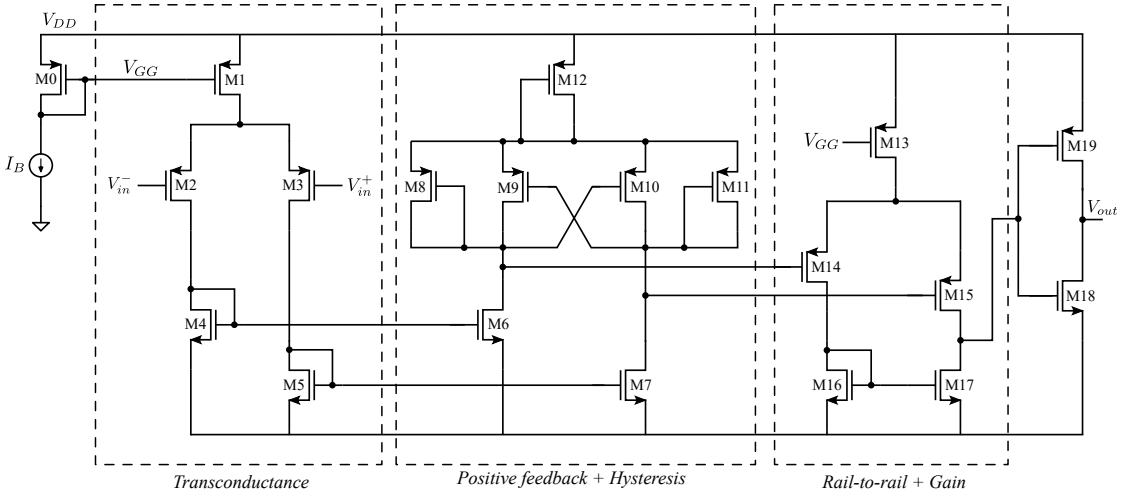
C_1	11.5 pF
C_2	1.5 pF
R_1	117.5 kΩ
R_2	740 kΩ
R_{DC}	6.15 kΩ
R	8 kΩ
k	40

Table 3.3: Parameters of the compensation circuit with capacitance multiplier (Figure 3.15).

measure has been derived and it is negligible with respect to the benefit in term of area saving. Indeed, considering the whole low-voltage control circuitry, the average power consumption with the capacitance multiplier is 720 µW, while it is 545 µW with the standard type 2 compensator.

3.3 Comparator with hysteresis

Particular performances are not required for the comparataror: it should be as fast as possible, with a reasonable power consumption, and hysteresis must be present. A simple but effective solution is well explained in Baker [31] and the design procedure is reported in the following paragraphs, for the sake of clearness. The circuit schematic is shown in Figure 3.16.



M0	15/1	M1	15/1	M2	10/1	M3	10/1	M4	2/1
M5	2/1	M6	4/1	M7	4/1	M8	2/1	M9	22/1
M10	22/1	M11	2/1	M12	10/1	M13	10/1	M14	10/1
M15	10/1	M16	3/1	M17	3/1	M18	2/1	M19	10/1

All transistors dimensions are in $\mu m/\mu m$.

Figure 3.16: Comparator with hysteresis.

The first stage is a standard transconductance differential amplifier with diode-connected active loads, whose aim is to enhance the sensitivity by amplifying the input voltage and to isolate the following decision making circuit from noise. Since the input common-mode voltage is within the range $0\,\mathrm{V} \div 1.2\,\mathrm{V}$, a p-type stage is the correct choice. As a rule of thumb, a good trade-off between speed and power consumption is reached with a bias current of $10\,\mu\mathrm{A}$. The gain of this stage is given by the ratio of the transconductances of M2 (or M3) and M4 (or M5). As already explained in Section 3.1, by imposing the requirement on CMIR$^-$ the aspect ratio of M4 can be found. Eq. 3.12 still holds:

$$\left(\frac{W}{L}\right)_4 > \frac{2I_4}{K_n(V_{TH2} - V_{TH4})} = \frac{20\,\mu\mathrm{A}}{300\,\mu\mathrm{A/V^2} \times (0.605\,\mathrm{V} - 0.37\,\mathrm{V^2})} = 1.2$$

thus $(W/L)_{4,5} = 2$. In order to have some gain, the form factor of M2 (or M3) should be rather big, but not too much otherwise the speed of the comparator is compromised by the too high input gate capacitance. However, a trade-off among trip voltages, CMIR$^+$ and power consumption needs to be found (see next formulas). Hence a unity gain has been chosen after some iterations, leading to the following results. With $(W/L)_{2,3} = 10$ a gain of approximately 1 is reached:

$$G_1 = \frac{g_{m2}}{g_{m4}} = \sqrt{\frac{K_p(W/L)_2}{K_n(W/L)_4}} = \sqrt{\frac{70\,\mu\text{A/V}^2 \times 10}{300\,\mu\text{A/V}^2 \times 2}} \approx 1.08$$

M1 should be dimensioned in order to satisfy the CMIR$^+$ constraint. A hypothesis to have a trip voltage of 100 mV has been accounted, thus $CMIR^+ = 1.1\,\text{V}$, not $CMIR^+ = 1.2\,\text{V}$. By using Eq. 3.11:

$$\left(\frac{W}{L}\right)_1 > \frac{2I_1}{K_p\left(V_{DD} - |V_{TH2}| - CMIR^+ - \sqrt{\frac{2I_2}{K_p(\frac{W}{L})_2}}\right)^2} =$$

$$= \frac{20\,\mu\text{A}}{70\,\mu\text{A/V}^2 \times \left(1.8\,\text{V} - 0.44\,\text{V} - 1.1\,\text{V} - \sqrt{\frac{10\,\mu\text{A}}{70\,\mu\text{A/V}^2 \times 10}}\right)^2} \approx 14.48$$

A value of 15 is used.

The second stage is the decision circuit and it is the heart of the comparator. It discriminates which one between the inputs is the bigger and it provides hysteresis to improve noise rejection. The cross-gate coupled transistors M9 and M10 create a positive feedback which enhances the gain ultimately. Moreover, the circuit permits to have hysteresis by unbalancing the form factors of transistors M8 to M11. Assuming $\beta_8 = \beta_{11} = \beta_A$ and $\beta_9 = \beta_{10} = \beta_B = 11\beta_A$, the hysteresis offset can be calculated as:

$$V_{HYST} = \frac{I_B}{g_m}\,\frac{\beta_B/\beta_A - 1}{\beta_B/\beta_A + 1} = \frac{10\,\mu\text{A}}{\sqrt{2 \times 70\,\mu\text{A/V}^2 \times 10 \times 5\,\mu\text{A}}}\,\frac{10}{12} \approx 100\,\text{mV}$$

Positive and negative trip voltages are the same with this design. A value of 100 mV ÷ 200 mV has been considered as a good trade-off between efficiency improvement and increased output ripple in pulse-skipping mode, after some simulations.

Next, a post-amplifier providing rail-to-rail output swing and further gain is inserted. In order to relax the requirement on the input common-mode range of this stage, the diode-connected transistor M12 is added: its aim is just to insert an offset voltage, so that the input common-mode voltage is lower, towards the middle of the rails. The design of this stage is standard and has been previously explained in Section 3.1. An inverter is finally placed to serve as a buffer.

In Figure 3.17 a simulation of the circuit shows that trip voltages are approximately 160 mV, a bit more than expected but acceptable.

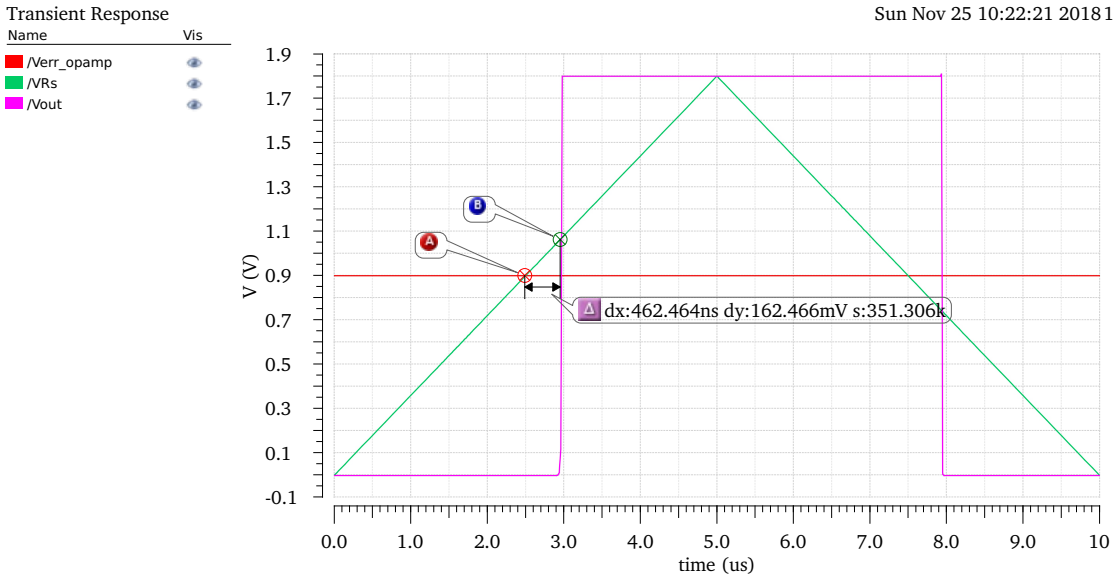
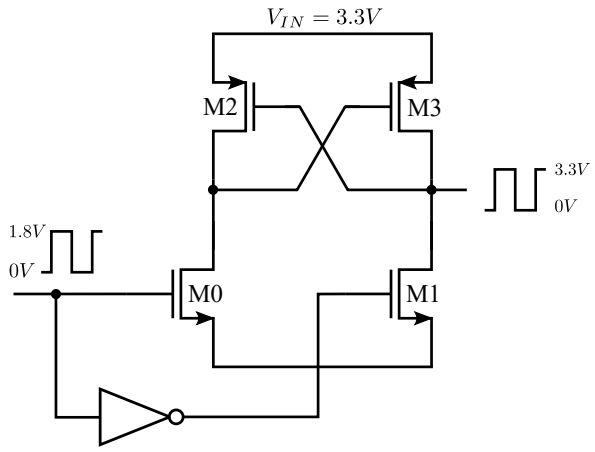


Figure 3.17: Comparator trip voltages simulation.

3.4 Gate driver



M0	2/0.6
M1	2/0.6
M2	2/0.5
M3	2/0.5

All transistors dimensions are in $\mu m/\mu m$.

Figure 3.18: Level shifter schematic.

Since the supply voltage for the control loop is 1.8 V, while the maximum rating for the gate-source voltage of power MOSFETs is 5 V, a level shifter is placed before the gate driver in order to use a smaller device, obtaining the same R_{on}. The voltage of the battery is in fact used to supply the gate driver, hence a conversion of the control square wave from V_{DD} to V_{IN} is needed. The schematic of the circuit is shown in Figure 3.18: it is a very simple latch-based shifter, fast

and without DC power consumption, leading to very good performances.

The gate driver is depicted in Figure 3.19: it is simply a cascade of inverters, the most used driving topology. Transistors have been dimensioned in order to match with the requirement on driving delay, listed in table 1.2, namely $\tau_{on,off} = 12\,\text{ns}$. The gate capacitance of the power MOSFET has been extracted from simulations and it is approximately 18 pF for the asynchronous design, while 35 pF for the synchronous one.

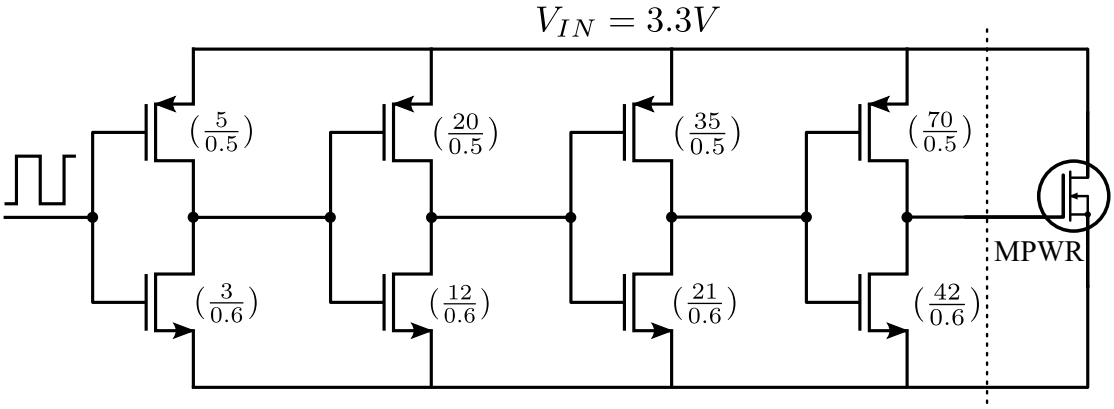


Figure 3.19: Power n-MOSFET driver schematic. All dimensions are in $\mu m/\mu m$.

3.5 Soft-start

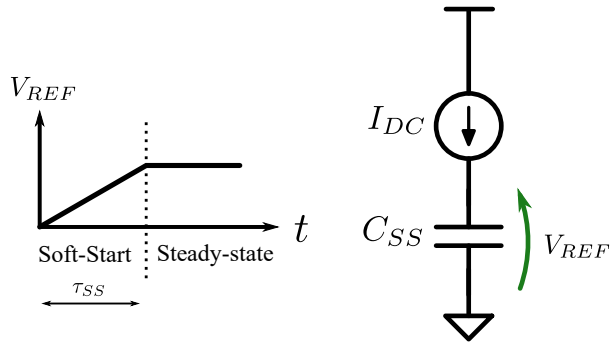


Figure 3.20: Soft-start principle.

As explained in Section 1.4, in order to avoid in-rush current during start-up a voltage ramp is provided as a reference at the input of the compensator, whose time length is calculated to ensure not to over-stress the components. This value has been set to 1 ms.

The simplest method is to inject a constant current I_{DC} on a capacitor C_{SS}, as depicted in Figure 3.20. However, although this method is effective, it is difficult to implement in a fully integrated way. The ratio of the current over the capacitance, indeed, should be 10^{-3} to have a 1 ms delay and a ramp height of 1 V. This means that either a really tiny current and a small capacitance, in the order of 1 nA and 1 pF respectively, or a normal current but a huge capacitance, in the order of 1 µA and 1 nF, have to be used. The first solution has the advantage to have a small occupation of area, thus it is indicated for a fully integrated design, but the critical drawback is that realize such a tiny current is difficult and the result could be very noisy and inaccurate [46]. On the other hand the latter is sufficiently precise but either an external capacitor is exploited or a very big area on the silicon die is occupied, both unacceptable costs.

Capacitance multiplier techniques can be exploited to overcome the aforementioned problems. A very good solution in terms of area occupation, accurateness and power consumption is presented in [44] and has been implemented. Subtractive current-mode and time-averaging capacitance multiplier techniques are used to obtain the ramp with driving currents and capacitances in the order of µA and pF respectively.

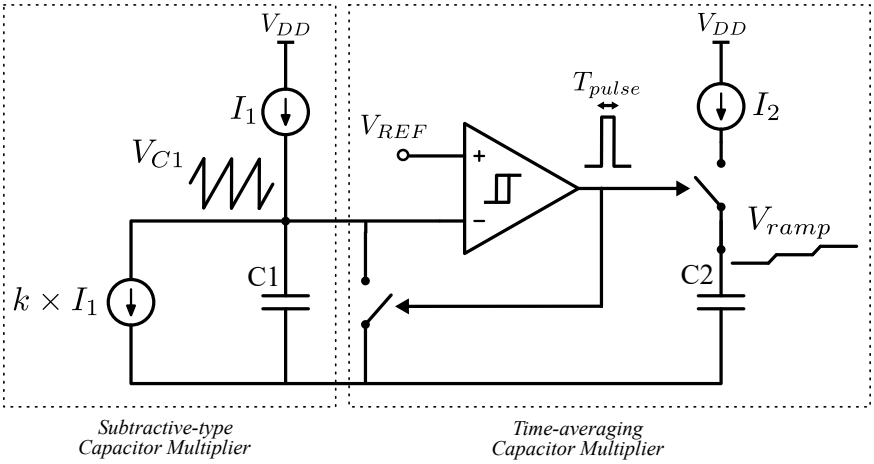


Figure 3.21: Soft-start ramp generation principle, exploiting capacitance multiplication techniques [44].

The working principle is illustrated in Figure 3.21. The circuit can be subdivided into two cascaded blocks, namely subtractive and time-averaging capacitance multiplier stages. In the first a current-mode technique is used and it is similar to the one explained in Section 3.2: the difference is just in the way the current feedback is obtained. Indeed, here the current is DC and the capacitor is referenced to ground, so a simple mirror can be used. Basically, a high portion of the bias

current is subtracted at the input terminal of the capacitor, resulting in a small current flowing through it. Calling I_1 the bias current, C_1 the capacitance and k the subtractive fraction ($0 < k < 1$), the higher the latter is the bigger the capacitance appears, because the effective current flowing through is $(1-k)I_1 << I_1$. The drawback is that power consumption increases beacuse a lot of current is wasted. However, this is a circuit activated during start-up only, which is a short period of time, hence it is worth it: a really relevant area on the die is saved on the other hand. The time needed for the voltage across C_1 to reach a reference value V_{REF} can be expressed as:

$$\tau_1 = \frac{C_1 V_{REF}}{I_{C_1}} = \frac{C_1 V_{REF}}{(1-k)I_1} \tag{3.21}$$

Next, the following stage exploits the fact that it is not important that the ramp is perfectly linear, but its average behavior should be. A possible approach is to charge another small capacitor with a not so small but pulsed driving current. The shape of the ramp will be a sum of small step functions, whit a linear overall behavior. A comparator with hysteresis is used to regulate the width of the pulses, while the frequency at which it changes state (i.e. the inverse of τ_1) is regulated by the previous stage. Indeed, the input of the comparator is the voltage across C_1 and the output is connected to two switches: one is responsible for discharging C_1, resetting basically the first stage, while the other for letting the bias current I_2 pass through C_2. Hysteresis is needed to keep the output of the comparator high for a sufficiently long time, hence ensuring that the first stage is fully reset; but at the same time the pulse should not be too long, otherwise the average current flowing through C_2 would be too high, leading to a small capacitance multiplication factor on the second stage. By defining the width of the pulse T_{pulse}, the number of cycles needed to let the output ramp reach V_{REF} can be expressed as:

$$N = \frac{C_2 V_{REF}}{I_2 T_{pulse}} \tag{3.22}$$

and so, referring to Eq. 3.21, the total soft-start time is:

$$\tau_{SS} = N\tau_1 = \frac{C_1 C_2 V_{REF}^2}{(1-k)I_1 I_2 T_{pulse}} \tag{3.23}$$

With $C_1 = 0.5\,\text{pF}$, $C_2 = 0.75\,\text{pF}$, $k = 0.9$, $I_1 = 1\,\mu\text{A}$, $I_2 = 0.75\,\mu\text{A}$ and $T_{pulse} = 5\,\text{ns}$, which are reasonable values, the total soft-start time, by substitution in Eq. 3.23, is:

$$\tau_{SS} = \frac{0.5\,\text{pF} \times 0.75\,\text{pF} \times (1\,\text{V})^2}{(1-0.9) \times 1\,\mu\text{A} \times 0.75\,\mu\text{A} \times 5\,\text{ns}} = 1\,\text{ms}$$

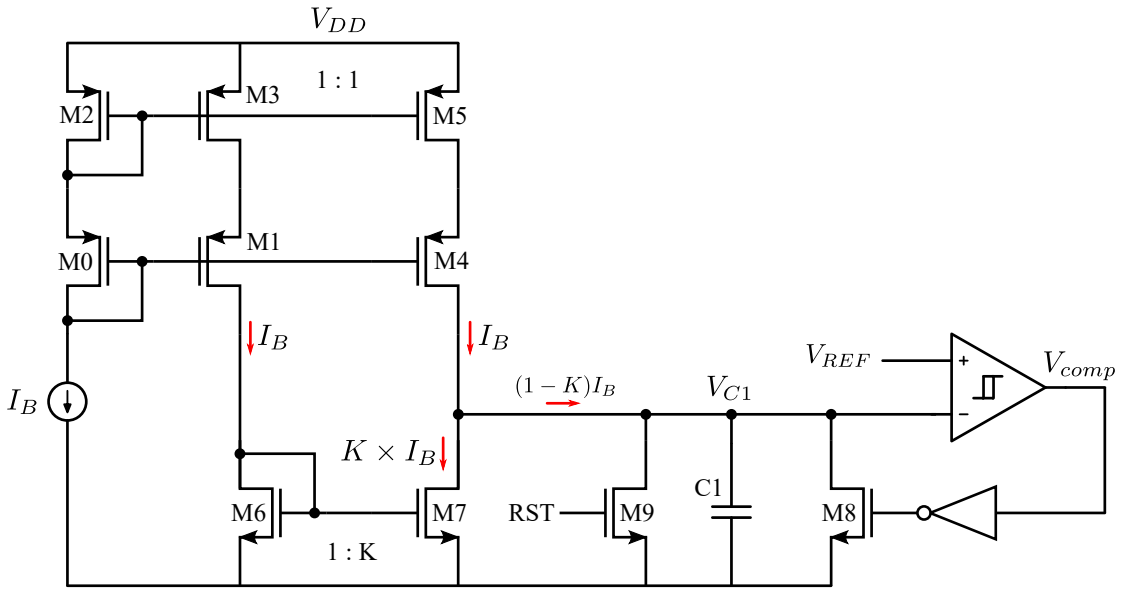
The whole system has been then implemented at transistor-level. The schematic of the comparator is the same as in Figure 3.16, but the form factors of transistors are modified to ensure a pulse width of 5 ns. Since it is not immediate how to relate the pulse width to the trip voltages (it depends also on the input waveform), the proper value of the ratio of β_B/β_A (see Section 3.3) has been attained by mean of simulations. The final aspect ratios are listed in the Figure 3.22. The length of transistors M8 to M11 has been increased to 2 µm in order to reduce the error due to geometrical mismatches. The ratio β_B/β_A should be in fact rather precise to get an accurate pulse width.

M0	15/1	M1	15/1	M2	10/1	M3	10/1	M4	2/1
M5	2/1	M6	4/1	M7	4/1	M8	6/2	M9	8/2
M10	8/2	M11	6/2	M12	10/1	M13	10/1	M14	10/1
M15	10/1	M16	3/1	M17	3/1	M18	2/1	M19	10/1

Figure 3.22: Transistors dimensions of the soft-start comparator, in $\mu m/\mu m$.

The first stage is depicted in Figure 3.23. The bias current I_1 is generated with cascode mirrors (M0 to M5) to ensure a more stable value of the current within the whole range of the voltage across C_1 (V_{C_1}). The subtraction at the node V_{C_1} is realized with a simple current mirror, i.e. with transistors M6 and M7. In order to have an accurate mirroring, their dimensions have been set to quite high values, respectively 40/2 and 36/2, so that geometrical errors are reduced. M8 is responsible to reset C_1, while M9 is added to ensure that the circuit start from a defined initial value when the `RST` signal is asserted. The time waveform of the voltage V_{C_1} is shown in Figure 3.24. The time length of the ramp is 7 µs instead of the expected 5 µs: this is because V_{C_1} swings a lot (from 0 V to 1 V), thus the current is not mirrored precisely by both branches M4-M5 and M7. We can see in fact that the slope is not perfectly linear, especially in the last part. However, this is not an issue: a slightly longer time is not crucial at all. On the contrary, it is more conservative in terms of stresses on components, because the average duty cycle during this phase will be lower.

The time-averaging capacitance multiplier transistor-level circuit is presented in Figure 3.25. The passing switch is realized with the p-MOSFET M4, which is open when $V_{comp} = V_{DD}$ while it lets the bias current pass through C_2 when $V_{comp} = 0\,\text{V}$. Again, the bias current is generated with a cascode mirror in order to have a more accurate result. Referring to the figure, $I_B = 1\,\mu\text{A}$ and N=0.75, obtaining a driving current of 0.75 µA. However, the node between the source of



M0	10/1	M1	10/1	M2	10/1	M3	10/1
M4	10/1	M5	10/1	M6	40/2	M7	36/2
M8	3/0.2	M9	2/0.2	C1	0.5 pF	I_B	1 µA

All transistors dimensions are in $\mu m/\mu m$.

Figure 3.23: Soft-start current-mode subtractive-type capacitor multiplier.

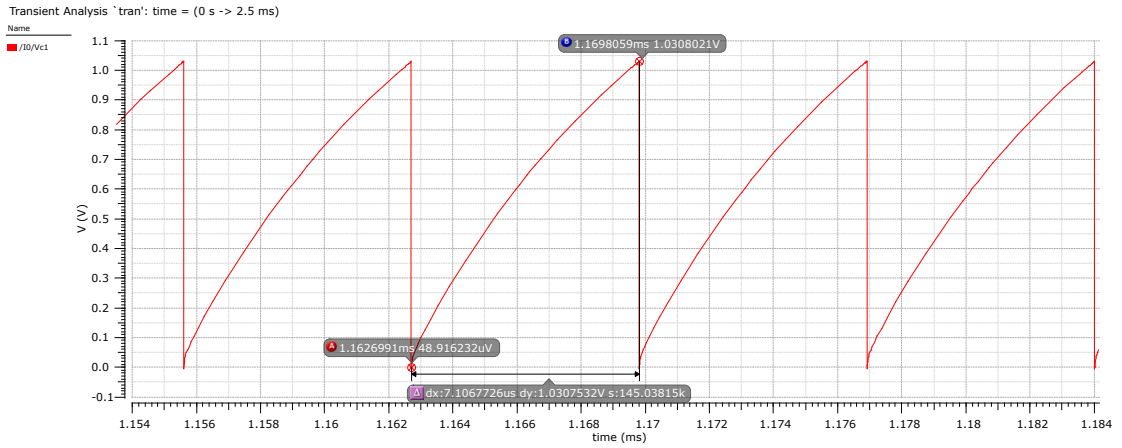
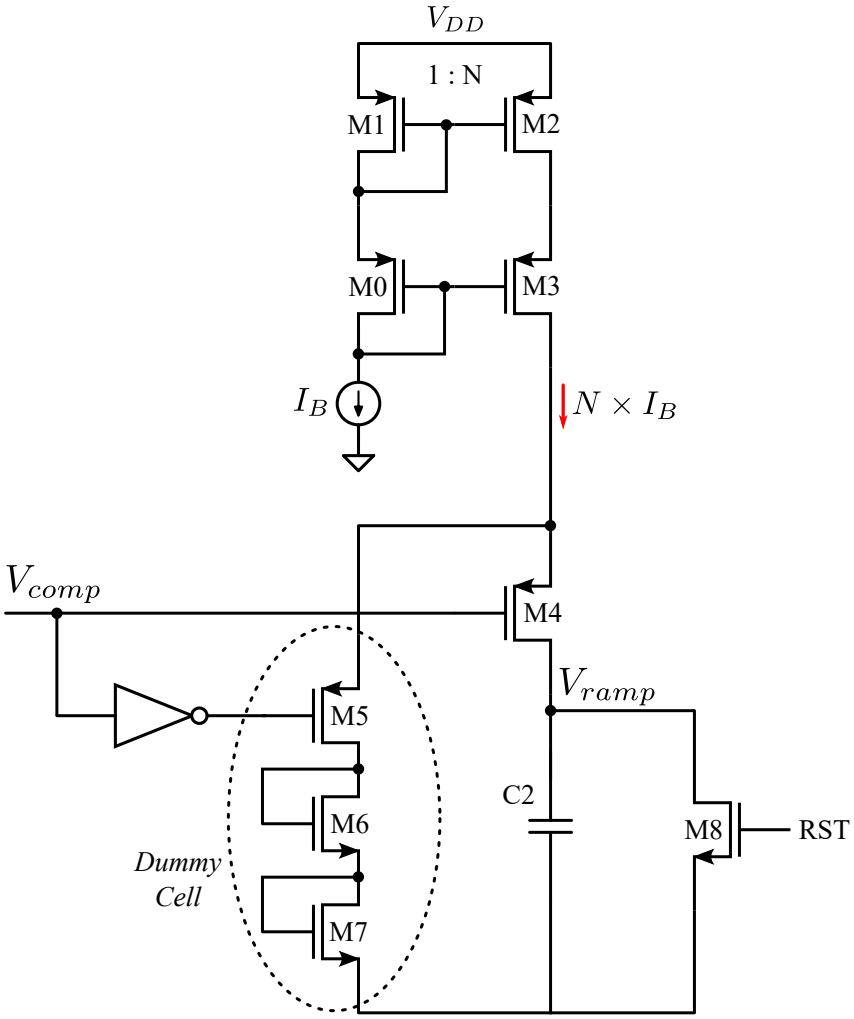


Figure 3.24: Time waveform of the voltage V_{C_1}.



M0	10/1	M1	10/1	M2	7.5/1	M3	7.5/1	M4	1/0.25
M5	1/0.25	M6	1/0.18	M7	1/0.18	M8	2/0.2	C2	0.75 pF

All transistors dimensions are in $\mu m/\mu m$

Figure 3.25: Soft-start averaging-type capacitor multiplier.

M4 and the drain of M3 swings a lot, especially when V_{ramp} is low because when $V_{comp} = 0\,\mathrm{V}$ the voltage at that node will be the threshold plus the overdrive, while when $V_{comp} = V_{DD}$ it will be just below V_{DD}. This means that all the parasitic capacitances at that node need to be charged and discharged, leading to spikes in the current flowing through M4, thus C_2. The result is that the driving current is not precise at all. A dummy cell is added to solve this issue, by keeping the voltage at the source of M4 almost constant. Moreover, it provides a path for the driving current when M4 is off, maintaining the mirror formed by transistors M0 to M3 always active. M5 has the function of a switch, complementary to M4, and M6 and M7 have been designed in order to produce a voltage more or less equal to a threshold plus the overdrive of M4, so that the source of M4 remains always at an almost constant voltage. In this way current spikes are reduced a lot. M8 has the function of resetting to 0 V the voltage across C_2 when the `RST` signal is asserted.

Finally, some logic circuitry has been designed to produce two signals, `RST` and `READY`, with one input only, namely `RESET`, so that the converter communicates with the main digital control just with two signals (`RESET` and `READY`). When `RESET` is asserted the converter starts from initial conditions: it is off and the reference voltage of the compensator is zero. Once RESET is released, the generation of the soft-start ramp begins and when it reaches the final value the signal `READY` is asserted, meaning that the output of the converter is 20 V, thus the stimulator can be used. The `RST` signal finally controls the transistors which reset the capacitors C_1 and C_2 of the soft-start circuitry. Figures 3.26 and 3.27 show the block diagram of the digital control.

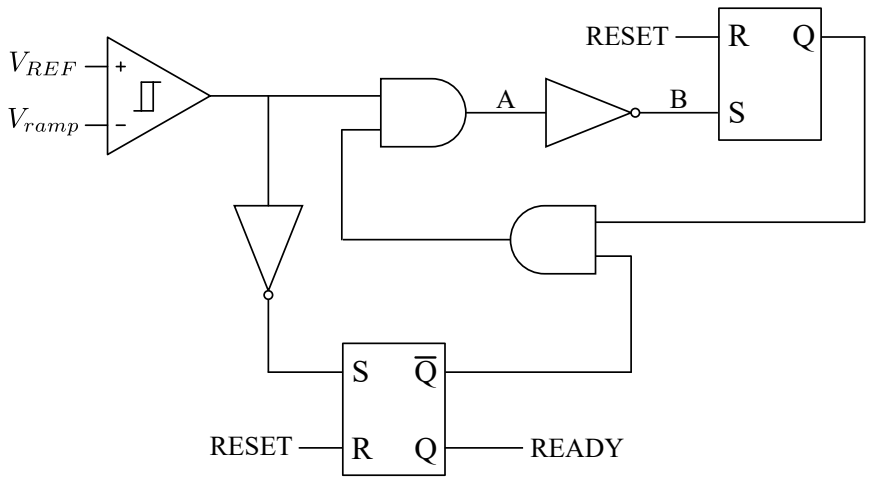


Figure 3.26: Logic control for the soft-start circuit (I).

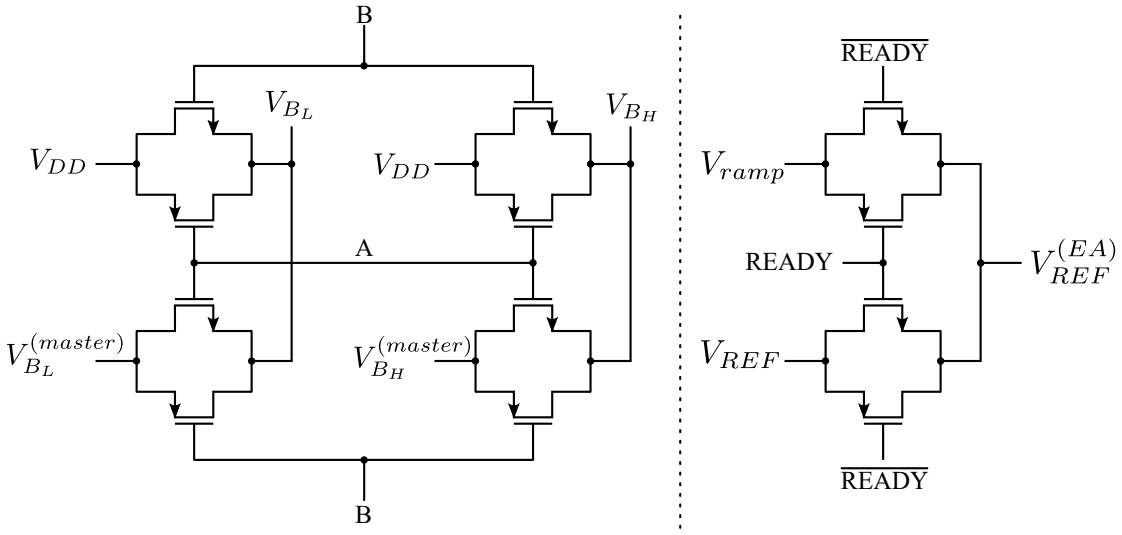


Figure 3.27: Logic control for the soft-start circuit (II).

By referring to Figure 3.26, `B` is the `RST` signal. When `RESET` is high, `READY` is low, `B` (`RST`) is high and so the capacitors C_1 and C_2 are discharged, hence the output of the comparator is high ($V_{ramp} = 0\,\mathrm{V} < V_{REF} = 1\,\mathrm{V}$). When `RESET` is released, `A` and `B` toggle, thus `RST` is low and the soft-start circuitry starts working. Once V_{ramp} reaches V_{REF}, the bottom flip-flop is set: `READY` becomes asserted while `A` and `B` toggle again, resetting the two capacitors C_1 and C_2. This state is maintained until `RESET` goes high again. Finally two multiplexers, depicted in Figure 3.27, are exploited to provide the correct bias voltages to the soft-start circuit (on the left of the figure) and the right reference voltage to the error amplifier (on the right of the figure). Particularly, the multiplexer on the left is responsible to shutdown all the cascode mirrors when the converter is not in soft-start mode, so that this circuitry does not consume any power.

Figures 3.28 and 3.29 show transient simulation results of the whole boost converter during soft-start, demonstrating proper functionality. The length of the ramp is approximately 1.2 ms and the logic signals are correct, as expected. Notice that the maximum inductor current during this phase is 340 mA, confirming the fact that the in-rush current issue is solved with this technique.

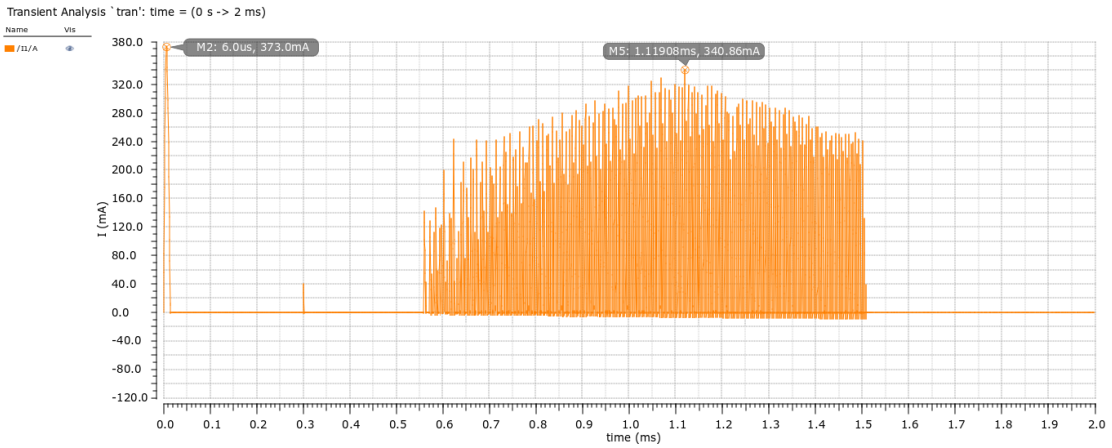


Figure 3.28: Inductor current during soft-start.

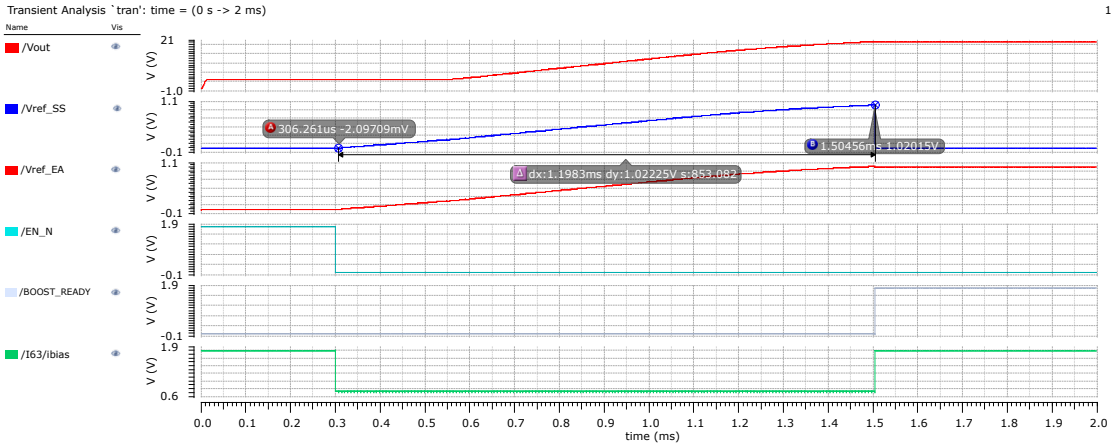


Figure 3.29: Waveforms and signals during soft-start.

3.6 Synchronous converter

A synchronous boost is build with an active switch instead of the diode. Usually, n-type MOSFETs are preferred to p-ones because they offer better performances, namely lower R_{on} with the same size. However, high-side driving of n-MOSFETs is more complicated, because a voltage higher than the source is required and is not available in the converter (the highest voltage is the output, which is connected to the source/drain of the transistor). Typical solutions to obtain such a voltage are charge pumps or bootstrap capacitors, but they require additional circuitry and possibly big components (in particular capacitors). A p-MOSFET, on the contrary, needs a gate voltage lower than the source, which can be obtained more easily, i.e.

by scaling down the output voltage of the boost itself. The proposed solution is basically to set a reference voltage for the high-side driving circuitry, which is used as lower supply for the control of the p-MOSFET. Communication between low-side and high-side is needed to drive both power transistors correctly and safely. The whole feedback loop described in the previous sections and chapters is the same also in the synchronous design: it is responsible for compensation and power n-MOSFET driving, which remain unchanged.

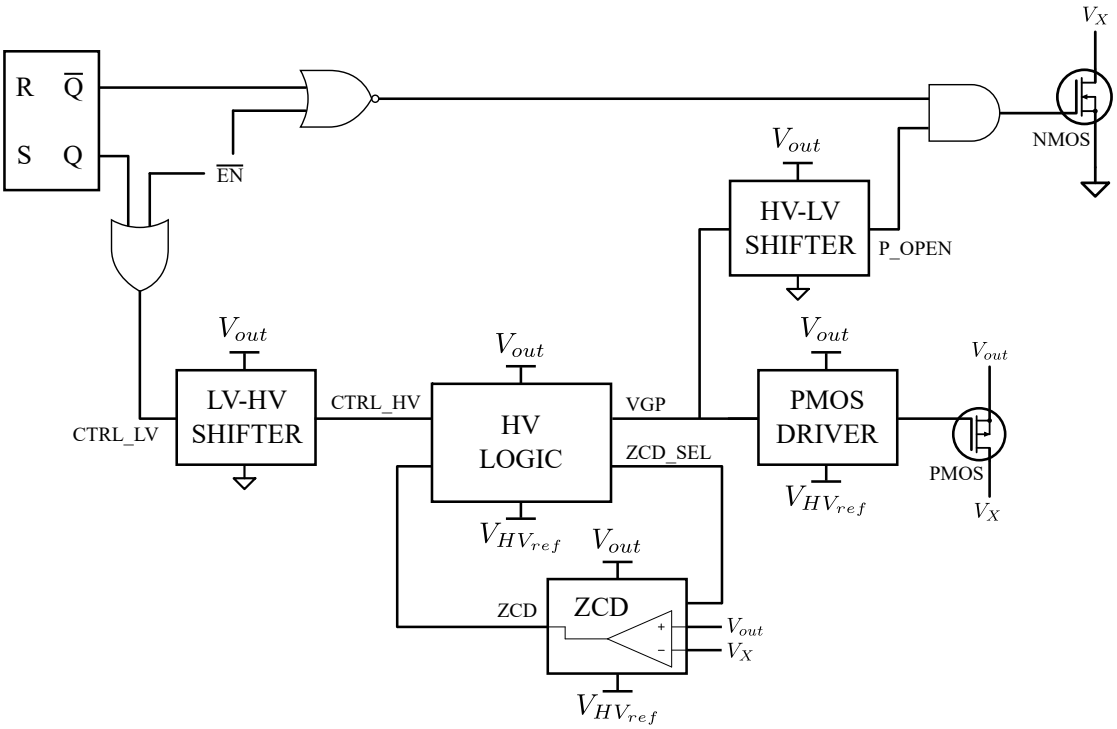


Figure 3.30: Block diagram of the p-MOSFET control circuitry.

In this section the additional blocks required to drive the p-MOSFET of the synchronous converter are presented. They have been designed with Verilog-A HDL only partially, because the needed circuitry and the constraints were quite straightforward, thus they have been built mainly at transistor-level directly. Listing:

- a logic control is needed to guarantee dead times between the activation of the low-side switch and the high-side one, otherwise the output would be shorted during that interval. This is critical and of paramount importance obviously;
- a gate driver, ensuring that the absolute maximum ratings on the gate-source voltage of the power MOSFET are satisfied;

– a way to detect the instant in which the current through the inductance becomes null, required to enable DCM operation; the block responsible of this function is called *Zero Current Detection* (ZCD);

– the power consumption of the whole additional circuitry should be low enough in order not to compromise the benefit given by a synchronous boost vs an asynchronous one in term of efficiency.

In Figure 3.30 the block diagram of the p-MOSFET driving circuit is depicted. The reference voltage ($V_{HV_{ref}}$) generation only has been omitted, but it will be presented in the next section.

3.6.1 Voltage reference regulation

In order to set and stabilize the voltage reference needed by the control circuitry of the high-side power p-MOSFET, a standard linear regulator is used. The amplifier creating the feedback high-gain loop has been done with HV transistors in order to guarantee the respect of absolute maximum ratings on junction breakdown voltages (it regulates a voltage of approximately 15 V in steady-state). The schematic of the circuit is shown in Figure 3.31. Basically the op-amp regulates the voltage $V_{HV_{ref}}$

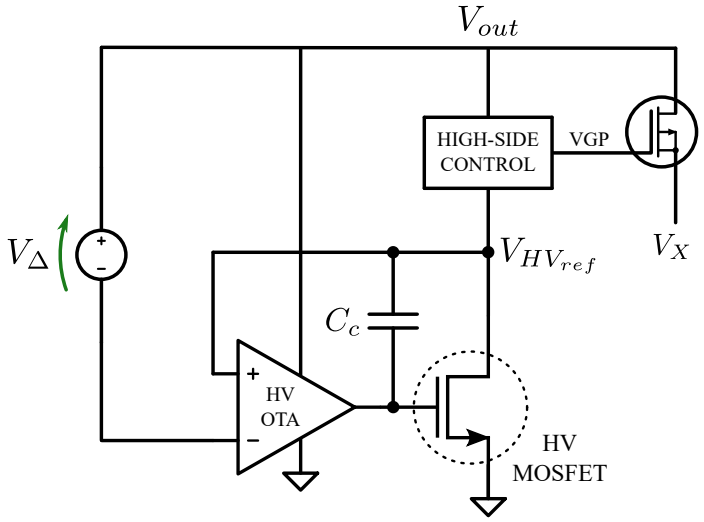


Figure 3.31: Linear regulator for the high-side reference voltage.

by controlling the current flowing through the HV MOSFET. The capacitor C_c is placed to absorb high-frequency current spikes coming from the high-side control and to compensate the feedback loop to guarantee the stability of the system.

The voltage reference V_Δ is connected in that way because ideally it has to track any variations of the output voltage, namely:

$$V_{out} - V_{HV_{ref}} = V_\Delta = const.$$

ensuring that the gate-source voltage of the power MOSFET does not exceed maximum ratings ($-5.5\,\mathrm{V}$) and the same for any transistor in the high-side control circuitry. Obviously ideal voltage sources do not exist and a circuit achieving sufficient performances should be designed. The simplest but effective method is to sense the output voltage with a resistive voltage divider, so that in steady-state V_Δ is $5\,\mathrm{V}$. Actually this comes without any additional cost because the compensation feedback loop measures the output voltage yet with a voltage divider (see Figure 3.6). R_1 can be therefore subdivided into the series of two resistors $R_1^{'}$ and $R_1^{''}$, as shown in Figure 3.32. Nothing changes for the error amplifier and for the transfer

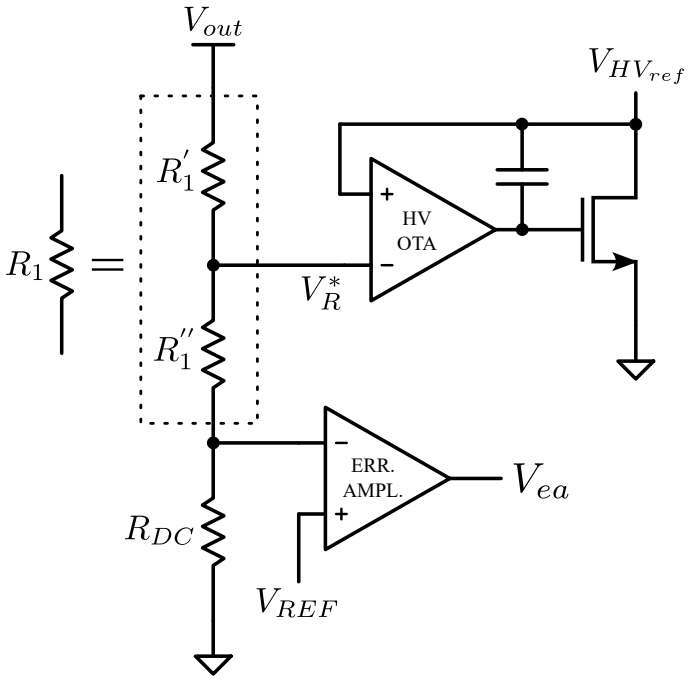


Figure 3.32: Voltage reference for the linear regulator.

function of the compensator, but the voltage reference V_R^* can be generated:

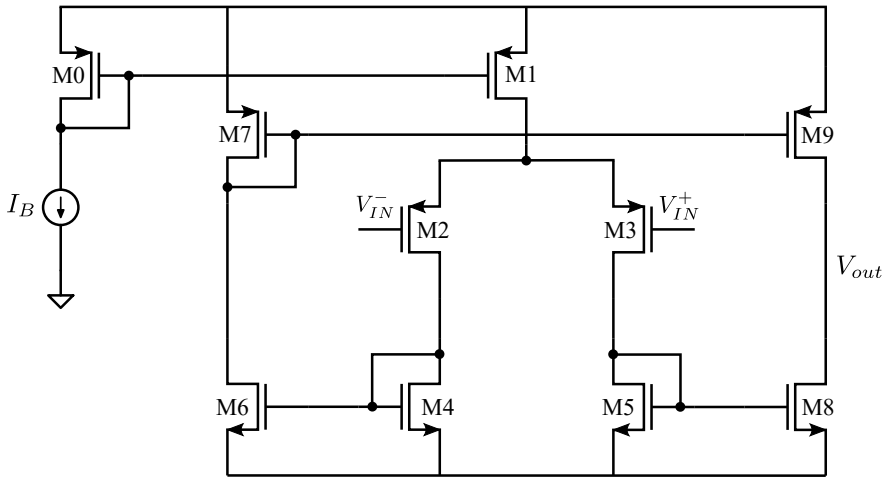
$$V_R^* = \frac{R_1^{''} + R_{DC}}{R_1^{'} + R_1^{''} + R_{DC}} V_{out} \tag{3.24}$$

By using parameters of Table 3.3 and inverting Eq. 3.24, the value of the resistances resulting in a voltage $V_R^* = 15\,\mathrm{V}$ are the following:

$$R_1' = 30.9\,\mathrm{k\Omega} \quad , \quad R_1'' = 86.6\,\mathrm{k\Omega}$$

To be precise, this is not a tracking reference because it does not subtract a constant offset from the output voltage but rather it provides a ratio of that voltage. However, by assuming small ripple (true in steady-state), it will be constant with a good approximation. The tricky point is the start-up phase: indeed during this operating mode the output voltage starts from 0 V and increases up to 20 V, hence V_Δ is not constant at all and, more importantly, is lower than 5 V, possibly below the threshold of the power MOSFET. This means that the power MOSFET does not close as it should and so body diode conducts for the whole period, leading to higher losses. However, this is not critical because the start-up phase lasts just for a short time with respect to the steady-state operation, thus does not affect the overall efficiency of the converter significantly.

The op-amp used to achieve high-gain in the regulator is a standard *Operational Transconductance Amplifier* (OTA). The design procedure is very similar to the one reported in Section 3.1 for a two-stages op-amp. Transistors here are HV devices, thus their output resistance is much bigger than the corresponding LV: a single-stage OTA is preferred because it achieves a sufficient gain but has better frequency and driving performances. Figure 3.33 shows the schematic of the OTA and the dimensions of the various transistors. Since the only high-impedance node



M0	10/2
M1	10/2
M2	10/3
M3	10/3
M4	20/3
M5	20/3
M6	20/3
M7	20/1
M8	20/3
M9	20/1
I_B	5 µA

All transistors are HV devices. Dimensions are in $\mu m/\mu m$.

Figure 3.33: Schematic of the HV OTA used in the regulator.

in the OTA circuit is the output, Miller effect is exploited for the compensation by inserting a capacitor C_c as depicted in Figure 3.31. The value of the capacitance is 10 pF: it is quite big both to insert a dominant pole in the transfer function and

to cause sufficiently low voltage spikes due to high-frequency currents injected by the high-side control.

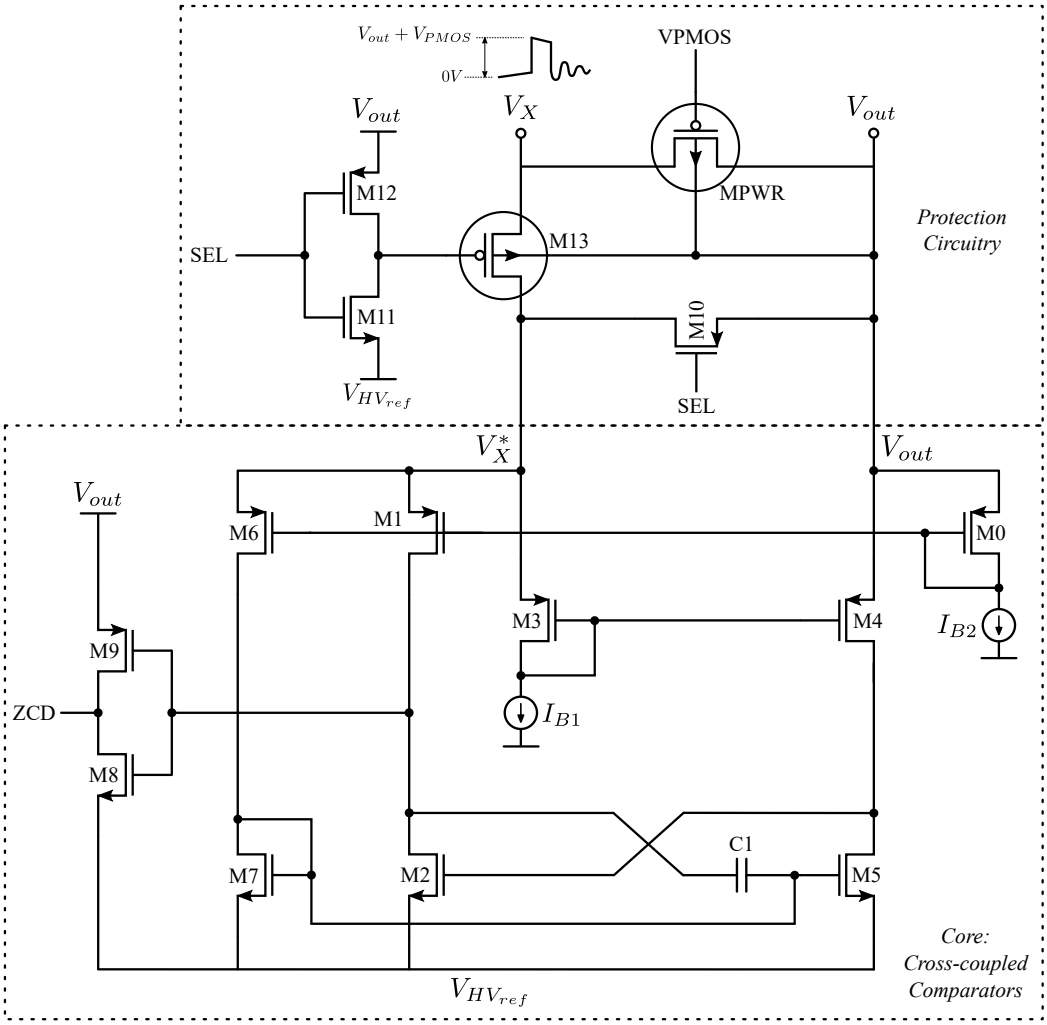
Stability analysis yields to a phase margin of 84° at a crossover frequency of 284 kHz, with a DC gain higher than 115dB. Nevertheless, commutations of the high-side power transistors cause relevant current spikes which are absorbed by the capacitor C_c and sensed by the feedback loop. Since they are at very high frequency (pulses last for 15 ns), a non-negligible voltage spike of approximately 1.2 V appears for few nanoseconds. However, proper functionality is demonstrated with simulations: the gate-source voltage across the p-MOSFET in this phase is sufficient to turn on the transistor, hence the body diode conducts just for a very short time and the whole high-side circuitry works correctly.

3.6.2 Gate driver

The gate driving circuit for the high-side power p-type MOSFET is very similar to the low-side one, i.e. a cascade of inverters. In this case it is simpler because a level shifter is not needed, since the whole control is supplied with a 5 V voltage, sufficient to drive the power transistor. The schematic is the same of Figure 3.19, but, instead of using LV 1.8 V devices, HV 5 V transistors are exploited. The gate capacitance of the p-MOSFET is approximately 20 pF, thus dimensions of each MOSFET in the driver schematic are similar to the low-side equivalent one, but adjusted to have approximately 15 ns of turn-on time.

3.6.3 Zero Current Detection

As previously mentioned, a ZCD circuit is needed to detect the instant at which the current becomes null. At that moment the switch has to be opened, enabling DCM operation. A popular method [47] is to sense the voltage across the p-MOSFET: since it is directly proportional to the current flowing through, the point at which it is null coincides with a zero current. A simple implementation is to use a comparator with the inputs across the power MOSFET. However, the standard common-source based comparator cannot work because of common-mode input issues. An effective alternative is to use cross-coupled comparators with the inputs at the source of current-biased p-type transistors [17], as shown in Figure 3.34. One comparator is composed by transistors M0, M1 and M2, while the other by M3, M4 and M5. Focusing on the core (lower part of the figure), taking only the first comparator as instance, the working principle is the following: the current I_{B2} passes always through M0, thus its V_{GS} is constant; the source is connected to the output node V_{out}, hence the gate voltage of M0 is $V_{out} - V_{GS_{M0}}$, which is equal to the gate voltage of M1. But the source of M1 is connected to V_X^*, so its V_{GS} depends on it and regulates the current flow through M1. Specifically, when



M0	5/1	M1	5/1	M2	3/1	M3	5/1
M4	5/1	M5	10/1	M6	5/1	M7	12/1
M8	2/1	M9	4/1	M10	10/1	M11	2/1
M12	4/1	M13	30/0.5	C1	20 fF	$I_{B1,2}$	10 μA

All transistors dimensions are in $\mu m/\mu m$.

Figure 3.34: ZCD circuit: cross-coupled comparators with bias and protection circuits.

$V_X^* > V_{out}$ M1 will produce more current than M0 and viceversa. This feature can be used to discriminate the ZCD instant, i.e. when the drain currents of M0 and M1 are the same.

By exploiting the same principle on the other comparator and by connecting them in a cross-coupled way, an overall comparator is effectively built. The cross-gate connection helps to enhance speed and noise rejection, because of the positive feedback and the fact that the two comparators act in an opposite way, amplifying in a sense the input voltage. M6, M7 and C1 are used to provide a stable DC steady-state operating point. In fast transients C1 can be approximated as a short-circuit, thus it latches transistor M2 and M5, which are the decision couple of the comparator. On the contrary, in steady-state, when $V_X^* < V_{out}$ C1 is an open-circuit and it is possible to force `ZCD='1'` by dimensioning M4, M6, M7 and M5 opportunely, that is by ensuring that $I_{D5} < I_{D4}$. C1 should be small in order not to degrade speed performances. Transistors M8 and M9 provide the correct rail-to-rail swing of the logic signal `ZCD`, from $V_{HV_{ref}}$ to V_{out}.

Nevertheless, a critical problem about absolute ratings is present. Indeed the voltage V_X swings over a wide range of voltage, namely from 0 V to 20 V (V_{out}). Without any protection mechanism ratings on V_{GS} of transistors and on the junction breakdown voltages would not be respected. This is the reason why MOSFETs from M10 to M13 are added. The node V_X^* is connected either to V_X or V_{out}, according to the logic signal `SEL`: when it is asserted, M13 is on and M10 off, and viceversa on the other case. When the ZCD circuit must be working, i.e. when $V_X \approx V_{out}$, `SEL` has to be asserted, thus M13 acts as a short and $V_X^* \approx V_X$ (M13 should be big enough to guarantee that). On the contrary, when the core must be protected, i.e. when $V_X \approx 0$ V, M10 is a short, hence $V_X^* \approx V_{out}$, M13 is open and protects the circuit because it is an HV device. Notice that it has a symmetrical structure: the source is connected to V_X^*, so both its drain-source and gate-source voltage ratings are respected. The digital control therefore is responsible to provide the correct timing on the signal `SEL` to ensure safe operation.

In Figure 3.35 the time waveform of the inductor current is plotted. From the graph it is possible to obtain the delay associated to the ZCD block, which is approximately 32 ns, i.e. the time needed by the cross-coupled comparators to sense the zero-current point and change the state. This is equivalent of a peak negative current of 10 mA, which represents a good performance definitely. Notice indeed that also in the asynchronous design a negative current appears, due to the reverse recovery time of the diode.

The designed circuit is functional and works properly. However, power consumption is quite high due to the fact that both comparators are always active and, particularly, that M1 and M6 sink a lot of current. When the protection circuitry is active, indeed, $V_X^* < V_{out}$ because of the voltage drop across M10, thus

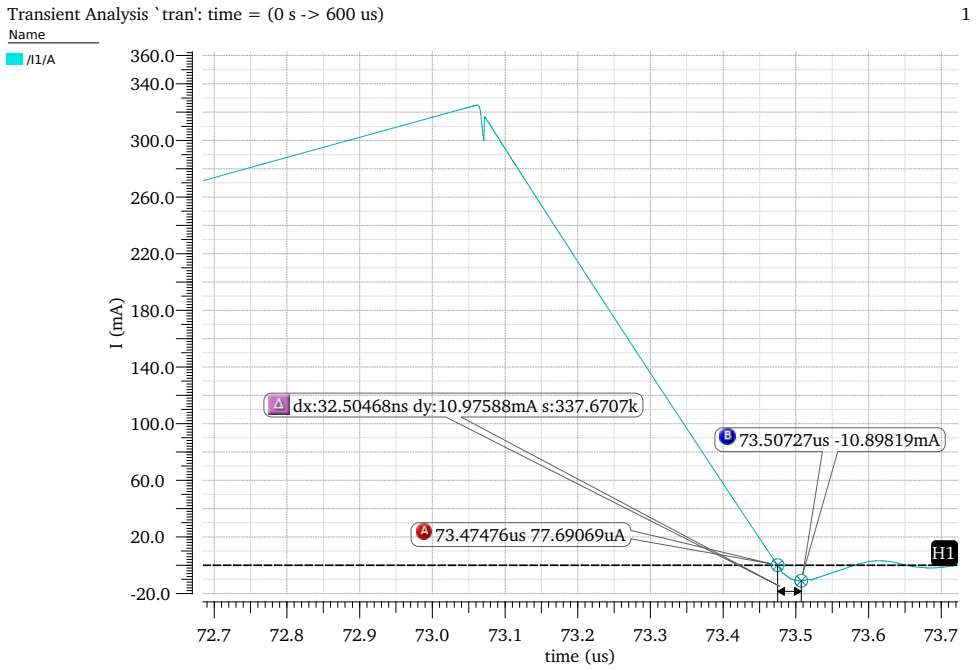


Figure 3.35: Inductor current waveform in the synchronous design: effect of ZCD delay.

I_1 and I_6 are bigger than I_{B2}. All this results in an average power consumption of 2.8 mW, which definitely compromises the improvement in efficiency obtained by using the p-MOSFET instead of the Schottky diode. In order to decrease consumed power relevantly, one bias current (I_{B2}) can be switched on only when the ZCD block is needed, i.e. during the conduction time of the p-MOSFET. By doing this, the proper default value `ZCD='1'` is ensured when I_{B2} is off: in fact M1 and M6, and thus M7 and M5, are off while M4, and hence M2, are on, leading to a stable asserted output. During this phase the power consumption is linked to I_{B1} only, i.e. approximately one-fourth compared to the previous system. Notice that the on period of the p-MOSFET is just a small portion of T_{sw}, so the improvement in power saving is expected to be really relevant.

A logic signal is needed to control the activation/deactivation of the bias current. The required information is already contained in the `SEL` signal of the ZCD block. However, it is a high-side logic block, thus it is quite expensive in terms of power consumption and delay to down-convert that signal. An equivalent low-side has been created therefore, based on `CTRL` and `POPEN` signals. The schematic is shown in Figure 3.36. The bias current is controlled by switching on and off a transistor, i.e. M3 in the figure. M1 and M2 are HV devices because the ZCD block works on high voltages, while M3 is LV, since at the gate the voltage does

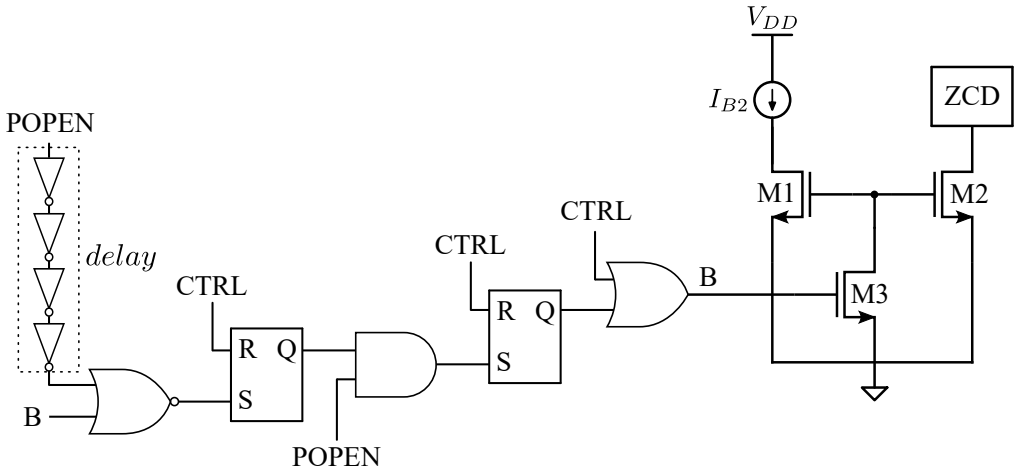


Figure 3.36: Logic circuit for power saving in the ZCD block.

not exceed V_{DD} surely. There are three phases on this control:

1. `CTRL='1'`, `POPEN='1'`: power n-MOSFET is on, so `B='1'`, M3 is on and the bias current of the ZCD block is deactivated. Hence `POPEN='1'` is stable and power consumption is reduced;

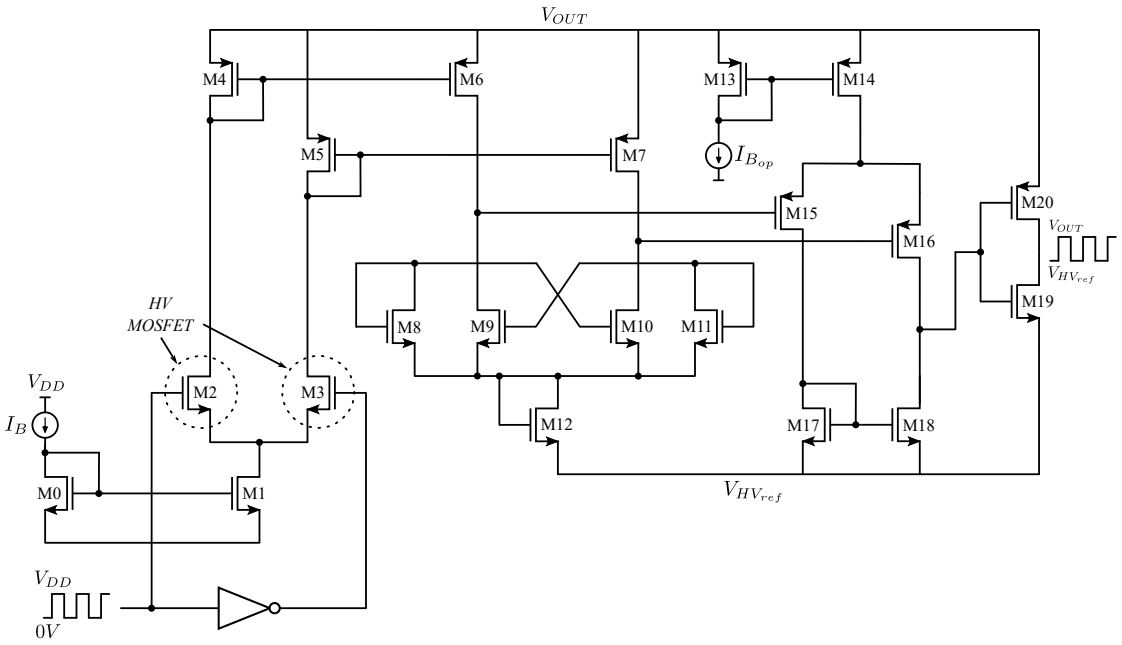
2. `CTRL='0'`, `POPEN='1'`: as soon as `CTRL` is low, `B='0'`, M3 becomes open and as a consequence the ZCD block is turned on, i.e. correctly biased. A short time is then required to its full activation, next also `POPEN` goes low;

3. `CTRL='0'`, `POPEN='0'`: the logic stays in this state waiting a commutation either of `POPEN`, coming from high-side (if DCM operation), or `CTRL` from low-side (if CCM operation) to disable the current mirror. Then it returns to the initial state, namely (1.) of this list. Flip-flops are used to ensure correct timing of `POPEN` sensing, while `CTRL` can go directly on the last `OR` gate.

With this technique efficiency is improved a lot especially at light load. The average power consumption becomes 1.1 mW indeed, which is much less compared to the previous 2.8 mW. Further improvements are hard to achieve due to the fact that the ZCD block requires a considerable current to have a fast response, thus bias currents cannot be reduced so much. Notice moreover that a slow activation means a bigger negative current on the inductor (because the delay is longer), which is translated ultimately in a drop in the efficiency, because some energy is subtracted from the output capacitor and transferred to the input. This has been considered therefore a good trade-off between speed and efficiency.

3.6.4 Logic control

The digital logic control have to guarantee proper dead times between activation/deactivation of the two power switches. Moreover it has to provide the signal `SEL` needed by the ZCD circuitry (see Section 3.6.3). The inputs of the block are the ZCD circuit output and the `CTRL` (output of the SR flip-flop of the low-side control loop) signals. A choice was made to put this digital circuit on the high-side, so that it is very fast to respond to `ZCD` commutations: the p-MOSFET could be switched off very quickly, just after the assertion of `ZCD`. The alternative would have been to keep the whole control ground-referenced, but in that case the `ZCD` signal should have been passed from high-side to low-side and then viceversa, increasing the delay time significantly.



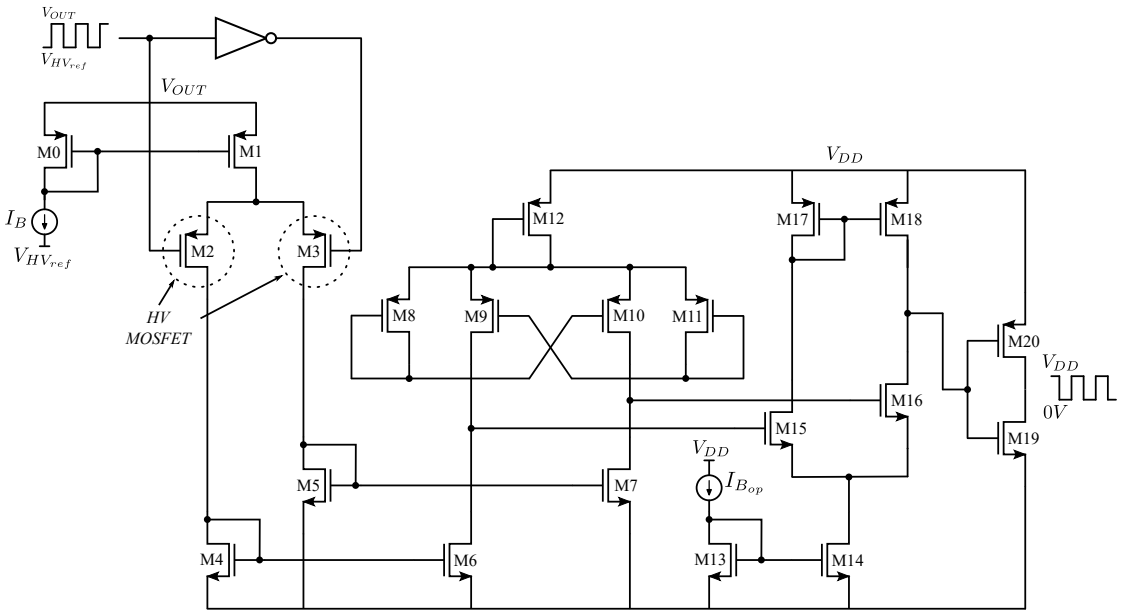
M0	2/1	M1	2/1	M2	10/1.3	M3	10/1.3	M4	0.5/1	M5	0.5/1
M6	1/2	M7	1/2	M8	1/1	M9	2/1	M10	2/1	M11	1/1
M12	5/1	M13	10/1	M14	10/1	M15	2/1	M16	2/1	M17	1/1
M18	1/1	M19	1/1	M20	2/1	I_B	10 μA	$I_{B_{op}}$	5 μA	V_{DD}	1.8 V

All transistors dimensions are in $\mu m/\mu m$.

Figure 3.37: Logic level shifter, from LV to HV (LV-HV SHIFTER block).

The fundamental block required to enable this kind of control is a level shifter of the logic signal from low-side to high-side and viceversa, so that the two circuits can communicate. The solution described in Section 3.4, based on a simple latch, cannot be recycled for this purpose, because the gate-source voltage of the top transistors would exceed the allowed ratings. The proposed circuits are depicted

in Figure 3.37 and 3.38, respectively for the low-side to high-side shifting and viceversa. Taking as instance the first (the second one is perfectly symmetrical), the idea is to use a standard comparator with different voltage references and both HV and LV devices. M2 and M3 are HV MOSFETs, while M4 and M5 LV: hence ratings on V_{GS} and junction breakdown voltages are respected. This input stage is ground-referenced and the input is a square wave from 0 V to 1.8 V, switching on and off alternatively M2 and M3. The whole following circuit on the contrary is referenced to the high-side negative supply $V_{HV_{ref}}$, linearly regulated (see Section 3.6.1). The output of the block will be a square wave from $V_{HV_{ref}}$ to V_{out}, i.e. approximately from 15 V to 20 V in steady-state. The dimensions of each transistor are kept as small as possible, to ensure a short processing delay time. Particularly, M4 and M5 should be very small in order to reduce parasitic capacitances, which act as a pull-up network with the transistor itself when the respective HV driving MOSFET is off. Nevertheless, at the same time they should provide a gate-source voltage high-enough to turn on and off M6 or M7. The proposed solution achieve good performances: a delay of approximately 8 ns is required to translate the waveform, with low area occupation and an overall quiescent current of 15 µA.



M0	5/1	M1	10/2	M2	10/1	M3	10/1	M4	1/1	M5	1/1
M6	1/1	M7	1/1	M8	2/1	M9	4/1	M10	4/1	M11	2/1
M12	10/1	M13	4/1	M14	4/1	M15	1/1	M16	1/1	M17	1/1
M18	1/1	M19	1/1	M20	2/1	I_B	10 µA	$I_{B_{op}}$	5 µA	V_{DD}	1.8 V

All transistors dimensions are in $\mu m/\mu m$.

Figure 3.38: Logic level shifter, from HV to LV (HV-LV SHIFTER block).

The high-side to low-side level shifter is perfectly symmetrical: p-MOSFETs are used instead of n-ones and voltage references are swapped. See Figure 3.38 for details on dimensions and bias currents.

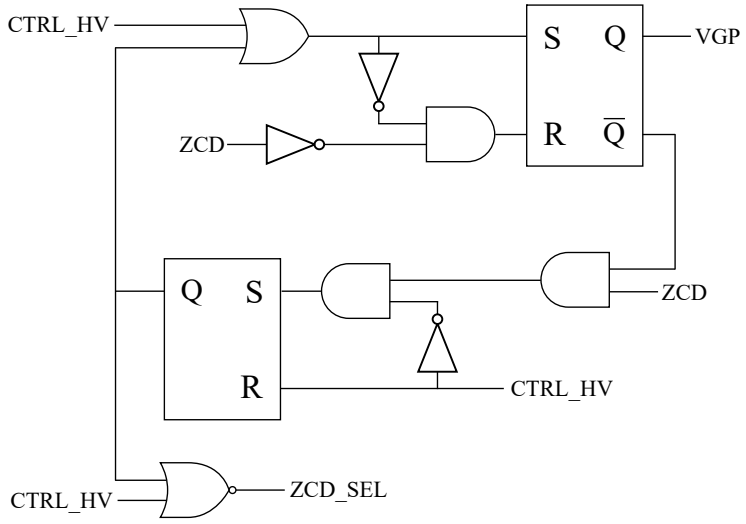


Figure 3.39: P-MOSFET logic control circuit (HV LOGIC block).

Finally, the logic circuit, depicted in Figure 3.39, is responsible to process the low-side `CTRL` (actually the up-shifted `CTRL_HV`, which is totally equivalent to `CTRL` in terms of information) and the high-side `ZCD` signals to provide the `ZCD_SEL`, `POPEN` and `VGP` (gate driving signal) digital outputs. The circuit is very simple but it guarantees a proper timing diagram, ensuring dead times between activation/deactivation of the power switches. There are four phases:

1. `CTRL='1'`, `ZCD='1'`: the n-MOSFET is closed, thus the p-one must be kept open (`VGP='1'`) and the protection circuit of the ZCD block activated (`ZCD_SEL='0'`). The top `OR` gate and the bottom `NOR` fulfill this purpose, while flip-flops are both reset. Notice that `ZCD` stays stable in state '1' thanks to the additional bias (see previous paragraphs).

2. `CTRL='0'`, `ZCD='1'`: the n-MOSFET is opening, hence a dead time must be respected before closing the p-MOSFET. This is achieved thanks to the `ZCD` signal, which is '1' until V_X goes higher than V_{out}. First of all, just after the transition of `CTRL` from '1' to '0', `ZCD_SEL` becomes '1', letting the ZCD block circuitry work. Flip-flops do not change their state until `ZCD` is low, then `VGP='0'`. This is equivalent to say that the p-MOSFET does not close until the n-MOSFET is open, because only in such condition $V_X > V_{out}$ is true. For a short time however the body diode of the p-transistor conducts,

but it is in the order of the gate driver delay ($\approx 10\,\text{ns}$), because ZCD is very fast to toggle from '1' to '0'.

3. CTRL='0', ZCD='0': p-MOSFET is closed and the circuit waits for the transitions of either ZCD or CTRL.

4. CTRL='1', ZCD='0' or CTRL='0', ZCD='1':

   – in the first case the converter is operating in CCM, because the CTRL signal goes high before ZCD is asserted, thus we are at the end of the switching period. The control however works properly thanks to an added AND gate on the low-side branch (see Figure 3.30). Its inputs are the Q signal of the main low-side flip-flop and a signal coming from the high-side control, POPEN, which is true when the p-MOSFET is open (it is the low-side equivalent of VGP). In this way a dead time before the activation of the n-MOSFET is respected, because it cannot be switched on until POPEN='1'. Notice that VGP goes towards the low-side branch via the HV-LV SHIFTER block and then the n-MOSFET driver, while it is directly connected to the p-MOSFET driver: consequently, the signal is faster ($\approx 10\,\text{ns}$ faster) to reach the p-transistor, guaranteeing in this way a dead time before the activation of the n-one.

   – in the second case the converter is operating in DCM, because ZCD is asserted before CTRL. At the first transistion of ZCD the bottom flip-flop is set, hence also the top one, causing the p-MOSFET to open. This state is kept until CTRL goes to '1'.

Referring to Figure 3.30, the two gates (OR and NOR) at the top-left are placed to ensure that when the boost converter is deactivated by the main digital control (i.e. when $\overline{EN}$='1') both the power switches are off.

3.7 Asynchronous vs synchronous design

The main figure of merit to be evaluated, which is the reason why the synchronous design has been developed, is the efficiency. The comparison has been carried out by imposing almost the same occupation of area (see Section 1.2) and by measuring then the current sunk from the battery, an ideal voltage generator in Virtuoso. As expected, using the p-MOSFET instead of the Schottky diode yields to better performances, as depicted in Figure 3.40. In the synchronous design an 87.4% peak efficiency is reached at 15 mA output current, while in the asynchronous converter it is just slightly above 85%. The average values are respectively 84.9% and 83.4%, which both fulfill the system high level specifications of Table 1.1.

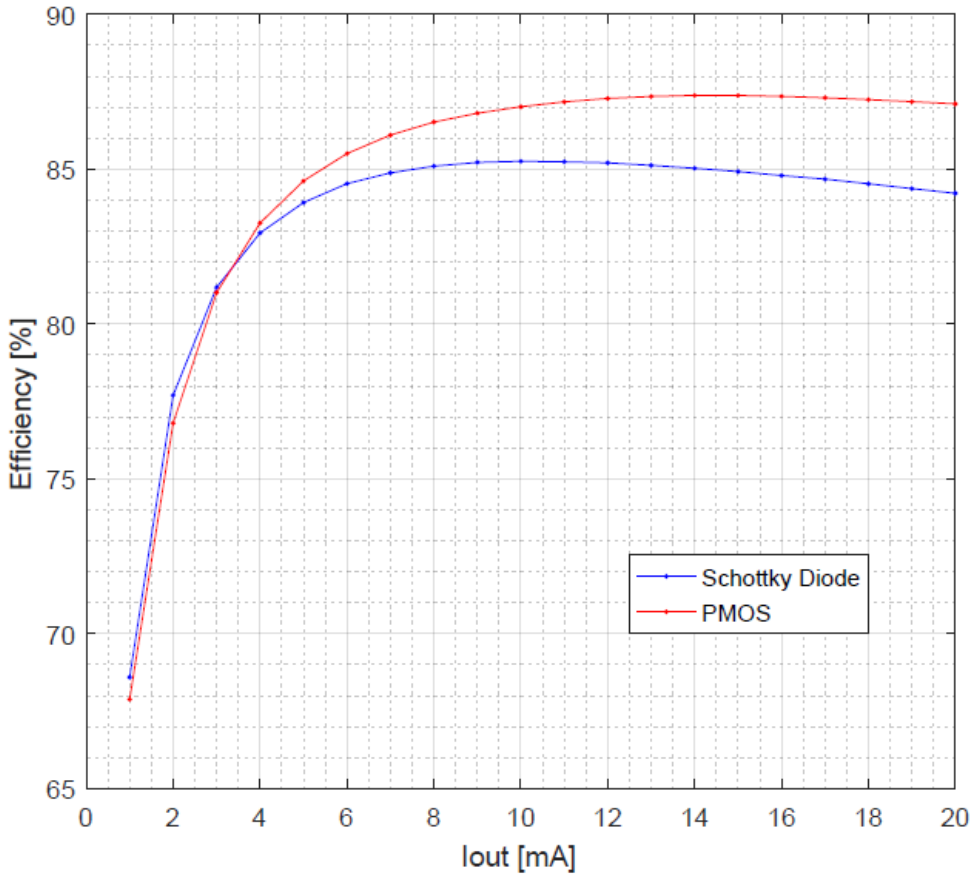


Figure 3.40: Efficiency: comparison between asynchronous and synchronous designs.

Notice that at light load the efficiency is faintly better in the asynchronous design: this is due to the losses associated to the control of the high-side p-MOSFET, which degrade performances relevantly. However, the synchronous converter has been selected and will be implemented in the SoC, even if more complex in terms of circuit.

Regarding battery lifetime, a rough analysis has been carried out. Two common cheap battery types have been selected, namely:

(a) 3 V, 225 mAh, non-rechargeable;

(b) 3.6 V, 110 mAh, rechargeable.

Considering the parameters listed at the beginning of Chapter 1, a worst case scenario is applied with: maximum number of meals per day (10), maximum pulse

width (2 ms), maximum frequency of pulses (20 Hz), maximum duration of stimulation (120 s) and always maximum output power (400 mW). Also, a DC quiescent current of 100 µA has been taken into account for the computation, representing the power consumed by the digital intelligence engine and the low-power analog front-end. By using non-rechargeable battery (a) this results in the worst lifetime of 46 days, while by using (b) 24 days. However, this is quite unrealistic, specially regarding the output power. Assuming that the load current varies within the specs range with an equiprobable distribution, the lifetimes becomes 70 and 36 days respectively. A typical scenario (mean value of the parameters) yields to 157 and 81 days.

These results show that the converter is well-suited in terms of efficiency for the application, because the battery lifetime is reasonable. Moreover, if longer duration is desired, a battery with higher capacitance can be picked.

Chapter 4

Conclusions

This thesis work has dealt with the design of a low-power integrated DC-DC boost converter for portable biomedical devices. It has been carried out in its entirely at *Imperial College London (UK), Centre for Bio-Inspired Technology* and it is part of a wider granted research project, *i2MOVE*, whose aim is to tackle obesity by electrically stimulating the vagus nerve. From high-level system specifications, the design has been fully developed till transistor-level schematic, as planned. Thus, it covers all the production steps typical of an IC, with the exception of layout generation and device testing. Various simulations showed that the converter behaves correctly and efficiently.

First of all, a quick literature review regarding DC-DC converters with similar characteristics and specifications has been performed. Among several topologies, a *switching Pulse-Width Modulated Boost converter* operating in *Discontinous Conduction Mode* with *Current Mode* control has been chosen for its good performances in terms of power efficiency and power density and its rather simple implementation. The behavior of the system, both of the power stage and the control loop, has been then analyzed and all the design formulas has been derived and next applied. By dimensioning the components and the parameters of the circuit, with the aid of a *MATLAB* script, the given specifications have been fulfilled totally in this preliminary theoretical phase. Both an *asynchronous* and a *synchronous* boost converter, i.e. respectively with a passive Schottky diode and an active power MOSFET secondary switch, has been designed: the first has the advantage to be simpler to drive, but the second is expected to be more efficient in terms of power conversion.

In order to verify functionality, the whole system has been described with a *Hardware Description Language*, namely *Verilog-A*, and simulated in *Cadence Virtuoso* software environment. However, this phase was important particularly for the extraction of the various requirements related to each component of the control loop, especially regarding those characteristics which were not straightforward to

obtain theoretically. At the end, a good description with Verilog-A enabled almost just one transistor-level design for each block, optimizing as a result the design time.

Next, every part of the circuit described in Verilog-A has been translated into an equivalent transistor-level schematic. A lot of simulations were performed demonstrating matching between the two versions. This phase has been the core of this thesis and some state-of-the-art solutions in IC design have been applied, alongside original ones which have been proposed by the author. In particular, available capacitance multiplication techniques have been exploited to enable the use of integrated capacitors and an effective drive for a high-side power transistor has been proposed.

Finally, simulations were performed to show the correct behavior and functionality of the system. The output voltage is regulated with a good accuracy, an 84.9% average efficiency has been reached in the synchronous design and the crossover frequency of the closed-loop system is at 30 kHz with approximately 60° of phase margin, thus a stable but sufficiently fast system. The whole set of initial constraints and specifications has been accomplished.

Future work

First of all, the layout of the converter has to be generated and integrated in the *i2MOVE SoC*. Then the device should be tested to verify actual functionality and performances. Optionally, if the output voltage needs to reach higher values because of issues in nerve stimulation effectiveness, a more complex topology could be implemented, specifically the cascade combination of an unregulated charge pump and the converter object of this thesis, just slightly modified. It has to be carefully investigated with respect to the control technique, but probably it is the best solution if higher conversion gains are required.

Appendix A

Code

A.1 MATLAB

The code written to evaluate the parameters and the stresses of the power stage is reported in this section.

Listing A.1: MATLAB code.

```
%% INPUT PARAMETERS and COMPUTATION
close all

Vout = 20;
L = 22*10^-6;
toff_switch = 12*10^-9;
ton_diode = 12*10^-9;
fsw = 240000;
Rds_on = 0.925;
Vdiode = 0.6;
deltaVdiode = 20;
Rfeedback = 100000;

n = 100;
I_vect = linspace(1,20,n)*10^-3;

% Inductor losses: from online Coilcraft tool
qL = 7/n*10^-3; %for LPS6235_223
PL(1) = 0.001; %for LPS6235_223
for i=1:n-1
   PL(i+1) = PL(i)+qL;
end

Vin = 3.3;

```

```
IL_peak = @(Iout)Iout*Rds_on/(2*L*fsw)*(sqrt(1+(8*L*fsw/...
    (Rds_on^2)*(Vout-Vin)/Iout))-1);
Ddcm = @(Iout)sqrt((2*L*fsw)*Iout*(Vout-Vin-...
    (IL_peak(Iout)*Rds_on/2)))/...
    (Vin-IL_peak(Iout)*Rds_on/2);
Isw_peak = IL_peak;
Isw_rms = @(Iout)Isw_peak(Iout)*sqrt(Ddcm(Iout)/3);
Id_peak = Isw_peak;
D2dcm = @(Iout)IL_peak(Iout)*L*fsw/...
    (Vout-Vin-IL_peak(Iout)*Rds_on/2);
Id_rms = @(Iout)Id_peak(Iout)*sqrt(D2dcm(Iout)/3);

PCout = 0.0003; % rough (over estimated)
PCin = 0.0002; % rough (over estimated)
PSw_cond = @(Iout)Rds_on*(Isw_rms(Iout))^2;
PSw_sw = @(Iout)fsw/2*Vout*Isw_peak(Iout)*toff_switch;
PD_cond = @(Iout)Vdiode*Iout;
    % or 5*Rds_on*(Id_rms(Iout))^2 if sync. design;
PD_sw = @(Iout)fsw/2*deltaVdiode*Id_peak(Iout)*ton_diode...
    + 0.0005; %0.0005 due to reverse recovery
PSw_gate = 0.00005; %50uW after simulations in Cadence
Pfeedback = Vout^2/Rfeedback;
PLoss = @(Iout) PCout + PCin + Pfeedback +...
    PSw_cond(Iout) + PSw_sw(Iout) + PD_cond(Iout) +...
    PD_sw(Iout) + PSw_gate; % without inductor losses

for i=1:n
    PLoss_tot(i) = PLoss(I_vect(i))+PL(i);
    POut(i) = Vout*I_vect(i);
    D(i) = Ddcm(I_vect(i));
    D2(i) = D2dcm(I_vect(i));
    ILpk(i) = IL_peak(I_vect(i));
    PSw_conducting(i) = PSw_cond(I_vect(i));
    PSw_switching(i) = PSw_sw(I_vect(i));
    PD_conducting(i) = PD_cond(I_vect(i));
    PD_switching(i) = PD_sw(I_vect(i));
end

efficiency(:) = POut(:)./(POut(:)+PLoss_tot(:));
average_efficiency = mean(efficiency(:))

%% PLOTTING: losses and efficiency
figure
subplot(1,2,1)
plot(I_vect*1000,PLoss_tot(:)*1000,'b')
title('Total power loss VS output current')
xlabel('Iout [mA]')
ylabel('PLoss [mW]')
grid 'on'
```

```
75 subplot(1,2,2)
76 plot(I_vect*1000,efficiency(:),'b')
77 title('Efficiency VS output current')
78 xlabel('Iout [mA]')
79 ylabel('Efficiency')
80 grid 'on'
81
82 %% PLOTTING: duty cycle
83 figure
84 subplot(1,3,1)
85 plot(I_vect*1000,D(:),'b')
86 title('Duty cycle VS output current')
87 xlabel('Iout [mA]')
88 ylabel('Dsw')
89 subplot(1,3,2)
90 plot(I_vect*1000,D2(:),'b')
91 title('Duty cycle passive switch VS output current')
92 xlabel('Iout [mA]')
93 ylabel('D2')
94 subplot(1,3,3)
95 plot(I_vect*1000,D2(:)/fsw*10^6)
96 title('T2 VS output current')
97 xlabel('Iout [mA]')
98 ylabel('T2 [us]')
99
100 %% PLOTTING: switching vs conduction losses
101 figure
102 subplot(1,3,1)
103 plot(I_vect*1000,PSw_conducting,'-b',...
104      I_vect*1000,PSw_switching,'-r',...
105      I_vect*1000,PD_conducting,'--b',...
106      I_vect*1000,PD_switching,'--r')
107 title('Losses VS output current')
108 xlabel('Iout [mA]')
109 ylabel('P [mW]')
110 legend('PSw_c_o_n_d','PSw_s_w','PD_c_o_n_d','PD_s_w')
111 subplot(1,3,2)
112 plot(I_vect*1000,PSw_conducting+PD_conducting,':m',...
113      I_vect*1000,PD_switching+PSw_switching+...
114         PSw_gate,'--g',...
115      I_vect*1000,PLoss_tot,'--b')
116 title('Losses VS output current')
117 xlabel('Iout [mA]')
118 ylabel('P [mW]')
119 legend('P_c_o_n_d','P_s_w','P_t_o_t')
120 subplot(1,3,3)
121 plot(I_vect*1000,(PSw_conducting+PD_conducting)./...
122         (PLoss_tot)*100,':m',...
123      I_vect*1000,(PD_switching+PSw_switching+...
```

```
124         PSw_gate)./(PLoss_tot)*100,'--g')
125 title('Normalized losses VS output current')
126 xlabel('Iout [mA]')
127 ylabel('[%]')
128 legend('P_c_o_n_d','P_s_w')
```

A.2 Verilog-A modules

In this section the complete code of each Verilog-A module is reported.

Listing A.2: Current sensor Verilog-A module code.

```
1  // VerilogA for Design_HV, current_sensor, veriloga
2
3  `include "constants.vams"
4  `include "disciplines.vams"
5
6  module current_sensor(a,b,out,vref);
7  input a,b;
8  inout out,vref;
9  electrical a,b,out,vref;
10 parameter Rs = 3.57;
11
12     analog begin
13         I(vref,out) <+ I(a,b);
14         I(out,vref) <+ V(out,vref)/Rs;
15     end
16
17 endmodule
```

Listing A.3: Comparator Verilog-A module code.

```
1  // VerilogA for Design_HV, comp_SE, veriloga
2
3  `include "constants.vams"
4  `include "disciplines.vams"
5
6  module comp_SE(in_p, in_n, out, vref, vsup);
7  input in_n, in_p, vsup, vref;
```

```
8  output out;
9  electrical in_n, in_p, vref, vsup, out;
10 parameter real comp_slope = 5;
11 parameter real in_offset = 0.0;
12 parameter real drop_out = 0.5;
13
14     analog begin
15         V(out,vref) <+ 0.5*(V(vsup,vref)-drop_out)*
16             tanh(comp_slope*(V(in_p,in_n)-in_offset))
17             +0.5*V(vsup,vref);
18         end
19
20 endmodule
```

Listing A.4: Comparator with hysteresis Verilog-A module code.

```
1  // VerilogA for Design_Boost, comp_hyst, veriloga
2
3  `include "constants.vams"
4  `include "disciplines.vams"
5
6  module comp_hyst(in_n,in_p,vsup,vref,out);
7  input in_n,in_p,vsup,vref;
8  output out;
9  electrical in_n,in_p,vsup,vref,out;
10 parameter real offset = 0.2; //hysteresis threshold
11 parameter real t_delay = 1e-9;
12 parameter real t_rf = 5e-9;
13 parameter real drop_out = 0.1;
14 integer state;
15
16     analog begin
17         state = V(in_p,vref) > (V(in_n,vref) +
18             (state ? -offset : offset)) ? 1:0;
19         V(out,vref) <+ transition(state*V(vsup,vref),
20             t_delay, t_rf, t_rf);
21     end
22
23 endmodule
```

Listing A.5: Set-reset flip-flop Verilog-A module code.

```
// VerilogA for Design_HV, flipflop, veriloga

`include "constants.vams"
`include "disciplines.vams"

module flipflop(vsupply, vref, reset, set, q);
input vsupply, vref, reset, set;
output q;
electrical vsupply, vref, reset, set, q;
parameter real thresh = 0.9; // threshold
parameter real delay_ = 1e-9;
parameter real rf_time = 5e-9; //rise and fall time
integer memory;

    analog begin

        @(initial_step) begin
            memory = 0;
        end

        if (V(reset,vref) >  thresh)
            memory = 0;
        else if (V(set,vref) > thresh)
            memory = 1;

        V(q,vref) <+ transition(memory*V(vsupply,vref),
            delay_, rf_time, rf_time);

    end

endmodule
```

Listing A.6: Level shifter and gate driver Verilog-A module code.

```
// VerilogA for Design_Boost, level_shifter, veriloga

`include "constants.vams"
`include "disciplines.vams"

module lev_shifter(Vin,Vout,Vref,Vsup);
input Vin,Vref,Vsup;
output Vout;
```

```
electrical Vin,Vref,Vsup,Vout;
parameter real imax = 0.01;
parameter real vin_max = 1.8;
parameter real drop_out = 0.2;
real rout, gain;
electrical temp;

    analog begin

        // if Val is expected to change in time
        // put rout and gain calculation outside
        // initial step; otherwise put them into
        // that, so simulation time is reduced

        @(initial_step) begin
            rout = V(Vsup,Vref)/imax;
            gain = (V(Vsup,Vref)-2*drop_out)/vin_max;
        end

        V(temp,Vref) <+ drop_out + gain*V(Vin,Vref);
        I(temp,Vout) <+ V(temp,Vout)/rout;
    end

endmodule
```

Listing A.7: Op-amp Verilog-A module code.

```
// VerilogA for Design_HV, opamp, veriloga

`include "discipline.h"
`include "constants.h"

//
// Based on the OVI Verilog-A Language Reference Manual,
// version 1.0 1996
//

`define PI      3.141592653589793

//--------------------
// opamp
//
```

```
16 // vin_p,vin_n: differential input voltage [V]
17 // vout: output voltage [V]
18 // vref: reference voltage [V]
19 // vspply:      positive supply voltage [V]
20 //
21 // INSTANCE parameters
22 //    gain = gain []
23 //    GBW = unity gain frequency [Hz]
24 //    Rin = input resistance [Ohms]
25 //    Vin_offset = input offset voltage referred
26 //        to negative [V]
27 //    Imax = maximum current [A]
28 //    SR = slew rate [A/F]
29 //    Rout = output resistance [Ohms]
30 //    Vsoft = soft output limiting value [V]
31 //
32
33 module opamp(vout, vref, vin_n, vin_p, vspply);
34 input vref, vspply;
35 inout vout, vin_p, vin_n;
36 electrical vout, vref, vin_p, vin_n, vspply;
37 parameter real gain = 10e3;
38 parameter real GBW  = 10e6;
39 parameter real Rin = 1e9;
40 parameter real vin_offset = 0.01;
41 parameter real Imax = 1e-3;
42 parameter real SR = 5e6;
43 parameter real Rout = 500;
44 parameter real Vsoft = 0.05;
45    real c1;
46    real gm;
47    real r1;
48    real vmax_in;
49    real vin_val;
50    electrical cout;
51
52    analog begin
53
54       @ ( initial_step or initial_step("dc") ) begin
55          c1 = Imax/(SR);
56          gm = 2 * `PI * GBW * c1;
57          r1 = gain/gm;
58          vmax_in = Imax/gm;
```

```
59          end
60
61          //
62          // Input stage.
63          //
64          vin_val = V(vin_p,vin_n) + Vin_offset;
65          I(vin_p, vin_n) <+ vin_val/ Rin;
66
67          //
68          // GM stage with limited output current.
69          //
70          if (vin_val > vmax_in)
71             I(vref, cout) <+ Imax;
72          else if (vin_val < -vmax_in)
73             I(vref, cout) <+ -Imax;
74          else
75             I(vref, cout) <+ gm*vin_val;
76
77          //
78          // Dominant Pole.
79          //
80          I(cout, vref) <+ ddt(c1*V(cout, vref));
81          I(cout, vref) <+ V(cout, vref)/r1;
82
83          //
84          // Output Stage.
85          //
86          I(vref, vout) <+ V(cout, vref)/Rout;
87          I(vout, vref) <+ V(vout, vref)/Rout;
88
89          //
90          // Soft Output Limiting.
91          //
92          if (V(vout,vref) > (V(vspply,vref) - Vsoft))
93             I(cout, vref) <+ gm*(V(vout, vspply)+Vsoft);
94          else if (V(vout,vref) < Vsoft)
95             I(cout, vref) <+ gm*(V(vout,vref)-Vsoft);
96       end
97
98    endmodule
```

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